

MP1800A Series

Signal Quality Analyzer

32 Gbit/s Signal Integrity Test Solution



Welcome to a 32-Gbit/s



Computer

Server

100GbE (25Gx4): 100GBASE-CR4, KR4
Infiniband EDR (26G)
32G Fibre Channel
High Speed Back Plane
Active Optical Cable (AOC)

For R&D in High-speed Interconnects and 100 GbE Devices

The growing demands of cloud computing and high-definition video streaming are driving increases in server and storage transmission speeds as well as in the transmission capacity of core networks. To meet these needs, the transmission speeds of physical-layer devices and modules are increasing, making signal integrity analysis ever more important in assuring quality. Installing the 28/32G Multi-Channel PPG and ED Module supports PCBs with high-speed interconnects up to 32.1 Gbit/s, BER measurements for device R&D, and simultaneous measurement of crosstalk between multi-channels, for more accurate signal integrity analysis.

100GbE (25Gx4)
OTU4 (28Gx4)
32G DP-QPSK for Long Haul
CEI-25G, CEI-28G-VSR
CFP/CFP2, QSFP/QSFP2 Module

Optical Module

Network Equipment

World

Module Configurations for Multi-channel BER and Jitter Measurements

MP1800A SQA is a modular BERT with plug-in modules;

- Pulse Pattern Generator (PPG) supporting high quality output and high amplitude signals
- Error Detector (ED) with high input sensitivity supporting signal analysis, such as Bathtub and Eye Diagram measurements
- Jitter Modulation Source (JMS) for generating various types of jitter, such as SJ/RJ/BUJ/SSC, and supporting Jitter Tolerance tests

32.1
Gbit/s

Wideband bit rates
from up to
32.1 Gbit/s

Up to
8
ch

Multi-channel synchronized
pattern generation and
simultaneous BER analysis

High Sensitivity
10
mV

High sensitivity ED
10 mV (Type.
Single-ended,
Eye Height)



MP1800A

Versatile signal integrity measurement functions

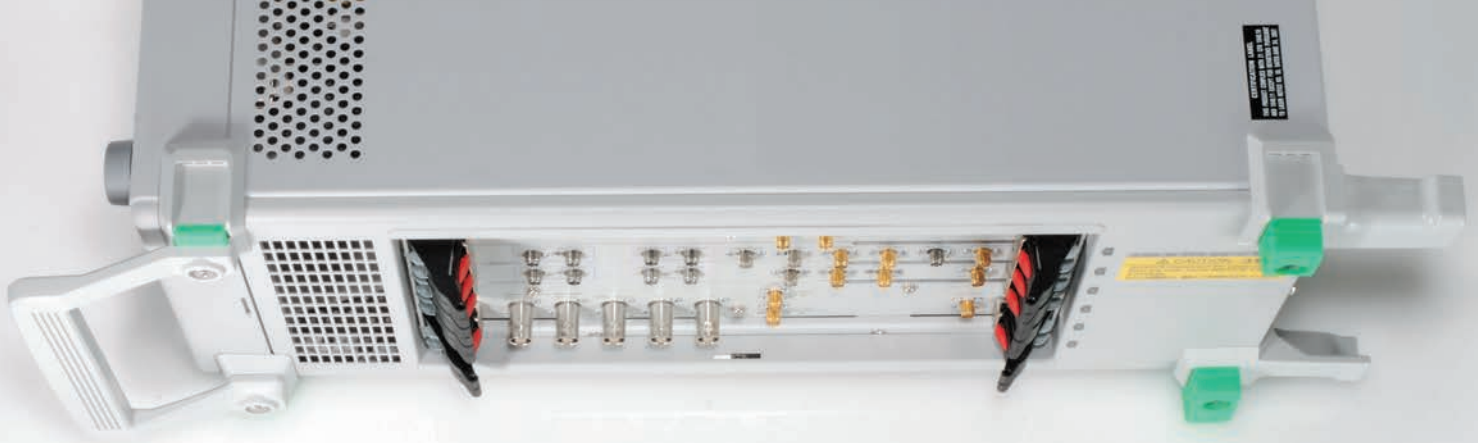
- ▶ T/J/DJ/RJ/Bathtub Jitter, Eye Diagram, Eye Margin auto-measurements
- ▶ 32.1 Gbit/s Jitter Tolerance tests
(using MU181500B, supports RJ/SJ/BUJ/SSC generation)
- ▶ 4-tap Emphasis signal generation up to 32.1 Gbit/s (using MP1825B)
- ▶ Crosstalk testing with independent variable data skew per channel

Excellent signal quality and Rx sensitivity

- ▶ 10 mV high input sensitivity Error Detector (ED)
- ▶ Low-jitter, High-quality waveforms
- ▶ Up to 3.5 Vp-p output amplitude enables direct-drive EML
- ▶ 4PAM/8PAM Signal Generation
(using MZ1834A/MZ1838A)

Data patterns for various applications

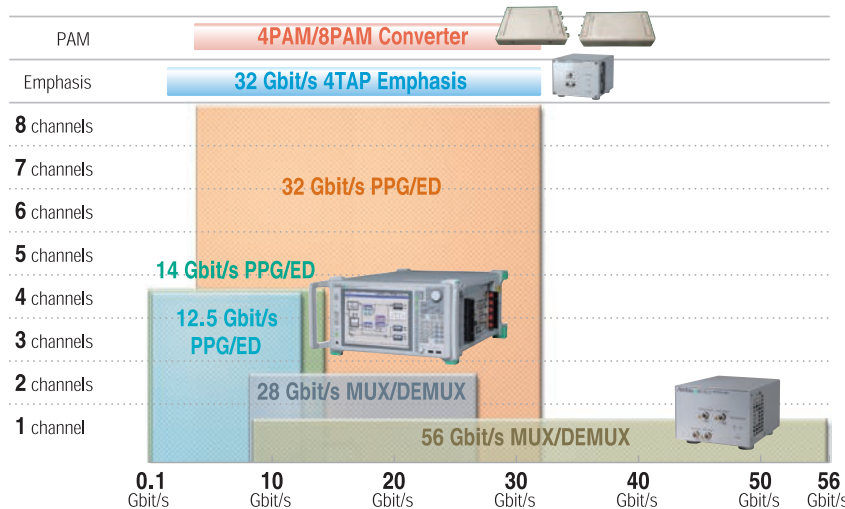
- ▶ DQPSK, DP-QPSK Pre-coding
- ▶ Burst Signal tests
- ▶ Programmable data patterns up to 256 Mbit/channel
CJTPAT, CJPAT, K28.5, etc.



Covers Wide Range of Bandwidths and Channels

Anritsu Signal Integrity Test Solution for Every Need

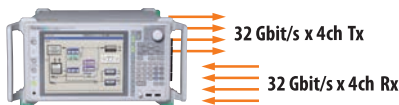
Adding the 32 Gbit/s module to the MP1800A Signal Quality Analyzer supports evaluation of the physical layer for optical modules and high-speed interconnects up to 32.1 Gbit/s. Combined installation with the synthesizer and Jitter modules supports a test environment without external signal generator. Moreover, powerful signal integrity tests at up to 32.1 Gbit/s are supported by linked operation with the MP1825B 4Tap Emphasis, MZ1834A 4PAM Converter and MZ1838A 8PAM Converter. In addition, bit rates are supported down to 0.1 Gbit/s by changing modules as well as up to 56 Gbit/s by connecting an external MUX/DEMUX (MP1821A/MP1822A).



POINT

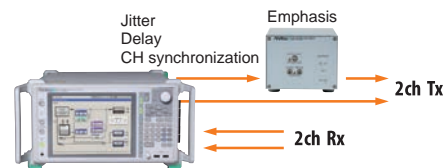
1 Supports up to 8 channels in 32 Gbit/s Band

The 4ch PPG and 4ch ED synthesizer configuration supports all-in-one evaluation of 4ch TRx devices, cutting total costs and saving space.



2 Signal Integrity Analysis using Jitter, Data Delay and 4Tap Emphasis

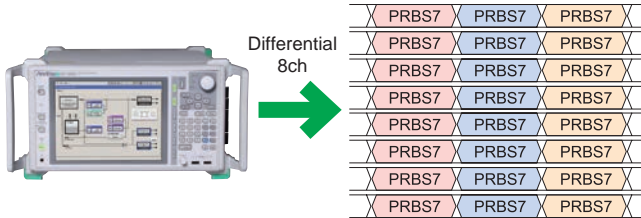
Jitter generation, Crosstalk tests using Data Delay, and Emphasis generation are essential tools at signal integrity analysis of high-speed interconnects. As the ideal solution, the all-in-one MP1800A supports a 2ch PPG and 2ch ED configuration with Jitter modulator, synthesizer, and individual variable delay functions, while linked operation with the compact MP1825B 4Tap Emphasis gets as close as possible to the DUT.



Features

Synchronization up to 8ch

Due to the modular platform design, the PPG/ED modules can be configured with various other modules to configure custom systems. The number of channels per 28G/32G PPG/ED module can be selected from 1, 2, or 4 and PPG/ED modules can be installed to support up to 8ch. Moreover, since each channel pattern can be synchronized, D/A converters, MUX/DEMUX, crosstalk, and skew tolerance can be evaluated.



*: For details about possible module combinations, see the Option Selection Guide for the MP1800A series.

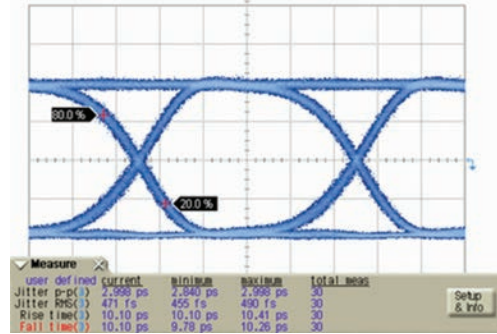
Low-jitter, High-quality Waveform

The PPG module supports low-jitter and high-quality waveforms. The output amplitude can be customized to application needs.

Low-jitter: 700 fs rms (typ.)

High amplitude: 0.5 Vp-p to 3.5 Vp-p

[MU183020A-013/023, MU183021A-013]



Output Waveform at 28 Gbit/s, 3.5 Vp-p (MU183020A-013)

High Sensitivity Error Detector (ED)

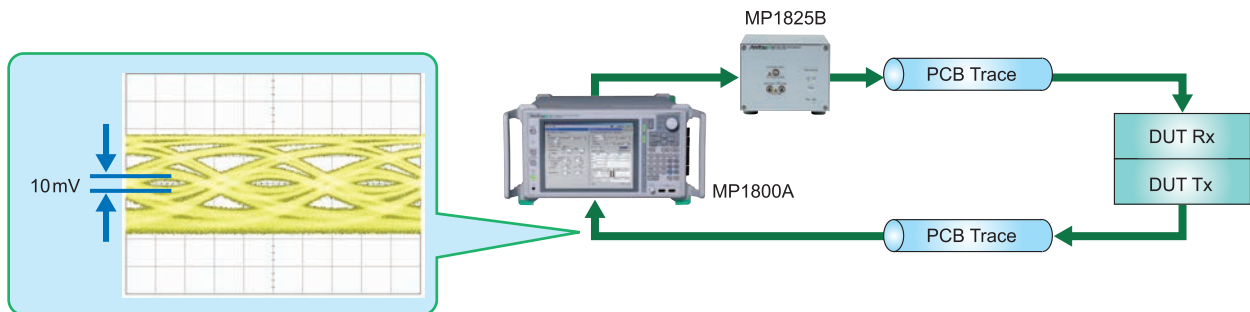
MU183040B/MU183041B 28 G/32 Gbit/s High Sensitivity ED extends the performance of the earlier A-type ED to offer world's best Rx sensitivity* with the world's fastest Auto Adjust* (auto-align of threshold level and phase points).

The MU183040B/41B High Sensitivity ED supports simultaneous multichannel measurements of low-amplitude, low Eye Opening DUTs such as High Speed Back Plane devices and Active Optical Cable (AOC) to achieve more-accurate, ideal signal quality analysis.

Eye Amplitude Sensitivity: 15 mVp-p (Typ. 28.1 Gbit/s, Single-end), ≤25 mVp-p (28.1 Gbit/s, Single-end)

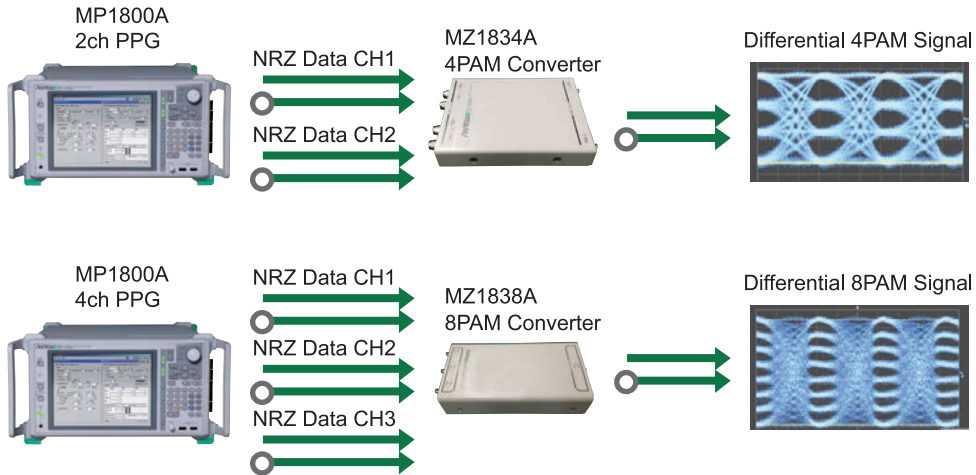
Eye Height Sensitivity: 10 mVp-p (Typ. 28.1 Gbit/s, Single-end)

*As of September, 2013



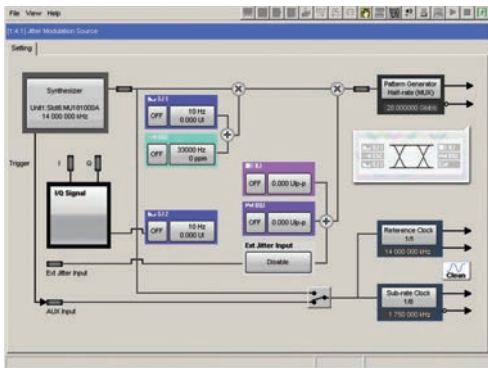
4PAM/8PAM Signal Generation

Combining the Anritsu MZ1834A/MZ1838A 4/8 PAM Converter with the MP1800A Signal Quality Analyzer supports generation of both 4PAM and 8PAM signals for R&D High Speed Back Plane and 400 GbE R&D. The MP1800A high-quality NRZ waveform and wideband passive PAM converter generate high-quality PAM signals with assured S/N.

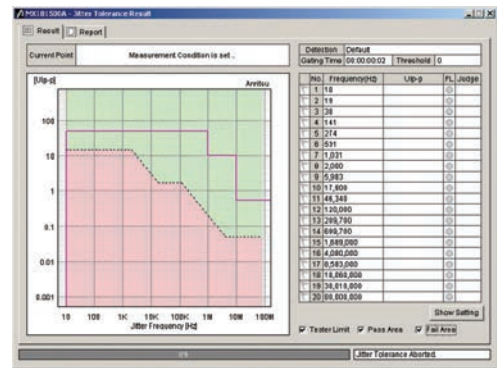


SJ, RJ, BUJ and SSC Jitter Generation Supporting 32.1 Gbit/s

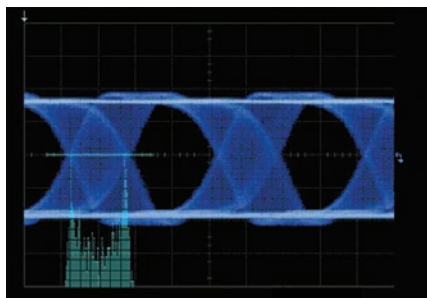
The intrinsic jitter of the clock output from the MU181500B Jitter Modulation Source is less than 350 fs rms. The combination of low-jitter waveform with excellent jitter transparency supports high-accuracy Jitter Tolerance tests. Moreover, simultaneous injection of RJ, BUJ and SSC as well as dual SJ for two-tone supports various Jitter Tolerance tests. Additionally, the MX181500A Jitter/Noise Tolerance Test Software supports multi-mask tables as well as easy mask editing to support next-generation standards.



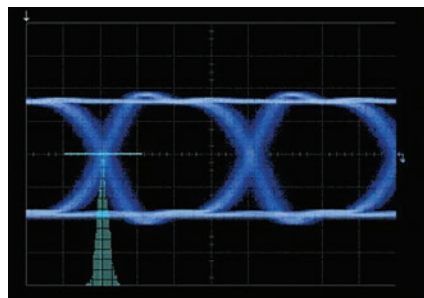
MU181500B Jitter Modulation Source Setting Screen



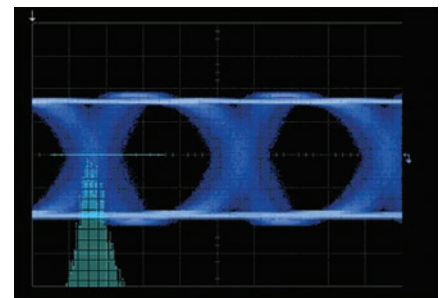
MX181500A Jitter/Noise Tolerance Test Software Setting Screen



Sinusoidal Jitter (SJ)



Random Jitter (RJ)



Bounded Uncorrelated Jitter (BUJ)

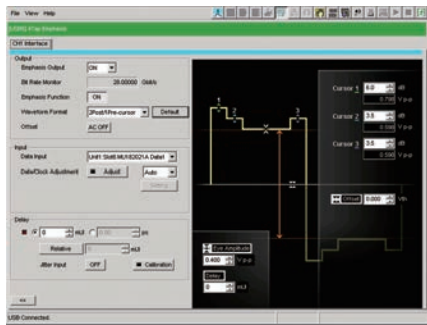
4Tap Emphasis

Combined use with the MP1825B 4Tap Emphasis supports generation of pre-emphasis 2- and 3-tap signals for standards up to 32.1 Gbit/s as well as 4-tap signals. The effect of pre-emphasis can be confirmed accurately because each tap can be changed independently.

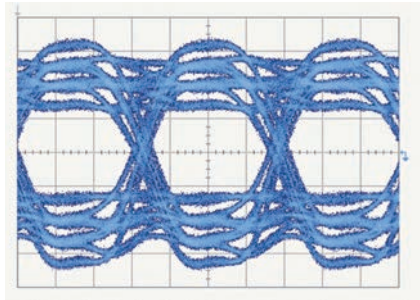
Since the MP1825B can be installed as a remote head for the MP1800A close to the Device Under Test (DUT), the shorter cables keeping signal quality high. Accurate Jitter Tolerance tests corrected using pre-emphasis signals are supported by the transparent input data and clock jitter.



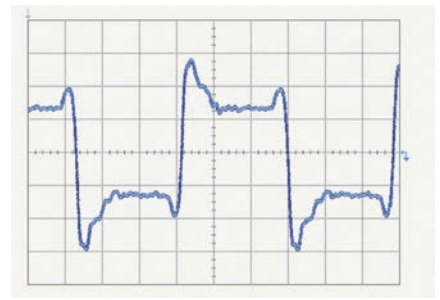
MP1825B



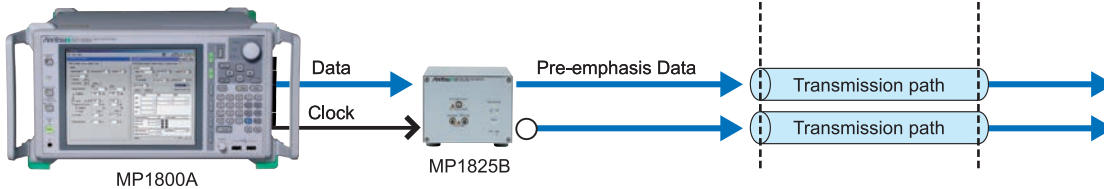
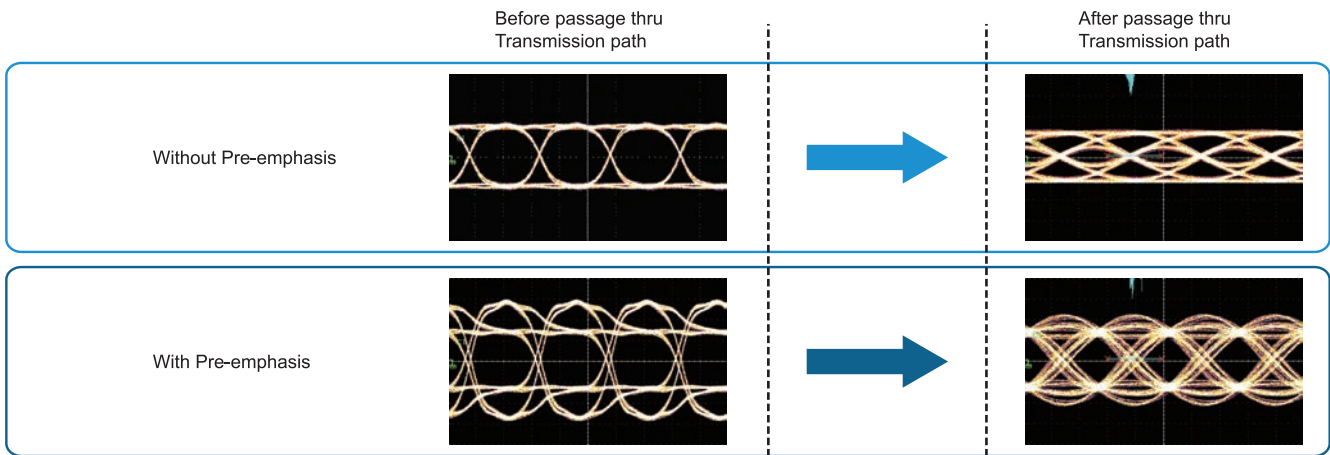
MP1825B 4Tap Emphasis Setting Screen



Waveform with PRBS31 Test Pattern



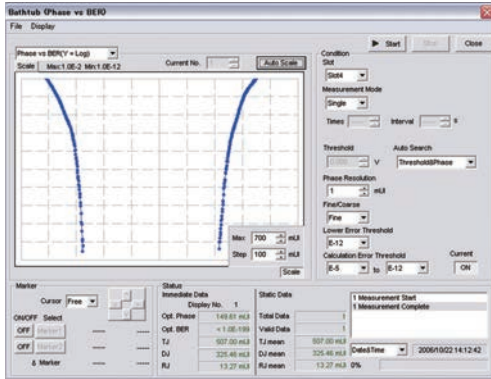
Waveform with FF00 Test Pattern



Optimizing Pre-emphasis Effect

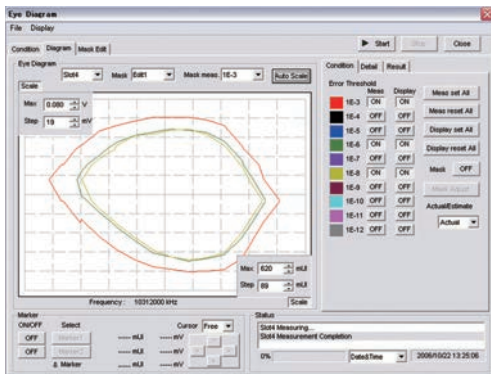
Bathtub Jitter

Measures optimum bit error rate based on changes in bit error rate relative to phase margin and performs jitter analysis (TJ, DJ, RJ).



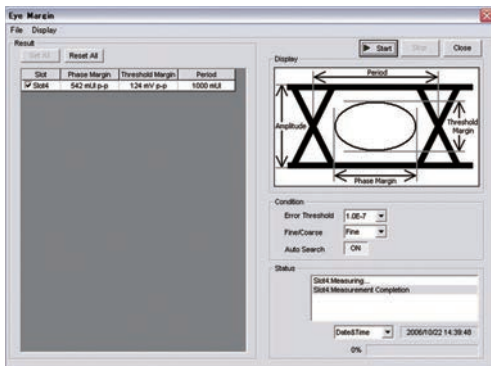
Eye Diagram

Captures bit error rate contours linking specified bit error rate points.



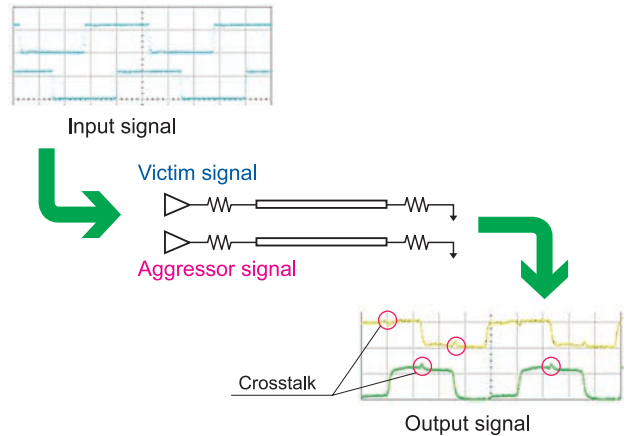
Eye Margin

Confirms Data threshold and phase margins.



Crosstalk Test

Independently controls phase for each channel using built-in PPG Data Delay option to examine DUT crosstalk characteristics with excellent accuracy in 1-mUI steps.



Versatile Pattern Generation

• Pseudorandom Patterns (PRBS)

All PRBS patterns required by standards are supported up to PRBS $2^{31} - 1$.

$$2^n - 1 \quad (n = 7, 9, 10, 11, 15, 20, 23, 31)$$

• Zero Substitution Pattern

Consecutive 0 s and 1 s patterns can be added to PRBS patterns for CDR tolerance tests.

$$2^n, 2^n - 1 \quad (n = 7, 9, 10, 11, 15, 20, 23)$$

• Data Pattern

Patterns required by each application, such as CJTPAT, CJPAT and K28.5 can be created flexibly.

256 Mbits/ch max. (Steps: 1 bit)

• Mixed Pattern

A mixed data and PRBS pattern can be output. At creation of SONET/SDH frames, adding a PRBS $2^{31} - 1$, etc., pattern to the payload supports setting of a continuous pattern across frames.

• Pre-code

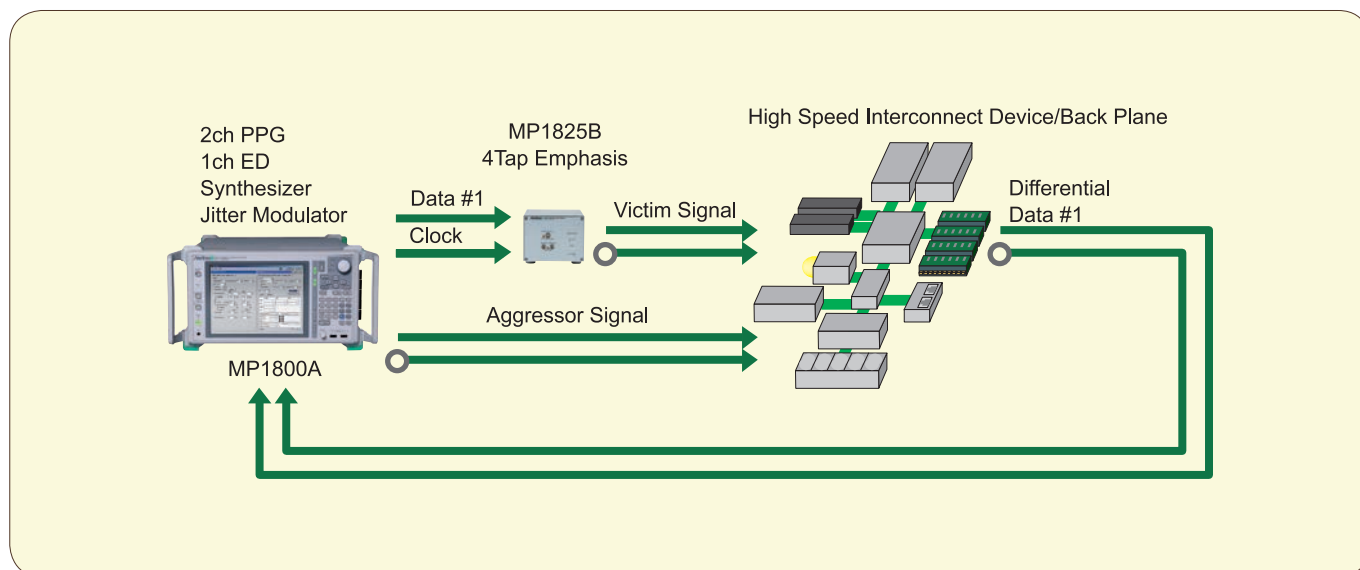
The DQPSK and DP-QPSK pre-code signal generation are supported. Hardware-based generation of modulation signals produces pure PRBS31 signals without pattern length restrictions.

• Burst Signals

Application evaluation using burst signals, such as optical loop test and transmission test using quantum noise technology are supported.

Application

30 Gbit/s Band Ultrafast Interconnect Evaluation



Required Test Items

- 32.1 Gbit/s Multi-channel signal generation
- Jitter Tolerance test
- Emphasis efficiency check
- Crosstalk test

Multi-channel

Along with support for multi-channels, the bit rate of devices such as back planes of high-performance servers is becoming increasingly faster. The MP1800A supports generating both the Victim signal with controlling Emphasis and the Aggressor signal for crosstalk testing simultaneously. The MP1800A offers multi-channel measurements for TRx devices such as Transceiver and Clock Data Recovery (CDR).

Skew and Crosstalk Effect Check

Processing high speed digital signals requires both logic tests and actual equipment tests. The MP1800A supports both pattern synchronization and phase adjustment functions, permitting easy tests of Rx device skew tolerance and crosstalk effects.

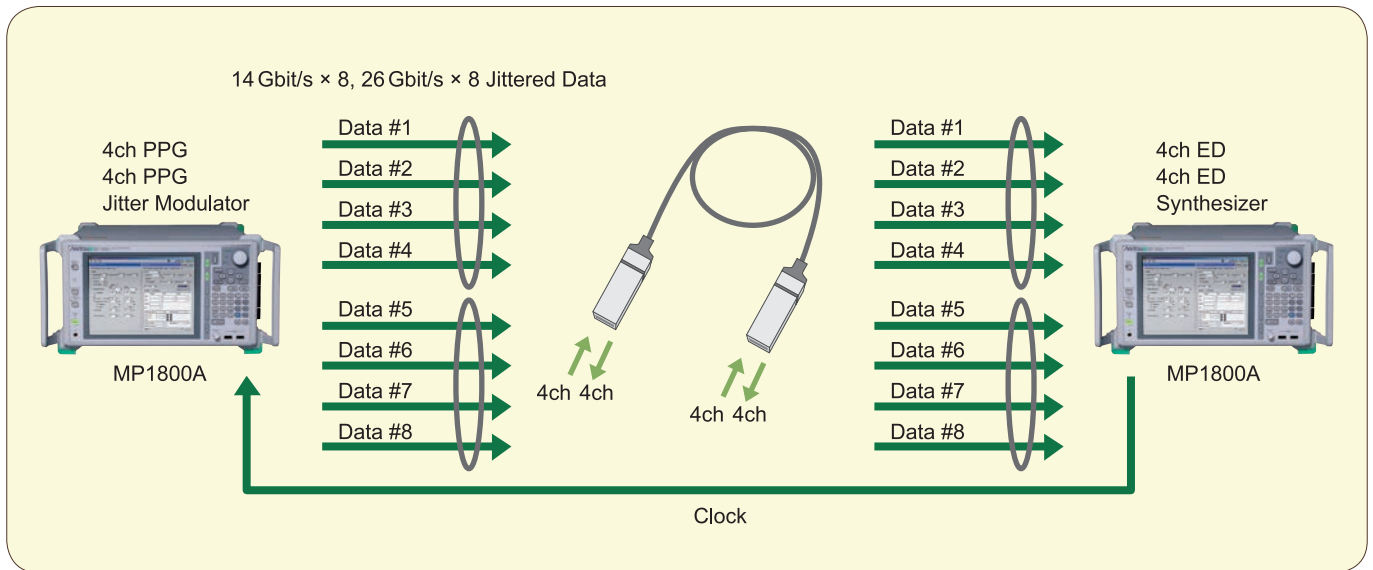
Jitter Tolerance Test

The MU181500B Jitter Modulation Source supports jitter tolerance tests of various standards because it can add SJ (two types), RJ, BUJ, and SSC simultaneously at up to 32.1 Gbit/s.

Verifying Emphasis Effect

The MP1825B 4Tap Emphasis is a 4 taps pre-emphasis converter for bit rates up to 32.1 Gbit/s; it supports easy changes to the pre-emphasis waveform amplitude, offset, amplitude of each taps, etc., for effective evaluation of the characteristics of high-speed interfaces below 10 Gbit/s, such as PCIe, USB, and Backplane Ethernet requiring pre-emphasis signals, as well as Infiniband 26G-IB-EDR, CEI-28G-VSR, 32G FC, etc., in the 30 Gbit/s band.

Infiniband FDR (14G)/EDR (26G) AOC Evaluation



Required Test Items

- Simultaneous 8ch (2 × 4ch end-to-end) BER measurement
- Crosstalk test
- Jitter Tolerance test
- Bathtub Jitter, Eye Diagram analysis

8ch (2 × 4ch End-to-End) Simultaneous Measurement

Infiniband QSFP-type active optical cables (AOC) support simultaneous transmission for up to 8 channels using 2 × 4ch end-to-end transmission. One MP1800A unit supports up to 8ch (with PPG 8ch, ED 8ch, or PPG 4ch + ED 4ch installed) and all channels can be measured simultaneously using two MP1800A units for fast measurement with high performance.

Jitter Tolerance Test

The MU181500B Jitter Modulation Source supports Jitter Tolerance tests of various standards because it can add SJ (two types), RJ, BUJ, and SSC simultaneously at up to 32.1 Gbit/s.

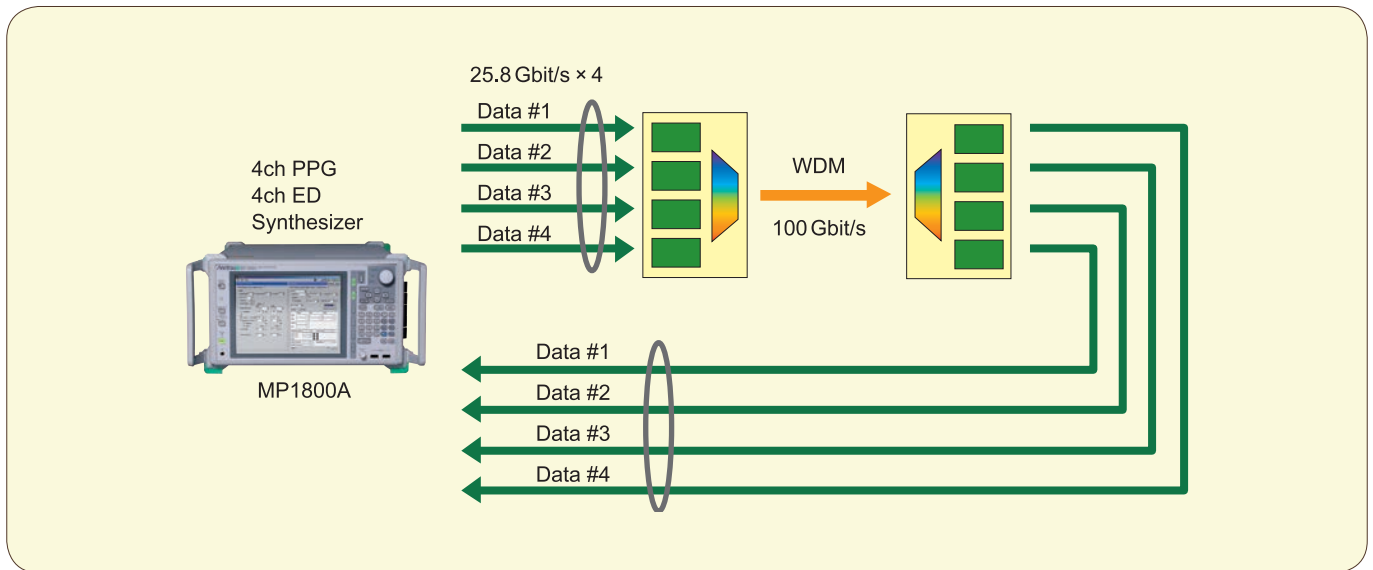
Crosstalk Effect Check

Processing high-speed digital signals requires both logic tests and actual equipment tests. The MP1800A supports both pattern synchronization and phase adjustment for each channel, permitting easy testing of AOC crosstalk effects.

Bathtub Jitter and Eye Diagram Analysis

The built-in ED Clock Delay function supports Bathtub Jitter (TJ, RJ, DJ) analysis. Low bit error rates of 1E-12, 1E-15, etc., can be estimated quickly from transitions in bit error rate versus phase.

100 GbE EML Device Evaluation



Required Test Items

- Simultaneous 4ch BER measurement
- Optical output waveform optimization using cross-point adjustment
- Inter-lane timing and skew control
- Input sensitivity test

100 GbE, 25G × 4λ Evaluation

The MP1800A can evaluate EML devices and optical modulators for 100-GbE standardized by IEEE802.3ba using PPG/ED modules supporting bit rates up to 32.1 Gbit/s. 4ch EML devices can be driven independently and simultaneously for accurate evaluation with excellent cost performance.

Optimum Signal Quality for EML Evaluation

EML devices can be direct-driven by the Variable Data Output Function at up to 3.5 Vp-p. The amplitude and crosspoint are easily adjusted on-screen, shortening evaluation times and offering high-reliability evaluation.

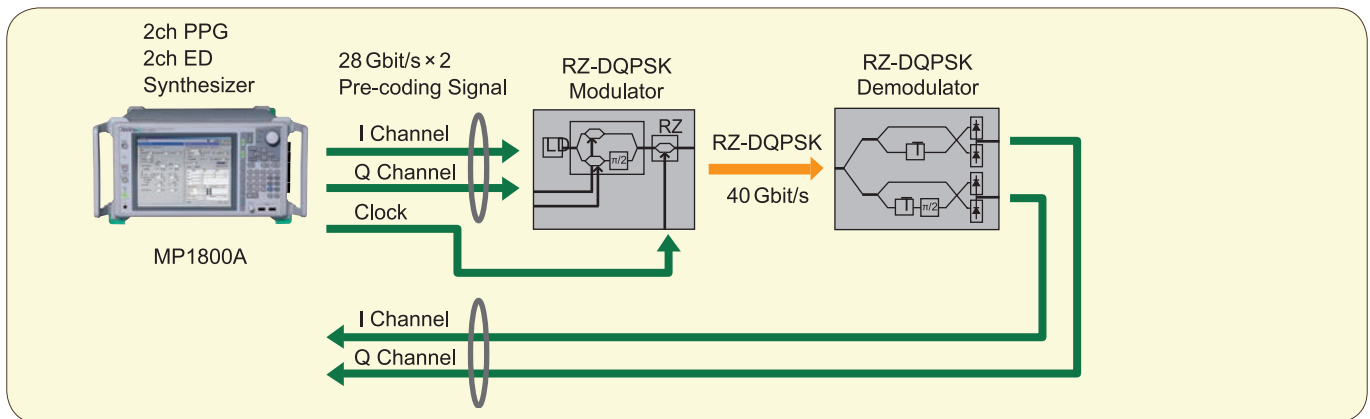
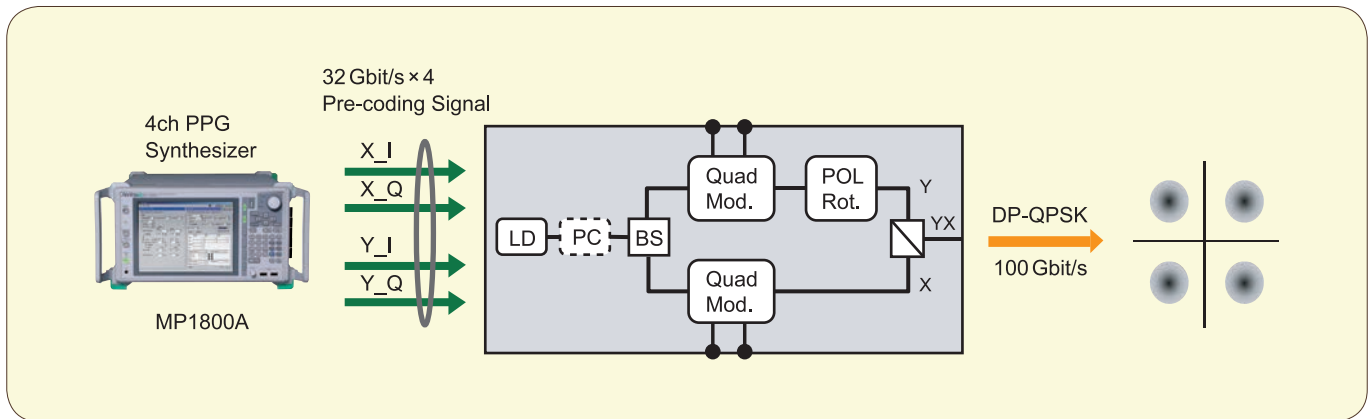
Skew and Crosstalk Effect Check

Applications using high-speed digital signals require both logic tests and actual equipment tests. The MP1800A supports both pattern synchronization and phase adjustment functions, permitting easy tests of Rx device skew tolerance and crosstalk effects.

Built-in Auto Search Function

Auto-adjustment of data and clock error is simplified using the built-in Auto Search function.

100 Gbit/s Band DP-QPSK and 40 Gbit/s Band DQPSK Evaluation



Required Test Items

- Pre-coding signal generator synchronized between channels
- Optical output waveform optimization using cross-point adjustment
- Timing control and skew control between channels
- Modulator input level tolerance

2ch/4ch Synchronization Pre-code Signal Generation

The Pre-code function automatically generates 100G DP-QPSK and 40G DQPSK modulation signals for evaluating optical modulators. Hardware-based generation of modulation signals produces pure PRBS31 signals without pattern length restrictions, resulting in high-reliability evaluations using high-load pseudo-random patterns closely approximating real signals.

Skew Effect Check

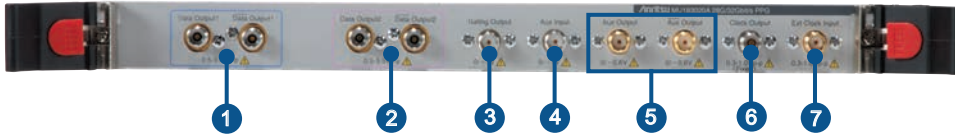
Processing high-speed digital signals requires both logic tests and actual equipment tests. The MP1800A supports both pattern synchronization and phase adjustment functions, permitting easy tests of Rx device skew tolerance and crosstalk effects.

Optimum High-quality Waveform for MZ-Modulator Evaluation

MZ-Modulator can be direct-driven by the Variable Data Output function at up to 3.5 Vp-p. The amplitude and crosspoint are easily adjusted on-screen, shortening evaluation times and offering high-reliability evaluation.

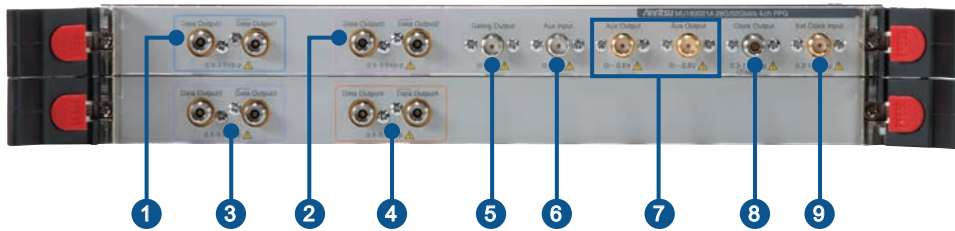
Module Panel Layout

• MU183020A 28G/32G bit/s PPG (1ch or 2ch)



1	Data1/XData1 Output*1	Output for Ch1 differential data signal	5	Aux/XAux Output	Output for differential auxiliary signal
2	Data2/XData2 Output*2	Output for Ch2 differential data signal	6	Clock Output	Output for clock signal
3	Gating Output	Output for burst timing signal	7	Ext Clock Input	Input for external clock signal
4	Aux Input	Input for auxiliary signal			

• MU183021A 28G/32G bit/s 4ch PPG



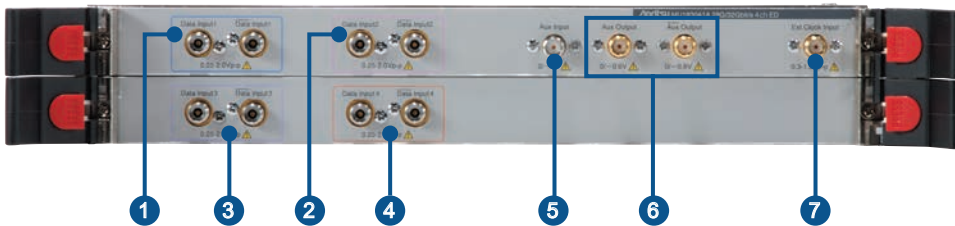
1	Data1/XData1 Output	Output for Ch1 differential data signal	6	Aux Input	Input for auxiliary signal
2	Data2/XData2 Output	Output for Ch2 differential data signal	7	Aux/XAux Output	Output for differential auxiliary signal
3	Data3/XData3 Output	Output for Ch3 differential data signal	8	Clock Output	Output for clock signal
4	Data4/XData4 Output	Output for Ch4 differential data signal	9	Ext Clock Input	Input for external clock signal
5	Gating Output	Output for burst timing signal			

• MU183040A 28G/32G bit/s ED (1ch or 2ch) • MU183040B 28G/32G bit/s High Sensitivity ED (1ch or 2ch)



1	Data1/XData1 Input*1	Input for Ch1 differential data signal	4	Aux/XAux Output	Output for differential auxiliary signal
2	Data2/XData2 Input*2	Input for Ch2 differential data signal	5	Ext Clock Input	Input for external clock signal
3	Aux Input	Input for auxiliary signal			

• MU183041A 28G/32G bit/s 4ch ED • MU183041B 28G/32G bit/s 4ch High Sensitivity ED

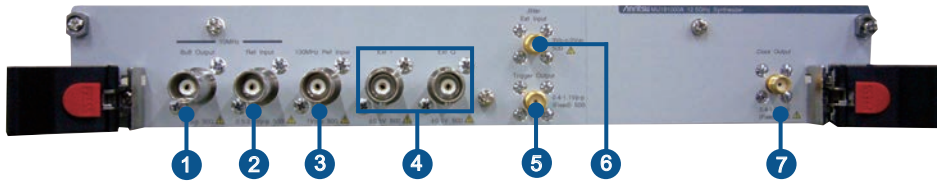


1	Data1/XData1 Input	Input for Ch1 differential data signal	5	Aux Input	Input for auxiliary signal
2	Data2/XData2 Input	Input for Ch2 differential data signal	6	Aux/XAux Output	Output for differential auxiliary signal
3	Data3/XData3 Input	Input for Ch3 differential data signal	7	Ext Clock Input	Input for external clock signal
4	Data4/XData4 Input	Input for Ch4 differential data signal			

*1: Data/XData when 1ch option was selected.

*2: Not implemented when 1ch option was selected.

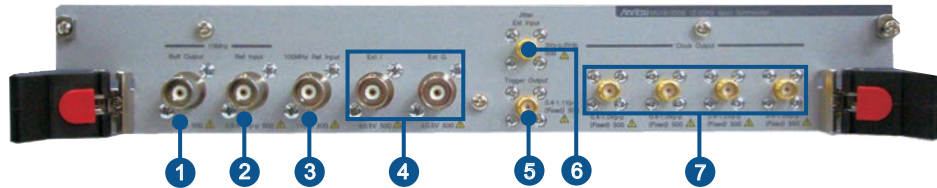
• **MU181000A 12.5 GHz Synthesizer**



1	10 MHz Buff Output	Output for 10 MHz reference clock	5	Trigger Output*1	Output for 1/64 clock or 1/1 clock
2	10 MHz Ref Input	Input for 10 MHz reference clock	6	Jitter Ext Input*1	Input for jitter modulation signal
3	100 MHz Ref Input*1	Input for 100 MHz reference clock	7	Clock Output	Clock output
4	Ext I, Q*1	Input for I, Q signal			

*1: Only enabled when Jitter Modulation option (MU181000A-001) installed

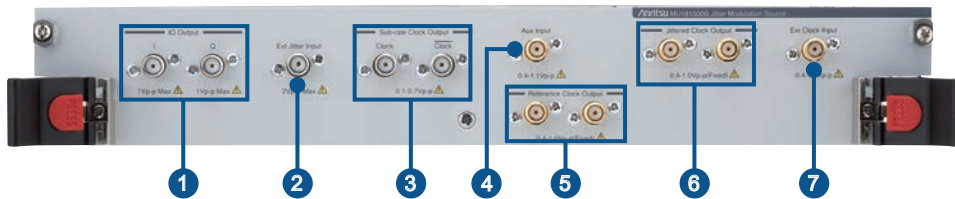
• **MU181000B 12.5 GHz 4 Port Synthesizer**



1	10 MHz Buff Output	Output for 10 MHz reference clock	5	Trigger Output*2	Output for 1/64 clock or 1/1 clock
2	10 MHz Ref Input	Input for 10 MHz reference clock	6	Jitter Ext Input*2	Input for jitter modulation signal
3	100 MHz Ref Input*2	Input for 100 MHz reference clock	7	Clock Output 1 to 4	Clock output 1 to 4
4	Ext I, Q*2	Input for I, Q signal			

*2: Only enabled when Jitter Modulation option (MU181000B-001) installed

• **MU181500B Jitter Modulation Source**



1	IQ Output	Outputs IQ signals	5	Reference Clock Output	Outputs two 1/1, 1/2, or 1/4 frequency-divided clocks based on either of following inputs: • Ext Clock Input • Aux Input
2	Ext Jitter Input	Input for modulation signal source	6	Jittered Clock Output	Outputs two jitter-modulated clock signals
3	Sub-rate Clock Output	Outputs frequency-divided clock (1/8 to 1/256) based on either of following inputs: • Ext Clock Input • Aux Input	7	Ext Clock Input	Input for external clock
4	Aux Input	Input clock signals			

Selection Guide

Category	Model Number	Model Name	28G 1ch Basic	28 Gbit/s Band High-speed Interconnects 32G 2ch + Jitter + Emphasis	Infiniband QSFP 28G 8ch + Jitter	100 GbE/ Silicon Photonics 28G 4ch	DP-QPSK 32G 4ch PPG	4PAM	8PAM
Main Frame	MP1800A	Signal Quality Analyzer	1	1	2	1	1	1	1
	MP1800A-014	2-slot for PPG and/or ED	1	1			1	1	1
	MP1800A-015	4-slot for PPG and/or ED			2*	1*			
	MP1800A-016	6-slot for PPG and/or ED							
	MP1800A-032	32 Gbit/s PPG and/or ED Support	1	1	2	1	1	1	1
Synthesizer (Sinusoidal Jitter)	MU181000A	12.5 GHz Synthesizer	1	1	1	1	1	1	1
	MU181000A-001	Jitter Modulation		1	1				
Jitter Modulator SJ (2-tone)/RJ/ BUJ	MU181500B	Jitter Modulation Source		1	1				
28G/32G PPG 1ch/2ch	MU183020A	28G/32G bit/s PPG	1	1				1	
	MU183020A-001	32G bit/s Extension		1				1	
	MU183020A-012	1ch 2 V Data Output	1*						
	MU183020A-013	1ch 3.5 V Data Output							
	MU183020A-022	2ch 2 V Data Output		1*				1*	
	MU183020A-023	2ch 3.5 V Data Output							
	MU183020A-030	1ch Data Delay							
	MU183020A-031	2ch Data Delay		1				1	
28G/32G PPG 4ch	MU183021A	28G/32G bit/s 4ch PPG			2	1	1		1
	MU183021A-001	32G bit/s Extension					1		1
	MU183021A-012	4ch 2 V Data Output			2*	1*	1*		1*
	MU183021A-013	4ch 3.5 V Data Output							
	MU183021A-030	4ch Data Delay			2	1	1		1
28G/32G ED 1ch/2ch	MU183040A/B	28G/32G bit/s ED	1	1					
	MU183040A/B-001	32G bit/s Extension							
	MU183040A/B-010	1ch ED	1	1					
	MU183040A/B-020	2ch ED							
28G/32G ED 4ch	MU183041A/B	28G/32G bit/s 4ch ED			2	1			
	MU183041A/B-001	32G bit/s Extension							
Emphasis	MP1825B	4Tap Emphasis		1					
	MP1825B-001	14 Gbit/s Operation							
	MP1825B-002	28 Gbit/s Operation		1					
	MP1825B-003	14 Gbit/s Variable Data Delay							
	MP1825B-004	28 Gbit/s Variable Data Delay							
	MP1825B-005	14.1 Gbit/s Extension							
	MP1825B-006	32.1 Gbit/s Extension		1					
Software	MX181500A	Jitter/Noise Tolerance Test Software		1	1				
PAM Signal Generation	MZ1834A	4PAM Converter						1	
	MZ1838A	8PAM Converter							1

*: Select any one

Specifications

• **MU183020A 28G/32G bit/s PPG, MU183021A 28G/32G bit/s 4ch PPG**

Bit Rate	Operational Bit-rate Range: 2.4 Gbit/s to 28.1 Gbit/s 2.4 Gbit/s to 32.1 Gbit/s (with Option-x01)
Bit-rate Setting Range (MU181000A/B synchronized operation)	<p>This item is specified when MU181000A or MU181000B is installed into the same main frame.</p> <p>When Full Rate Clock Output is selected: 2.400 000 Gbit/s to 12.500 000 Gbit/s, 0.000 001 Gbit/s step 12.500 002 Gbit/s to 25.000 000 Gbit/s, 0.000 002 Gbit/s step 25.000 004 Gbit/s to 28.100 000 Gbit/s, 0.000 004 Gbit/s step 25.000 004 Gbit/s to 32.100 000 Gbit/s, 0.000 004 Gbit/s step (with Option-x01)</p> <p>When Half Rate Clock Output is selected: 2.400 000 Gbit/s to 25.000 000 Gbit/s, 0.000 002 Gbit/s step 25.000 004 Gbit/s to 28.100 000 Gbit/s, 0.000 004 Gbit/s step 25.000 004 Gbit/s to 32.100 000 Gbit/s, 0.000 004 Gbit/s step (with Option-x01)</p>
Bit-rate Setting Range (MU181000A/B and MU181500B synchronized operation)	<p>This item is specified when MU181000A and MU181500B are installed to the same main frame.</p> <p>When Full Rate Clock Output is selected: 2.400 000 Gbit/s to 3.125 000 Gbit/s, 0.000 001 Gbit/s step 3.200 001 Gbit/s to 6.250 000 Gbit/s, 0.000 001 Gbit/s step 6.400 001 Gbit/s to 12.500 000 Gbit/s, 0.000 001 Gbit/s step 12.800 002 Gbit/s to 25.000 000 Gbit/s, 0.000 002 Gbit/s step 25.600 004 Gbit/s to 28.100 000 Gbit/s, 0.000 004 Gbit/s step 25.600 004 Gbit/s to 32.100 000 Gbit/s, 0.000 004 Gbit/s step (with Option-x01)</p> <p>When Half Rate Clock Output is selected: 2.400 000 Gbit/s to 3.125 000 Gbit/s, 0.000 002 Gbit/s step 3.200 002 Gbit/s to 6.250 000 Gbit/s, 0.000 002 Gbit/s step 6.400 002 Gbit/s to 12.500 000 Gbit/s, 0.000 002 Gbit/s step 12.800 002 Gbit/s to 25.000 000 Gbit/s, 0.000 002 Gbit/s step 25.600 004 Gbit/s to 28.100 000 Gbit/s, 0.000 004 Gbit/s step 25.600 004 Gbit/s to 32.100 000 Gbit/s, 0.000 004 Gbit/s step (with Option-x01)</p>
Bit-rate Setting Range (with external clock source)	<p>This item is specified when external clock source is used.</p> <p>When Full Rate Clock Output is selected: 2.4 Gbit/s to 16.0 Gbit/s 16.0 Gbit/s to 20.4 Gbit/s 20.0 Gbit/s to 28.1 Gbit/s 20.0 Gbit/s to 32.1 Gbit/s (with Option-x01)</p> <p>When Half Rate Clock Output is selected: 2.4 Gbit/s to 28.1 Gbit/s 2.4 Gbit/s to 32.1 Gbit/s (with Option-x01)</p>
Bit-rate Setting Range (MU181500B synchronized operation with external clock source)	<p>This item is specified when MU181000B is installed into the same mainframe and external clock source is used.</p> <p>When Full Rate Clock Output is selected: 2.4 Gbit/s to 15.0 Gbit/s 15.0 Gbit/s to 20.0 Gbit/s 20.0 Gbit/s to 28.1 Gbit/s 20.0 Gbit/s to 30.0 Gbit/s (with Option-x01) 30.0 Gbit/s to 32.1 Gbit/s (with Option-x01)</p> <p>When Half Rate Clock Output is selected: 2.4 Gbit/s to 28.1 Gbit/s 2.4 Gbit/s to 30.0 Gbit/s (with Option-x01) 30.0 Gbit/s to 32.1 Gbit/s (with Option-x01)</p>

External Clock Input	<p>Number of Input: 1 (Single end) Frequency: 1.2 GHz to 16.05 GHz Amplitude: 0.3 Vp-p to 1.0 Vp-p (–6.5 to +4.0 dBm) Termination: 50Ω/AC Coupling Connector: SMA (f.)</p>
Aux Input	<p>Number of Input: 1 (Single end) Signal Type: Error Injection, Burst Minimum Pulse Width: 1/128 Input level: 0/–1 V (H: –0.25 V to 0.05 V, L: –1.1 V to –0.8 V) Termination: 50Ω/GND Connector: SMA (f.)</p>
Aux Output	<p>Number of Output: 2 (Differential) Signal Type: 1/n Clock (n = 4, 6, 8, 10 . . . 510, 512), Pattern Sync, Burst Out2 Output level: 0/–0.6 V (H: –0.25 V to 0.05 V, L: –0.80 V to –0.45 V) Termination: 50Ω/GND Connector: SMA (f.)</p>
Gating Output	<p>Burst, Repeat Timing Signal Output level: 0/–1 V (H: –0.25 V to 0.05 V, L: –1.25 V to –0.8 V) Termination: 50Ω/GND Connector: SMA (f.)</p>
Pattern Generation	<p>PRBS Pattern length: $2^n - 1$ (n = 7, 9, 10, 11, 15, 20, 23, 31) Mark ratio: 1/2 (1/2INV is supported by a logic inversion) Zero-Substitution: Pattern with continuous 0 s appended to M-sequence signal + 1 bit Pattern: 2^n or $2^n - 1$ (n = 7, 9, 10, 11, 15, 20, 23) 0 continuous substitution count: 1 to (pattern length – 1) bits 0 at next bit after 0 substitution changed to 1 Data Data length: 2 bits to 268 435 456 bits, 1 bit step Mixed Pattern Pattern: PRBS, Data – 1 to Data – 511 Mixed Row Length (Data + PRBS Length): 1 536 to 2 415 919 104, 256 bits step Data length: 1 024 bits to 268 435 456 bits, 1 bit step PRBS length/Mark Ratio: Same as PRBS PRBS Sequence: Restart, Consecutive</p>
Pattern Sequence	<p>Repeat: Continuous Pattern Burst Burst Cycle: 25 600 bits to 2 147 483 648 bits, 256 bits step Enable period Internal: 12 800 bits to 2 147 483 392 bits, 256 bits step Ext Trigger, Enable: 12 800 bits to 2 147 483 648 bits, 256 bits step</p>
Pre-code	<p>Pre-code function: ON and OFF Type: DQPSK (MU183020A, MU183021A) DP-QPSK (MU183021A) Initial Data: 0 or 1 selectable</p>
Error addition	<p>Timing: Internal, external trigger Error event: Repeat, Single Error rate: $a \times 10^{-b}$ (a = 1 to 9, b = 3 to 12), Upper limit: 5E-3</p>

	MU183020A-x12	MU183020A-x13	MU183021A-x22	MU183021A-x23
Number of Outputs	2: Data, XData (Independent)		4: Data1, XData1, Data2, XData2 (Independent)	
Output Amplitude	0.5 Vp-p to 2.0 Vp-p 2 mV step	0.5 Vp-p to 3.5 Vp-p 2 mV step	0.5 Vp-p to 2.0 Vp-p 2 mV step	0.5 Vp-p to 3.5 Vp-p 2 mV step
	MU183021A-x12	MU183021A-x13		
Number of Outputs	8: Data, XData (Independent)			
Output Amplitude	0.5 Vp-p to 2.0 Vp-p 2 mV step	0.5 Vp-p to 3.5 Vp-p 2 mV step		
Data Output*1	<p>Output amplitude setting error: ± 50 mV $\pm 17\%$ of setting amplitude*2 Offset: -2.0 Voh to +3.3 Voh, 1 mV step Current limitation: Sourcing 50 mA, Sinking 80 mA Cross point setting range: 20 to 80%/0.1% step: at 1.0 Vp-p to upper limit of output amplitude setting 30 to 70%/0.1% step: at 0.5 Vp-p to 0.998 Vp-p Tr/Tf 12 ps (20 to 80%)*3, *4, *5 Jitter (p-p): 8 ps p-p*3, *4, *5, *6, *10 Jitter (RMS): 700 fs*3, *4, *5, *6 Waveform Distortion (0-peak): ± 25 mV $\pm 15\%$*3, *4, *5 Output: On/Off selectable Inter channel skew: ± 0.25 UI*6, *7, *8 Termination: AC/DC 50Ω Connector: K (f.)</p>			
Clock Output*9	<p>Number of output: 1 Full Rate : Clock frequency is same as bit-rate when Full Rate Clock Output is selected. 2.4 GHz to 28.1 GHz 2.4 GHz to 32.1 GHz (Option-x01) Half Rate: Clock frequency is half of bit-rate when Half Rate Clock Output is selected. 1.2 GHz to 14.05 GHz 1.2 GHz to 16.05 GHz (Option-x01) Amplitude: 0.3 Vp-p to 1.0 Vp-p Output: On/Off selectable Termination: 50Ω/AC Coupling Connector: K (f.)</p>			
Delay (MU183020A-x30, x31 MU183021A-x30)	<p>Phase variable range: -1 000 mUI to +1 000 mUI, 2 mUI step Phase setting error: ± 50 mUIp-p*5, *6 (Bit rate ≤ 28.1 Gbit/s), ± 75 mUIp-p*5, *6 (Bit rate > 28.1 Gbit/s)</p>			

*1: Unless otherwise specified, these are defined with PRBS2³¹ - 1, Mark Ratio 1/2, Cross-point 50%, using an optional accessories (J1439A coaxial cable, 0.8 m, K connector) and a sampling oscilloscope which has 70 GHz bandwidth.

*2: This value is assured when Cross point is set to 50% or within the range of 30 to 80% and Bit rate is set to 25 or 28.1 Gbit/s.

*3: Without Option-x01: at 28.1 Gbit/s

With Option-x01: at 32.1 Gbit/s

*4: With Option-x12 or x22: at amplitude 2.0 Vp-p,

With Option-x13 or x23: at amplitude 3.5 Vp-p

*5: Typical value

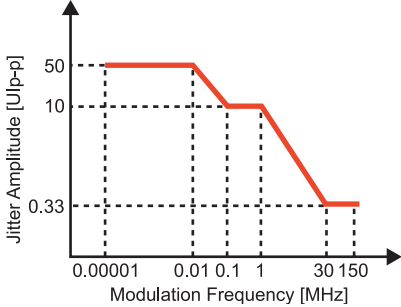
*6: Using oscilloscope with intrinsic jitter of less than 200 fs (RMS).

*7: With MU183020A-x22 or MU183020A-x23. Or, when MU183021A is used.

*8: With Option-x30 or x31.

*9: These values are monitored using an applicable part (J1439A coaxial cable, 0.8 m, K connector) at a sampling oscilloscope bandwidth of 70 GHz.

*10: This value is the peak-to-peak jitter of the crossing point on Eye pattern measured at 1k Jitter total samples and 30 counts, and is not the estimated TJ at BER 1E-12 using DR/RJ decomposition.

<p>Jitter Tolerance</p>	<p>Bit-rate: 28.1 Gbit/s 32.1 Gbit/s (Option-x01) Test Pattern: PRBS $2^{31} - 1$</p>  <p>Jitter Amplitude [UIp-p]</p> <p>Modulation Frequency [MHz]</p>
<p>Multi-Channel Operation</p>	<p>MU183020A Combination*1, *2: 2ch (Bit shifted test pattern as 56G/64 Gbit/s band signal source) CH Sync.: 2 to 4ch*3,*6 Phase variable range: -64 000 mUI to +64 000 mUI*5</p> <p>MU183021A Combination*2: 2ch (Bit shifted test pattern as 56G/64 Gbit/s band signal source) 4ch (Bit shifted test pattern as 112G/128 Gbit/s band signal source) CH Sync.: 2 to 8ch*3,*4 Phase variable range: -64 000 mUI to +64 000 mUI*5</p>
<p>Operating Temperature</p>	<p>15° to 35°C</p>

- *1: Option-x31 is required for target channels.
- *2: Combination extending over multiple slots cannot be set.
- *3: When target channels are installed successively from Slot 1.
- *4: Option-x30 is required for target channels.
- *5: A separate value can be set for each channel. This value is common to both Channel Combination and Channel Synchronization.
- *6: Option-x30 or x31 is required for target channels.

- MU183040A 28G/32G bit/s ED, MU183041A 28G/32G bit/s 4ch ED
- MU183040B 28G/32G bit/s High Sensitivity ED, MU183041B 28G/32G bit/s 4ch High Sensitivity ED

Bit-rate	Operational Bit-rate Range: 2.4 Gbit/s to 28.1 Gbit/s 2.4 Gbit/s to 32.1 Gbit/s (with Option-x01)															
Data Input	<p>Number of Input MU183040A/B-010 . . . 2 (Data , XData) MU183040A/B-020 . . . 4 (Data1 to Data2, XData1 to XData2) MU183041A/B . . . 8 (Data1 to Data4, XData1 to XData4)</p> <p>Amplifier: Single-ended 50Ω, Differential 50Ω, Differential 100Ω can be set. Data, XData can be set. Tracking, Independent, Alternate can be set. (Data-XData or XData-Data can be set when Alternate is selected.*1)</p> <p>Format: NRZ</p> <table border="1"> <thead> <tr> <th colspan="2"></th> <th>MU183040A/MU183041A</th> <th>MU183040B/MU183041B</th> </tr> </thead> <tbody> <tr> <td colspan="2">Input Amplitude*8</td> <td>0.25 Vp-p to 2.0 Vp-p</td> <td>0.05 Vp-p to 1.0 Vp-p</td> </tr> <tr> <td rowspan="2">Sensitivity*8</td> <td>Eye Amplitude</td> <td>50 mVp-p*2, *3, *4</td> <td>15 mVp-p*2, *3, *4 ≤25 mVp-p*4</td> </tr> <tr> <td>Eye Height</td> <td>–</td> <td>10 mVp-p*2, *3, *4, *9</td> </tr> </tbody> </table> <p>Note: Be careful about the maximum input amplitude. 2 Vp-p Max. for A-type, and 1 Vp-p Max. for B-type.</p> <p>Threshold voltage: –3.5 V to +3.3 V, 1 mV step (Can be set individually for Data and XData.) Absolute value of difference between Data and XData Threshold values shall be 3 V or less.</p> <p>Phase Margin: 20 ps*2, *4, *5, *7 28 ps*4, *5, *6, *7</p> <p>Termination: GND/50Ω, Variable/50Ω Termination voltage: –2.5 V to +3.5 V, 10 mV step (When termination variable is selected) Connector: K (f.)</p>			MU183040A/MU183041A	MU183040B/MU183041B	Input Amplitude*8		0.25 Vp-p to 2.0 Vp-p	0.05 Vp-p to 1.0 Vp-p	Sensitivity*8	Eye Amplitude	50 mVp-p*2, *3, *4	15 mVp-p*2, *3, *4 ≤25 mVp-p*4	Eye Height	–	10 mVp-p*2, *3, *4, *9
		MU183040A/MU183041A	MU183040B/MU183041B													
Input Amplitude*8		0.25 Vp-p to 2.0 Vp-p	0.05 Vp-p to 1.0 Vp-p													
Sensitivity*8	Eye Amplitude	50 mVp-p*2, *3, *4	15 mVp-p*2, *3, *4 ≤25 mVp-p*4													
	Eye Height	–	10 mVp-p*2, *3, *4, *9													
Clock Input	<p>Number of Input: 1 (Single-end) Frequency: 1.2 GHz to 16.05 GHz Amplitude: 0.3 Vp-p to 1.0 Vp-p (–6.5 to +4.0 dBm) Termination: 50Ω/AC Coupling Connector: SMA (f.)</p>															
Aux Input	<p>Number of Input: 1 (Single-end) Input Signal: External Mask, Burst Minimum Pulse Width: 1/128 of Bit-rate Input Level: 0/–1 V (H: –0.25 V to 0.05 V, L: –1.1 V to –0.8 V) Termination: GND/50Ω Connector: SMA (f.)</p>															
Aux Output	<p>Number of Output: 2 (Differential) Input Signal: 1/n Clock (n = 4, 6, 8, 10 . . . 510, 512), Pattern Sync, Error, Sync. gain Pattern Sync. PRBS, PRGM: Position: (Least common multiple of 1 to Pattern Length and 128) – 135, 8 step Mixed Data: Block No. setting: 1 to the Block No. specified for Mixed Data, in single steps Row No. setting: 1 to the Row No. specified for Mixed Data, in single steps Output Level: 0/–0.6 V (H: –0.25 V to 0.05 V, L: –0.80 V to –0.45 V) Termination: GND/50Ω Connector: SMA (f.)</p>															

*1: Absolute value of difference between Data and XData Threshold values shall be 1.5 V or less.

*2: 28.1 Gbit/s

*3: PRBS31, Single-ended, Mark Ratio 1/2, 20° to 30°C

*4: Typical value

*5: 0.5 Vp-p Input

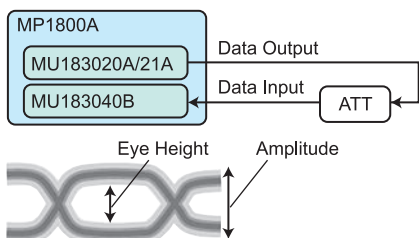
*6: 25 Gbit/s

*7: PRBS31, Single-ended, Mark ratio 1/2

*8: Input amplitude is a range where Auto Adjust function operates. Input sensitivity is the minimum input amplitude which becomes error-free.

*9: Sensitivity of eye height. Eye Height is the internal amplitude of Eye when the output amplitude of the MU183020A/21A + ATT is set to 15 mV with the measurement system as the figure below (A sampling oscilloscope with the bandwidth of 70 GHz or more is used).

The number of samples with Sampling Oscilloscope is equivalent to BER 1E–9 or less at this internal amplitude.



Pattern Detection	<p>PRBS Pattern length: $2^n - 1$ ($n = 7, 9, 10, 11, 15, 20, 23, 31$) Mark ratio: 1/2 (1/2INV is supported by a logic inversion) Zero-Substitution: Pattern with continuous 0s appended to M-sequence signal + 1 bit Pattern: 2^n or $2^n - 1$ ($n = 7, 9, 10, 11, 15, 20, 23$) 0 continuous substitution count: 1 to (pattern length - 1) bits 0 at next bit after 0 substitution changed to 1 Data Data length: 2 bits to 268 435 456 bits, 1 bit step Mixed Pattern Pattern: PRBS, Data - 1 to Data - 511 Mixed Row Length (Data + PRBS Length): 1 536 to 2 415 919 104, 256 bits step Data length: 1 024 bits to 268 435 456 bits, 1 bit step PRBS length/Mark Ratio: Same as PRBS PRBS Sequence: Restart, Consecutive</p>
Pattern Sequence	<p>Repeat: Continuous Pattern Burst Burst Cycle: 25 600 bits to 2 147 483 648 bits, 256 bits step Enable period Internal: 12 800 bits to 2 147 483 392 bits, 256 bits step Ext Trigger, Enable: 12 800 bits to 2 147 483 648 bits, 256 bits step</p>
Measurement Type	Error Rate, Error Count, Error Interval, Error Free Interval (%), Frequency Clock Count, Sync Loss Interval, Clock Loss Interval
Error Detection Mode	Total error, Insertion Error, Omission Error, Transition Error, Non Transition Error
Error Analysis	Eye Margin, Eye Diagram, Bathub Jitter, Auto Adjust, Auto Search
Burst Measurement Signal	Burst Trigger: Internal, External
Variable Clock Delay	Phase variable range: -1 000 mUI to +1 000 mUI, 2 mUI step Phase setting error: $\pm 50 \text{ mUI} \cdot p^{*1, *2}$ mUI - ps selectable
Multi-channel Operation	MU183040A/B (with Option-x20): 2ch combination ^{*3} MU183041A/B (4ch): 2ch or 4ch combination
Operating Temperature	15° to 35°C

*1: Using oscilloscope with residual jitter of less than 200 fs (RMS).

*2: Typical value

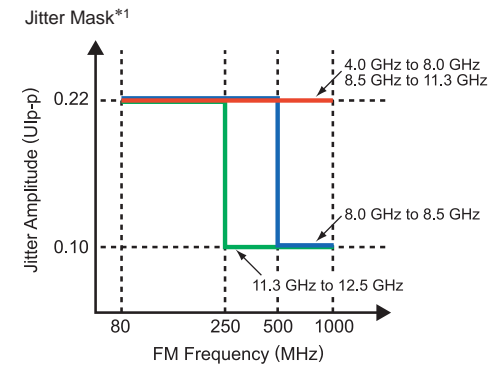
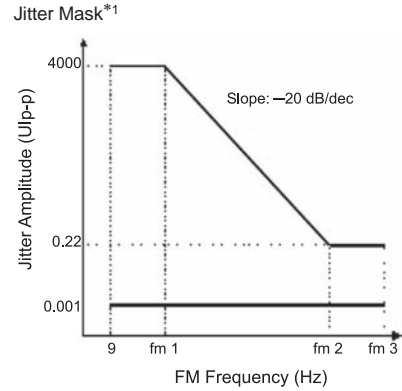
*3: Combination extending over multiple slots cannot be set.

• **MU181000A 12.5 GHz Synthesizer, MU181000B 12.5 GHz 4port Synthesizer**

<p>Clock Output</p>	<p>Number of Output: 1 [MU181000A], 4 [MU181000B] Frequency Range: 0.1 GHz to 12.5 GHz, Steps: 1 kHz/1 MHz Offset from Set Frequency: -1000 ppm to +1000 ppm, Steps: 1 ppm, 1 Hz (Min) Level: 0.632 Vp-p to 2 Vp-p (AC) [MU181000A] 0.4 Vp-p to 1 Vp-p (AC) [MU181000B, MU181000A/B-001] SSB Phase Noise: ≤ -80 dBc/Hz (10 kHz offset) Intrinsic Jitter: ≤ 20 ps p-p [MU181000A/B] ≤ 20 ps p-p (fc >400 MHz) [MU181000A/B-001] Waveform: Square wave (<1 GHz), Square wave or Sine wave (≥ 1 GHz) Duty: 50 \pm10% Inter-channel Skew: ≤ 10 ps (12.5 GHz) [MU181000B] Connector: SMA(f.), Termination: 50Ω/GND</p>
<p>10 MHz Input</p>	<p>Frequency: 10 MHz ± 10 ppm Level: 0.5 Vp-p to 2.0 Vp-p Waveform: Square wave or Sine wave Duty: 50 \pm10% Connector: BNC, Termination: 50Ω/GND</p>
<p>10 MHz Output</p>	<p>Level: 1.0 Vp-p $\pm 30\%$ (AC) Waveform: Square wave Duty: 50 \pm10% Connector: BNC, Termination: 50Ω/GND</p>

• MU181000A/B-001 Jitter Modulation

External Modulation Input	Frequency Range: 9 Hz to 1 GHz Level Range: 3 Vp-p, 0 V(dc) (Max.) Waveform: Sine wave Connector: SMA(f.), Termination: 50Ω/GND																																					
External I, Q Input	Frequency Range: DC to 320 MHz (-3 dB) Bandwidth Limit: 5 MHz (0.1 GHz <fc ≤0.4 GHz), 10 MHz (0.4 GHz <fc ≤0.65 GHz), 20 MHz (0.65 GHz <fc ≤1.4 GHz), 100 MHz (1.4 GHz <fc ≤2.4 GHz), 320 MHz (2.4 GHz <fc ≤4.0 GHz) Level Range: ±0.5 V Connector: BNC, Termination: 50Ω/GND																																					
100 MHz Reference Signal Input (SSC)	Output Center Frequency is × 25 or × 50 of Reference Input Frequency Modulation Frequency: 30 kHz to 33 kHz Frequency Deviation: 50 kHz Level: 1.0 Vp-p ±30% (AC) Waveform: Square wave or Sine wave Duty: 50 ±10% Connector: BNC, Termination: 50Ω/GND																																					
Trigger Output	Available from 800 MHz to 12.5 GHz of center frequency (fc) Frequency: 1/64 (800 MHz <fc ≤6.4 GHz), 1/1 or 1/64 selectable (6.4 GHz <fc ≤12.5 GHz) Level: 0.4 Vp-p to 1.1 Vp-p (AC) Connector: SMA(f.), Termination: 50Ω/GND																																					
Internal Jitter Function	Modulation Frequency Range <table border="1" data-bbox="432 810 911 968"> <thead> <tr> <th>Center Frequency (fc)</th> <th>fm1</th> <th>fm2</th> <th>fm3</th> </tr> </thead> <tbody> <tr> <td>0.1 GHz to 0.8 GHz</td> <td>13.75 Hz</td> <td>250 kHz</td> <td>5 MHz</td> </tr> <tr> <td>0.8 GHz to 1.6 GHz</td> <td>27.5 Hz</td> <td>500 kHz</td> <td>10 MHz</td> </tr> <tr> <td>1.6 GHz to 3.2 GHz</td> <td>55 Hz</td> <td>1 MHz</td> <td>20 MHz</td> </tr> <tr> <td>3.2 GHz to 6.4 GHz</td> <td>110 Hz</td> <td>2 MHz</td> <td>40 MHz</td> </tr> <tr> <td>6.4 GHz to 12.5 GHz</td> <td>220 Hz</td> <td>4 MHz</td> <td>80 MHz</td> </tr> </tbody> </table> <p>Modulation Frequency Accuracy: ±100 ppm Jitter Amplitude Accuracy*1: ±0.01 UI ±Q% (0.001 UIp-p to 2.19 UIp-p, fc <1 GHz) ±0.02 UI ±Q% (0.001 UIp-p to 2.19 UIp-p, fc ≥1 GHz) ±0.2 UI ±Q% (2.2 UIp-p to 21.99 UIp-p) ±2 UI ±Q% (22 UIp-p to 4000 UIp-p)</p> <table border="1" data-bbox="432 1136 703 1241"> <thead> <tr> <th>FM</th> <th>Q</th> </tr> </thead> <tbody> <tr> <td>9 Hz ≤fm ≤500 kHz</td> <td>7</td> </tr> <tr> <td>500 kHz <fm ≤2 MHz</td> <td>12</td> </tr> <tr> <td>2 MHz <fm ≤80 MHz</td> <td>15</td> </tr> </tbody> </table>	Center Frequency (fc)	fm1	fm2	fm3	0.1 GHz to 0.8 GHz	13.75 Hz	250 kHz	5 MHz	0.8 GHz to 1.6 GHz	27.5 Hz	500 kHz	10 MHz	1.6 GHz to 3.2 GHz	55 Hz	1 MHz	20 MHz	3.2 GHz to 6.4 GHz	110 Hz	2 MHz	40 MHz	6.4 GHz to 12.5 GHz	220 Hz	4 MHz	80 MHz	FM	Q	9 Hz ≤fm ≤500 kHz	7	500 kHz <fm ≤2 MHz	12	2 MHz <fm ≤80 MHz	15					
Center Frequency (fc)	fm1	fm2	fm3																																			
0.1 GHz to 0.8 GHz	13.75 Hz	250 kHz	5 MHz																																			
0.8 GHz to 1.6 GHz	27.5 Hz	500 kHz	10 MHz																																			
1.6 GHz to 3.2 GHz	55 Hz	1 MHz	20 MHz																																			
3.2 GHz to 6.4 GHz	110 Hz	2 MHz	40 MHz																																			
6.4 GHz to 12.5 GHz	220 Hz	4 MHz	80 MHz																																			
FM	Q																																					
9 Hz ≤fm ≤500 kHz	7																																					
500 kHz <fm ≤2 MHz	12																																					
2 MHz <fm ≤80 MHz	15																																					
External Jitter Function	Modulation Frequency Range: 9 Hz to 5 MHz (0.1 GHz ≤fc ≤0.4 GHz) 9 Hz to 10 MHz (0.4 GHz <fc ≤0.65 GHz) 9 Hz to 20 MHz (0.65 GHz <fc ≤1.4 GHz) 9 Hz to 100 MHz (1.4 GHz <fc ≤2.4 GHz) 9 Hz to 500 MHz (2.4 GHz <fc ≤4.0 GHz) 9 Hz to 1 GHz (4.0 GHz <fc ≤12.5 GHz) UI Range: 0.22, 2.0, 20, 200, 4000 UI Modulation Frequency Range*1 <table border="1" data-bbox="432 1493 935 1734"> <thead> <tr> <th>Center Frequency</th> <th>Input Frequency</th> <th>Jitter Amplitude</th> </tr> </thead> <tbody> <tr> <td>1.4 GHz to 2.4 GHz</td> <td>80 MHz to 100 MHz</td> <td rowspan="3">Max. 0.22 UI</td> </tr> <tr> <td>2.4 GHz to 4.0 GHz</td> <td>80 MHz to 500 MHz</td> </tr> <tr> <td>4.0 GHz to 8.0 GHz</td> <td>80 MHz to 1 GHz</td> </tr> <tr> <td rowspan="2">8.0 GHz to 8.5 GHz</td> <td>80 MHz to 500 MHz</td> <td rowspan="2">Max. 0.10 UI</td> </tr> <tr> <td>500 MHz to 1 GHz</td> </tr> <tr> <td>8.5 GHz to 11.3 GHz</td> <td>80 MHz to 1 GHz</td> <td>Max. 0.22 UI</td> </tr> <tr> <td rowspan="2">11.3 GHz to 12.5 GHz</td> <td>80 MHz to 250 MHz</td> <td rowspan="2">Max. 0.22 UI</td> </tr> <tr> <td>250 MHz to 1 GHz</td> </tr> </tbody> </table> <p>Modulation Sensitivity: 0.22 UI Range, Input level: 0.5 Vp-p</p> <table border="1" data-bbox="432 1787 1158 1913"> <thead> <tr> <th>Output Clock Frequency</th> <th>FM Frequency</th> <th>Input Frequency</th> <th>Jitter Amplitude</th> </tr> </thead> <tbody> <tr> <td rowspan="3">0.1 GHz ≤fc ≤12.5 GHz</td> <td>4 MHz</td> <td>9 Hz to 4 MHz</td> <td rowspan="3">0.1 UIp-p ±0.03 UI</td> </tr> <tr> <td>80 MHz</td> <td>4 MHz to 80 MHz</td> </tr> <tr> <td>500 MHz</td> <td>80 MHz to 500 MHz</td> </tr> <tr> <td>2.4 GHz <fc ≤12.5 GHz</td> <td>1 GHz</td> <td>500 MHz to 1 GHz</td> <td></td> </tr> </tbody> </table>	Center Frequency	Input Frequency	Jitter Amplitude	1.4 GHz to 2.4 GHz	80 MHz to 100 MHz	Max. 0.22 UI	2.4 GHz to 4.0 GHz	80 MHz to 500 MHz	4.0 GHz to 8.0 GHz	80 MHz to 1 GHz	8.0 GHz to 8.5 GHz	80 MHz to 500 MHz	Max. 0.10 UI	500 MHz to 1 GHz	8.5 GHz to 11.3 GHz	80 MHz to 1 GHz	Max. 0.22 UI	11.3 GHz to 12.5 GHz	80 MHz to 250 MHz	Max. 0.22 UI	250 MHz to 1 GHz	Output Clock Frequency	FM Frequency	Input Frequency	Jitter Amplitude	0.1 GHz ≤fc ≤12.5 GHz	4 MHz	9 Hz to 4 MHz	0.1 UIp-p ±0.03 UI	80 MHz	4 MHz to 80 MHz	500 MHz	80 MHz to 500 MHz	2.4 GHz <fc ≤12.5 GHz	1 GHz	500 MHz to 1 GHz	
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External Jitter Function	Modulation Sensitivity: 2, 20, 200, 4000 UI Range, Input level: 0.5 Vp-p Clock Frequency: 0.1 GHz $\leq f_c \leq$ 0.8 GHz																				
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Triangle Wave Modulation	PCIe-Gen I (2.5 GHz) or PCIe-Gen II (5 GHz) Clock Output Frequency Setting: Spread Method Center/Spread Method Down selectable Frequency Offset: -1000 ppm to +1000 ppm, Steps: 1 ppm Modulation Frequency Accuracy: 31.25 kHz \pm 1000 ppm Frequency Deviation: \pm 6.25 MHz (PCIe-Gen I, 2.5 GHz), \pm 12.5 MHz (PCIe-Gen II, 5 GHz) Deviation Accuracy: \pm 10%																				

*1: The maximum jitter amplitude is limited according to the jitter tolerance of PPG or ED modules. Refer to the jitter tolerance specification of PPG/ED modules.

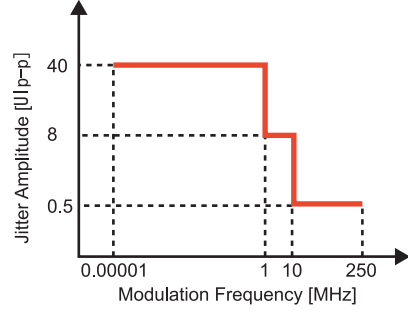
• **MU181500B Jitter Modulation Source**

External Clock Input	<p>Number of Input: 1 Frequency Range: 6.400 001 GHz to 12.500 000 GHz (MU181000A/B, Combination: On) 0.800 000 GHz to 15.000 000 GHz (MU181000A/B, Combination: Off, or External synthesizer) Amplitude: 0.4 Vp-p to 1.0 Vp-p Connector: SMA(f.), Termination: 50Ω/AC Coupling</p>
External Jitter Input	<p>Number of Input: 1 Frequency Range: 10 kHz to 1 GHz Amplitude: 0 to 2.0 Vp-p Connector: SMA(f.), Termination: 50Ω/GND</p>
Jittered Clock Output	<p>Number of Output: 2 Frequency Range: 0.800 001 GHz to 1.562 500 GHz (MU181000A/B, Combination: On), Steps: 0.000 001 GHz 1.600 001 GHz to 3.125 000 GHz (MU181000A/B, Combination: On), Steps: 0.000 001 GHz 3.200 001 GHz to 6.250 000 GHz (MU181000A/B, Combination: On), Steps: 0.000 001 GHz 6.400 001 GHz to 12.500 000 GHz (MU181000A/B, Combination: On), Steps: 0.000 001 GHz 12.800 002 GHz to 15.000 000 GHz (MU181000A/B, Combination: On), Steps: 0.000 002 GHz 0.8 GHz to 15 GHz (MU181000A/B, Combination: Off, or External synthesizer) Frequency Offset: -1000 ppm to +1000 ppm (MU181000A/B, Combination: On), Steps: 1 ppm None (MU181000A/B, Combination: Off, or External synthesizer) Amplitude: 0.4 Vp-p (Min.), 1.0 Vp-p (Max.) Intrinsic Jitter: ≤350 fs (4.25, 7.0125, 10, 12.5, 14, 15 GHz) Connector: SMA(f.), Termination: 50Ω/AC Coupling</p>
IQ Output	<p>Number of Output: 2 (I, Q) Amplitude: 1 Vp-p (Max.) Connector: SMA(f.), Termination: 50Ω/GND</p>
AUX Input	<p>Number of Input: 1 Frequency Range: Same frequency with External Clock Input Amplitude: 0.4 Vp-p (Min.), 1.1 Vp-p (Max.) Connector: SMA(f.), Termination: 50Ω/AC Coupling</p>
Reference Clock Output	<p>Number of Output: 2 Reference Clock: External Clock Input or AUX Input (MU181000A/B, Combination: On) External Clock Input (MU181000A/B, Combination: Off, or External synthesizer) Frequency Range: 1/N of Jittered Clock Output Frequency (N: 1, 2, or 4) Amplitude: 0.4 Vp-p (Min.), 1.0 Vp-p (Max.) (Jittered Clock Output Frequency: ≥4 GHz) 0.4 Vp-p (Min.), 1.2 Vp-p (Max.) (Jittered Clock Output Frequency: <4 GHz) Connector: SMA(f.), Termination: 50Ω/AC Coupling</p>
Sub-rate Clock Output	<p>Number of Output: 2 (Differential) Frequency Range: 1/N of Jittered Clock Output Frequency (N: 8 to 256, Steps: 1) Amplitude: 0.1 Vp-p to 0.7 Vp-p, Steps: 10 mV Accuracy: ±70 mV ±20% of Amplitude (N: 8) Connector: SMA(f.), Termination: 50Ω/AC Coupling</p>

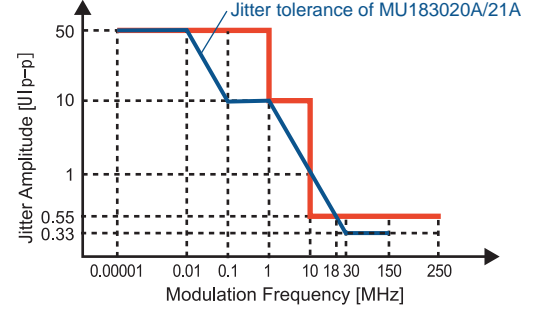
Internal Sinusoidal Jitter (SJ1)

Mask*1

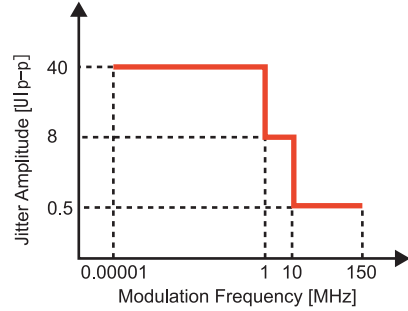
Jittered Clock Output Frequency: 8.500 001 GHz to 15 GHz
Full Rate Mode*2



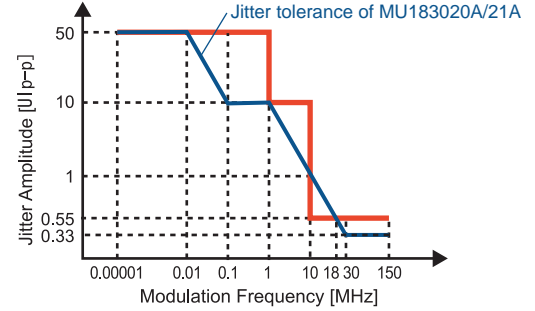
Half Rate Mode*2



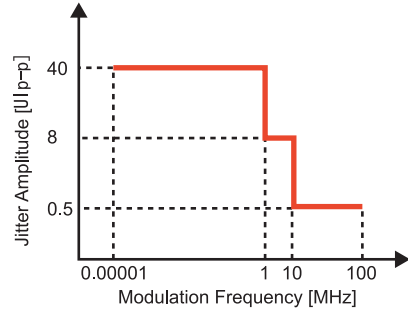
Jittered Clock Output Frequency: 4.000 001 GHz to 8.5 GHz
Full Rate Mode*2



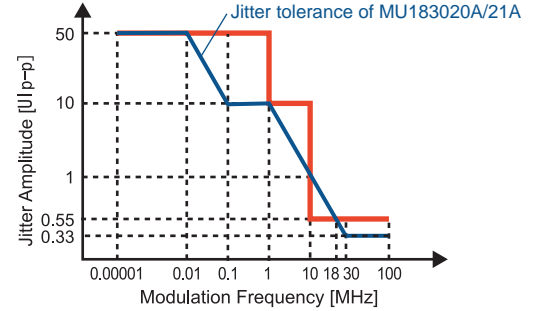
Half Rate Mode*2



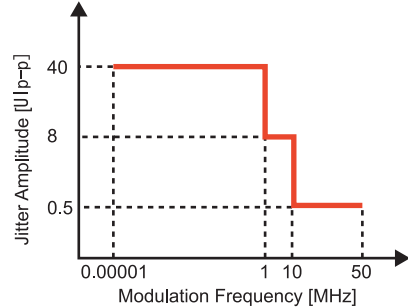
Jittered Clock Output Frequency: 1.200 001 GHz to 4 GHz
Full Rate Mode*2



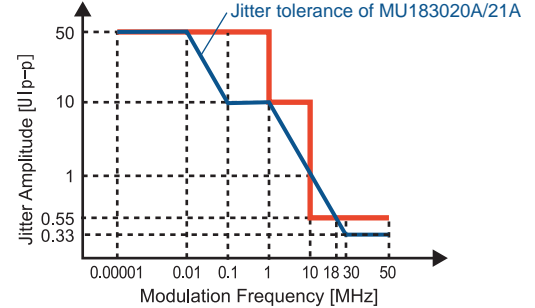
Half Rate Mode*2



Jittered Clock Output Frequency: 0.800 001 GHz to 1.2 GHz
Full Rate Mode*2



Half Rate Mode*2



Internal Sinusoidal Jitter (SJ1)

Modulation Frequency (FM): 10 Hz to 10 kHz, Steps: 1 Hz
 10 kHz to 100 kHz, Steps: 10 Hz
 100 kHz to 1 MHz, Steps: 100 Hz
 1 MHz to 10 MHz, Steps: 1 kHz
 10 MHz to 100 MHz, Steps: 10 kHz
 100 MHz to 250 MHz, Steps: 100 kHz

Accuracy: ± 100 ppm

Amplitude*1:

Full Rate Mode*2

Jittered Clock Output Frequency: 8.500 001 GHz to 15 GHz
 0 to 40 Ulp-p (FM: 10 Hz to 1 MHz), Steps: 0.1 UI
 0 to 8 Ulp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.01 UI
 0 to 0.5 Ulp-p (FM: 10.01 MHz to 250 MHz), Steps: 0.001 UI

Jittered Clock Output Frequency: 4.000 001 GHz to 8.5 GHz
 0 to 40 Ulp-p (FM: 10 Hz to 1 MHz), Steps: 0.1 UI
 0 to 8 Ulp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.01 UI
 0 to 0.5 Ulp-p (FM: 10.01 MHz to 150 MHz), Steps: 0.001 UI

Jittered Clock Output Frequency: 1.200 001 GHz to 4 GHz
 0 to 40 Ulp-p (FM: 10 Hz to 1 MHz), Steps: 0.1 UI
 0 to 8 Ulp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.01 UI
 0 to 0.5 Ulp-p (FM: 10.01 MHz to 100 MHz), Steps: 0.001 UI

Jittered Clock Output Frequency: 1.800 001 GHz to 1.2 GHz
 0 to 40 Ulp-p (FM: 10 Hz to 1 MHz), Steps: 0.1 UI
 0 to 8 Ulp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.01 UI
 0 to 0.5 Ulp-p (FM: 10.01 MHz to 50 MHz), Steps: 0.001 UI

Half Rate Mode*2

Jittered Clock Output Frequency: 8.500 001 GHz to 15 GHz
 0 to 50 Ulp-p (FM: 10 Hz to 1 MHz), Steps: 0.2 UI
 0 to 10 Ulp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.02 UI
 0 to 0.55 Ulp-p (FM: 10.01 MHz to 250 MHz), Steps: 0.002 UI

Jittered Clock Output Frequency: 4.000 001 GHz to 8.5 GHz
 0 to 50 Ulp-p (FM: 10 Hz to 1 MHz), Steps: 0.2 UI
 0 to 10 Ulp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.02 UI
 0 to 0.55 Ulp-p (FM: 10.01 MHz to 150 MHz), Steps: 0.002 UI

Jittered Clock Output Frequency: 1.200 001 GHz to 4 GHz
 0 to 50 Ulp-p (FM: 10 Hz to 1 MHz), Steps: 0.2 UI
 0 to 10 Ulp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.02 UI
 0 to 0.55 Ulp-p (FM: 10.01 MHz to 100 MHz), Steps: 0.002 UI

Jittered Clock Output Frequency: 1.800 001 GHz to 1.2 GHz
 0 to 50 Ulp-p (FM: 10 Hz to 1 MHz), Steps: 0.2 UI
 0 to 10 Ulp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.02 UI
 0 to 0.55 Ulp-p (FM: 10.01 MHz to 50 MHz), Steps: 0.002 UI

Accuracy: ± 0.03 UI $\pm Q\%$ (Amplitude: 0.002 Ulp-p to 2.19 Ulp-p)
 ± 0.2 UI $\pm Q\%$ (Amplitude: 2.2 Ulp-p to 21.9 Ulp-p)
 ± 2 UI $\pm Q\%$ (Amplitude: 22 Ulp-p to 50 Ulp-p)

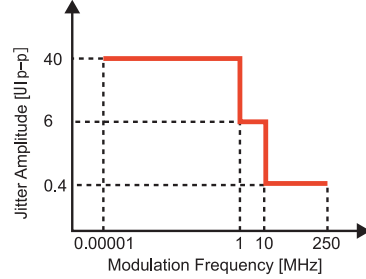
FM	Q
10 Hz \leq fm \leq 500 kHz	7
500 kHz $<$ fm \leq 2 MHz	10
2 MHz $<$ fm \leq 80 MHz	13
80 MHz $<$ fm \leq 250 MHz	15

On/Off Function: Supported

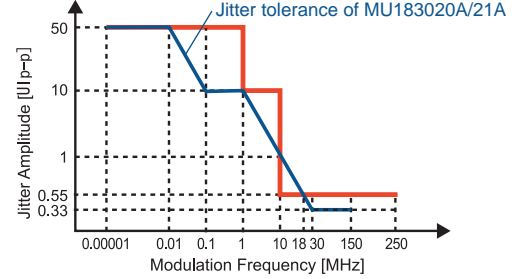
External Sinusoidal Jitter (SJ2)
[MU181000A/B-001]

Mask*1

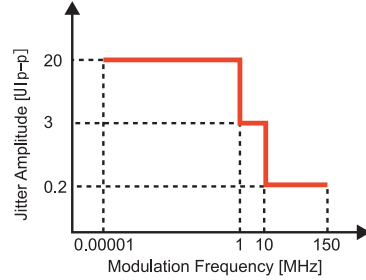
Jittered Clock Output Frequency: 6.400 001 GHz to 15 GHz
Full Rate Mode*2



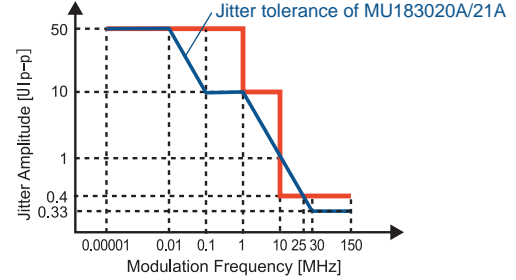
Half Rate Mode*2



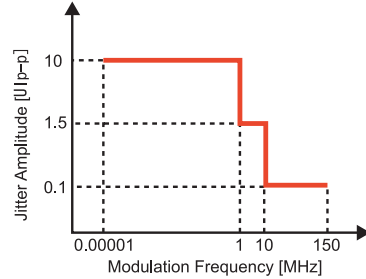
Jittered Clock Output Frequency: 3.200 001 GHz to 6.25 GHz
Full Rate Mode*2



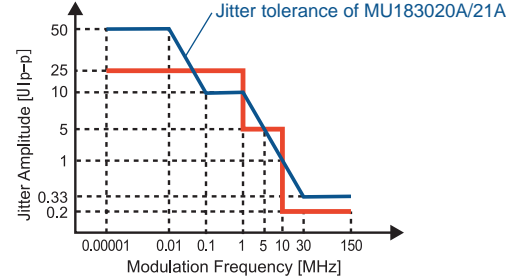
Half Rate Mode*2



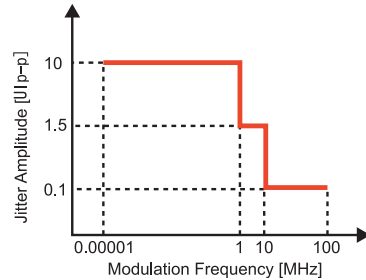
Jittered Clock Output Frequency: 1.800 001 GHz to 3.125 GHz
Full Rate Mode*2



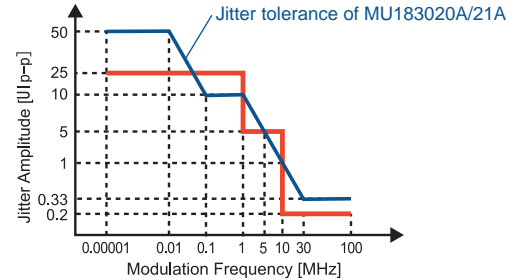
Half Rate Mode*2



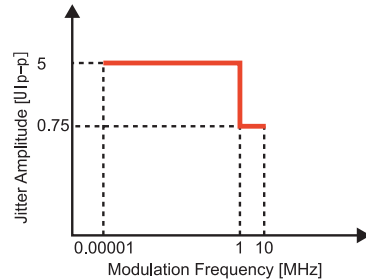
Jittered Clock Output Frequency: 1.600 001 GHz to 1.8 GHz
Full Rate Mode*2



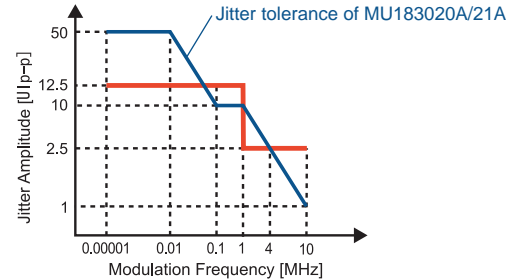
Half Rate Mode*2



Jittered Clock Output Frequency: 0.800 001 GHz to 1.562 5 GHz
Full Rate Mode*2



Half Rate Mode*2



External Sinusoidal Jitter (SJ2)
[MU181000A/B-001]

Modulation Frequency (FM): 10 Hz to 10 kHz, Steps: 1 Hz
 10 kHz to 100 kHz, Steps: 10 Hz
 100 kHz to 1 MHz, Steps: 100 Hz
 1 MHz to 10 MHz, Steps: 1 kHz
 10 MHz to 100 MHz, Steps: 10 kHz
 100 MHz to 250 MHz, Steps: 100 kHz

Accuracy: ± 100 ppm

Amplitude*1:

Full Rate Mode*2

Jittered Clock Output Frequency: 6.400 001 GHz to 15 GHz
 0 to 40 Ulp-p (FM: 10 Hz to 1 MHz), Steps: 0.1 UI
 0 to 6 Ulp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.01 UI
 0 to 0.4 Ulp-p (FM: 10.01 MHz to 250 MHz), Steps: 0.001 UI

Jittered Clock Output Frequency: 3.200 001 GHz to 6.25 GHz
 0 to 20 Ulp-p (FM: 10 Hz to 1 MHz), Steps: 0.1 UI
 0 to 3 Ulp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.01 UI
 0 to 0.2 Ulp-p (FM: 10.01 MHz to 150 MHz), Steps: 0.001 UI

Jittered Clock Output Frequency: 1.800 001 GHz to 3.125 GHz
 0 to 10 Ulp-p (FM: 10 Hz to 1 MHz), Steps: 0.1 UI
 0 to 1.5 Ulp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.01 UI
 0 to 0.1 Ulp-p (FM: 10.01 MHz to 150 MHz), Steps: 0.001 UI

Jittered Clock Output Frequency: 1.600 001 GHz to 1.8 GHz
 0 to 10 Ulp-p (FM: 10 Hz to 1 MHz), Steps: 0.1 UI
 0 to 1.5 Ulp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.01 UI
 0 to 0.1 Ulp-p (FM: 10.01 MHz to 100 MHz), Steps: 0.001 UI

Jittered Clock Output Frequency: 0.800 001 GHz to 1.562 5 GHz
 0 to 5 Ulp-p (FM: 10 Hz to 1 MHz), Steps: 0.1 UI
 0 to 0.75 Ulp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.01 UI

Half Rate Mode*2

Jittered Clock Output Frequency: 6.400 001 GHz to 15 GHz
 0 to 50 Ulp-p (FM: 10 Hz to 1 MHz), Steps: 0.2 UI
 0 to 10 Ulp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.02 UI
 0 to 0.55 Ulp-p (FM: 10.01 MHz to 250 MHz), Steps: 0.002 UI

Jittered Clock Output Frequency: 3.200 001 GHz to 6.25 GHz
 0 to 50 Ulp-p (FM: 10 Hz to 1 MHz), Steps: 0.2 UI
 0 to 10 Ulp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.02 UI
 0 to 0.4 Ulp-p (FM: 10.01 MHz to 150 MHz), Steps: 0.002 UI

Jittered Clock Output Frequency: 1.800 001 GHz to 3.125 GHz
 0 to 25 Ulp-p (FM: 10 Hz to 1 MHz), Steps: 0.2 UI
 0 to 5 Ulp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.02 UI
 0 to 0.2 Ulp-p (FM: 10.01 MHz to 150 MHz), Steps: 0.002 UI

Jittered Clock Output Frequency: 1.600 001 GHz to 1.8 GHz
 0 to 25 Ulp-p (FM: 10 Hz to 1 MHz), Steps: 0.2 UI
 0 to 5 Ulp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.02 UI
 0 to 0.2 Ulp-p (FM: 10.01 MHz to 100 MHz), Steps: 0.002 UI

Jittered Clock Output Frequency: 0.800 001 GHz to 1.562 5 GHz
 0 to 12.5 Ulp-p (FM: 10 Hz to 1 MHz), Steps: 0.2 UI
 0 to 2.5 Ulp-p (FM: 1.001 MHz to 10 MHz), Steps: 0.02 UI

Accuracy: ± 0.03 UI $\pm Q\%$ (Amplitude: 0.002 Ulp-p to 2.19 Ulp-p)

± 0.2 UI $\pm Q\%$ (Amplitude: 2.2 Ulp-p to 21.9 Ulp-p)

± 2 UI $\pm Q\%$ (Amplitude: 22 Ulp-p to 50 Ulp-p)

FM	Q
10 Hz \leq fm \leq 500 kHz	10
500 kHz $<$ fm \leq 2 MHz	13
2 MHz $<$ fm \leq 80 MHz	15
80 MHz $<$ fm \leq 250 MHz	18

On/Off Function: Supported

Spread Spectrum Clocking (SSC)

Type: Down-Spread, Center-Spread, Up-Spread
 Modulation Frequency: 28 kHz to 34 kHz, Steps: 1 Hz
 Accuracy: ± 100 ppm
 Deviation: 0 to 5000 ppm, Steps: 1 ppm
 On/Off Function: Supported

<p>Random Jitter (RJ)</p>	<p>Bandwidth: 10 kHz to 1 GHz Crest Factor: 16 dB</p> <p>Filter Type User Filter Filter: 10 MHz, 20 MHz, Through (HPF 3 dB bandwidth) 100 MHz, Through (LPF 3 dB bandwidth)</p> <p>Amplitude*¹ Full Rate Mode*²</p> <table border="1" data-bbox="477 474 1123 554"> <thead> <tr> <th>Jittered Clock Output Frequency [GHz]</th> <th>Setting Range [UIp-p]</th> <th>Steps [mUI]</th> </tr> </thead> <tbody> <tr> <td>≥2.5</td> <td>0 to 0.5</td> <td>2</td> </tr> <tr> <td><2.5</td> <td>0 to 0.2f</td> <td>2</td> </tr> </tbody> </table> <p>Half Rate Mode*³</p> <table border="1" data-bbox="477 585 1123 665"> <thead> <tr> <th>Jittered Clock Output Frequency [GHz]</th> <th>Setting Range [UIp-p]</th> <th>Steps [mUI]</th> </tr> </thead> <tbody> <tr> <td>≥2.5</td> <td>0 to 0.5</td> <td>4</td> </tr> <tr> <td><2.5</td> <td>0 to 0.2f</td> <td>4</td> </tr> </tbody> </table> <p>f: Jittered Clock Output Frequency [GHz] Accuracy: ±4.9 ps ±15% (Jittered Clock Output Frequency: ≥4 GHz) ±7.0 ps ±15% (Jittered Clock Output Frequency: <4 GHz)</p> <p>PCIe (Data clocked) or PCIe (Common Ref. clock) Filter Filter: LF (10 kHz to 1.5 MHz) or HF (1.5 MHz to 100 MHz) for PCIe</p> <p>Amplitude*¹ Full Rate Mode*²</p> <table border="1" data-bbox="477 854 1222 909"> <thead> <tr> <th>Jittered Clock Output Frequency [GHz]</th> <th>LF and HF Setting Range [ps rms]</th> <th>Steps [ps rms]</th> </tr> </thead> <tbody> <tr> <td>>4</td> <td>0 to 8.8</td> <td>0.1</td> </tr> </tbody> </table> <p>Half Rate Mode*²</p> <table border="1" data-bbox="477 940 1222 995"> <thead> <tr> <th>Jittered Clock Output Frequency [GHz]</th> <th>LF and HF Setting Range [ps rms]</th> <th>Steps [ps rms]</th> </tr> </thead> <tbody> <tr> <td>>4</td> <td>0 to 8.8</td> <td>0.2</td> </tr> </tbody> </table> <p>LF Amplitude ≥ HF Amplitude Accuracy: ±0.6 ps ±10% On/Off Function: Supported</p>	Jittered Clock Output Frequency [GHz]	Setting Range [UIp-p]	Steps [mUI]	≥2.5	0 to 0.5	2	<2.5	0 to 0.2f	2	Jittered Clock Output Frequency [GHz]	Setting Range [UIp-p]	Steps [mUI]	≥2.5	0 to 0.5	4	<2.5	0 to 0.2f	4	Jittered Clock Output Frequency [GHz]	LF and HF Setting Range [ps rms]	Steps [ps rms]	>4	0 to 8.8	0.1	Jittered Clock Output Frequency [GHz]	LF and HF Setting Range [ps rms]	Steps [ps rms]	>4	0 to 8.8	0.2
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<p>Bounded Uncorrelated Jitter (BUJ)</p>	<p>PRBS Pattern Length: $2^n - 1$ (n = 7, 9, 11, 15, 23, or 31) BUJ Rate: 0.1 Gbit/s to 3.2 Gbit/s, Steps: 1 kbit/s 4.9 Gbit/s to 6.25 Gbit/s, Steps: 1 kbit/s (Jittered Clock Output Frequency: >4 GHz) 9.8 Gbit/s to 12.5 Gbit/s, Steps: 1 kbit/s (Jittered Clock Output Frequency: >4 GHz)</p> <p>Filter Type (LPF 3 dB Bandwidth): 50, 100, 200, 300, 500 MHz, Through (Jittered Clock Output Frequency: >4 GHz) 50, 100, 200, 300 MHz, Through (Jittered Clock Output Frequency: ≤4 GHz)</p> <p>Amplitude*¹: Full Rate Mode*²</p> <table border="1" data-bbox="445 1272 1086 1352"> <thead> <tr> <th>Jittered Clock Output Frequency [GHz]</th> <th>Setting Range [UIp-p]</th> <th>Steps [mUI]</th> </tr> </thead> <tbody> <tr> <td>≥2.5</td> <td>0 to 0.5</td> <td>2</td> </tr> <tr> <td><2.5</td> <td>0 to 0.2f</td> <td>2</td> </tr> </tbody> </table> <p>Half Rate Mode*²</p> <table border="1" data-bbox="445 1383 1086 1463"> <thead> <tr> <th>Jittered Clock Output Frequency [GHz]</th> <th>Setting Range [UIp-p]</th> <th>Steps [mUI]</th> </tr> </thead> <tbody> <tr> <td>≥2.5</td> <td>0 to 0.5</td> <td>4</td> </tr> <tr> <td><2.5</td> <td>0 to 0.2f</td> <td>4</td> </tr> </tbody> </table> <p>f: Jittered Clock Output Frequency [GHz] Accuracy: ±4.9 ps ±15% (Jittered Clock Output Frequency: ≥4 GHz) ±7.0 ps ±15% (Jittered Clock Output Frequency: <4 GHz)</p> <p>PRBS Pattern Length: $2^n - 1$ (n = 7, 9) BUJ Rate: 6, 5.5, 4.9 Gbit/s, LPF 500 MHz BUJ Rate: 3.2 Gbit/s, 3 Gbit/s, LPF 300 MHz BUJ Rate: 3.2 Gbit/s, 2 Gbit/s, LPF 200 MHz BUJ Rate: 2 Gbit/s, 1.1 Gbit/s, LPF 100 MHz On/Off Function: Supported</p>	Jittered Clock Output Frequency [GHz]	Setting Range [UIp-p]	Steps [mUI]	≥2.5	0 to 0.5	2	<2.5	0 to 0.2f	2	Jittered Clock Output Frequency [GHz]	Setting Range [UIp-p]	Steps [mUI]	≥2.5	0 to 0.5	4	<2.5	0 to 0.2f	4												
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<p>External Jitter</p>	<p>Bandwidth: 10 kHz to 1 GHz Accuracy*³: 0.5 UI ±10% (2 Vp-p) Linearity*³: ±6 ps ±10% On/Off Function: Supported</p>																														

*1: The maximum jitter amplitude is limited according to the jitter tolerance of PPG or ED modules. Refer to the jitter tolerance specification of PPG/ED modules.

*2: Full Rate Mode: MU181020A/B PPG or MU182020A/21A MUX as a Full Rate

Half Rate Mode: MU182020A/21A MUX as a Half Rate

*3: Jittered Clock Output Frequency: Specified as 5 GHz, Modulation Frequency: 0.5 GHz, Sinusoidal Jitter

• **MP1825B 4Tap Emphasis**

Bit Rate	<p>1 Gbit/s to 14.05 Gbit/s [MP1825B-001] 1 Gbit/s to 14.1 Gbit/s [MP1825B-001, 005] 1 Gbit/s to 28.1 Gbit/s [MP1825B-002, when not using Doubler Input/Output] 1 Gbit/s to 32.1 Gbit/s [MP1825B-002, 006, when not using Doubler Input/Output] 8 Gbit/s to 28.1 Gbit/s [MP1825B-002, when using Doubler Input/Output]</p>
Data Output*1	<p>Number of Output: 2 (Data/xData) Emphasis Setting: a) 2post-cursor, 1pre-cursor b) 3post-cursor c) 1post-cursor, 1pre-cursor d) 2post-cursor e) 1post-cursor f) Rev. 3post-cursor Peak Voltage: 100 mVp-p to 1.5 Vp-p (Single-ended) Eye Amplitude: 100 mVp-p to 1.0 Vp-p (Single-ended), Steps: 2 mVp-p Offset: -1.0 Vth to +1.0 Vth, Steps: 1 mV Total Jitter*2: 8 ps p-p (typ.) Tr/Tf*3: 20 ps (typ.), ≤25 ps (20 to 80%) [MP1825B-001] 12 ps (typ.), ≤16 ps (20 to 80%) [MP1825B-002] Cursor1 Emphasis: -20 to +20 dB, 20log (Eye Amplitude/Cursor1), Steps: 0.1 dB Cursor2 Emphasis: -20 to +20 dB, 20log (Eye Amplitude/Cursor2), Steps: 0.1 dB Cursor3 Emphasis: -20 to +20 dB, 20log (Eye Amplitude/Cursor3), Steps: 0.1 dB On/Off Function: Supported Connector: K (f.), Termination: 50 Ω/AC Coupling</p>
Data Input	<p>Amplitude: 0.4 Vp-p to 1.2 Vp-p Connector: SMA (f.) [MP1825B-001], K (f.) [MP1825B-002], Termination: 50 Ω/GND</p>
Clock Input	<p>Frequency Range: 1 GHz to 14.05 GHz [MP1825B-001] 1 GHz to 14.1 GHz [MP1825B-001, 005] 1 GHz to 28.1 GHz [MP1825B-002] 1 GHz to 32.1 GHz [MP1825B-002, 006] Amplitude: 0.25 Vp-p to 1.0 Vp-p Connector: SMA (f.) [MP1825B-001], K (f.) [MP1825B-002], Termination: 50 Ω/AC Coupling</p>
Clock Buffer Output	<p>Frequency Range: 1 GHz to 14.05 GHz [MP1825B-001] 1 GHz to 14.1 GHz [MP1825B-001, 005] 4 GHz to 14.05 GHz [MP1825B-002] Amplitude: 0.4 Vp-p (Min.), 1.0 Vp-p (Max.) (Fixed) Connector: SMA (f.), Termination: 50 Ω/AC Coupling</p>
Doubler Input [MP1825B-002]	<p>Frequency Range: 4 GHz to 14.05 GHz Amplitude: 0.25 Vp-p to 1.2 Vp-p Connector: SMA (f.), Termination: 50 Ω/AC Coupling</p>
Doubler Output [MP1825B-002]	<p>Amplitude: 0.4 Vp-p (Min.), 1.0 Vp-p (Max.) (Fixed) Connector: K (f.), Termination: 50 Ω/AC Coupling</p>
Variable Data Delay [MP1825B-003 or MP1825B-004]	<p>Phase Variable Range: -1000 mUI to +1000 mUI Accuracy: 50 mUIp-p (typ.)</p>
General Specification	<p>Channel Switch: CH1/CH2 (Rear panel switch) Operation Interface: USB 2.0 or 1.1 Type B Power Supply: 100 V(ac) to 240 V(ac), 50 Hz/60 Hz Power Consumption: <100 W Dimensions: 120 (W) × 90.9 (H) × 140 (D) mm Mass: <5 kg Operating Temperature: 15° to 35°C EMC: EN61326-1, EN61000-3-2 LVD: EN61010-1</p>

*1: Measured at PRBS 2³¹ - 1, Mark Ratio 1/2 with 50 GHz sampling oscilloscope

*2: Measured at 14.05 Gbit/s or 28.1 Gbit/s (with MP1825B-002) with the sampling oscilloscope, intrinsic jitter should be less than 200 fs (rms)

*3: Emphasis Function: Off

Ordering Information

Please specify the model/order number, name and quantity when ordering.
The names listed in the chart below are Order Names. The actual name of the item may differ from the Order Name.

• MU183020A

Model/Order No.	Name
Unit/Module	
MU183020A	28G/32G bit/s PPG
Standard Accessories	
J1137	Terminator: 3 pcs
J1359A	Coaxial Adaptor (K-P, K-J, SMA): 1 pc
J1341A	Open: 1 pc
J1451A	Coaxial Attenuator (6 dB): 1 pc
Z0897A	MP1800A Manual CD: 1 pc
Z0918A	MX180000A Software CD: 1 pc
Options	
MU183020A-001	32G bit/s Extension
MU183020A-012	1ch 2 V Data Output
MU183020A-013	1ch 3.5 V Data Output
MU183020A-022	2ch 2 V Data Output
MU183020A-023	2ch 3.5 V Data Output
MU183020A-030	1ch Data Delay
MU183020A-031	2ch Data Delay
Retrofit Options	
MU183020A-101	32G bit/s Extension Retrofit
MU183020A-112	1ch 2 V Data Output Retrofit
MU183020A-113	1ch 3.5 V Data Output Retrofit
MU183020A-122	2ch 2 V Data Output Retrofit
MU183020A-123	2ch 3.5 V Data Output Retrofit
MU183020A-130	1ch Data Delay Retrofit
MU183020A-131	2ch Data Delay Retrofit
Standard Accessories for MU183020A-x12, x13	
J1137	Terminator: 2 pcs
J1359A	Coaxial Adaptor (K-P, K-J, SMA): 2 pcs
Standard Accessories for MU183020A-x22, x23	
J1137	Terminator: 4 pcs
J1359A	Coaxial Adaptor (K-P, K-J, SMA): 4 pcs
Maintenance Service	
MU183020A-ES310	Three Years Extended Warranty Service
MU183020A-ES510	Five Years Extended Warranty Service

• MU183040A

Model/Order No.	Name
Unit/Module	
MU183040A	28G/32G bit/s ED
Standard Accessories	
J1137	Terminator: 2 pcs
J1341A	Open: 1 pc
Z0897A	MP1800A Manual CD: 1 pc
Z0918A	MX180000A Software CD: 1 pc
Options	
MU183040A-001	32G bit/s Extension
MU183040A-010	1ch ED
MU183040A-020	2ch ED
Retrofit Options	
MU183040A-101	32G bit/s Extension Retrofit
MU183040A-120	2ch ED Retrofit
Standard Accessories for MU183040A-x10	
J1341A	Open: 2 pcs
J1359A	Coaxial Adaptor (K-P, K-J, SMA): 2 pcs
Standard Accessories for MU183040A-x20	
J1341A	Open: 4 pcs
J1359A	Coaxial Adaptor (K-P, K-J, SMA): 4 pcs
Maintenance Service	
MU183040A-ES310	Three Years Extended Warranty Service
MU183040A-ES510	Five Years Extended Warranty Service

• MU183040B

Model/Order No.	Name
Unit/Module	
MU183040B	28G/32G bit/s High Sensitivity ED
Standard Accessories	
J1137	Terminator: 2 pcs
J1341A	Open: 1 pc
Z0897A	MP1800A Manual CD: 1 pc
Z0918A	MX180000A Software CD: 1 pc
Options	
MU183040B-001	32 Gbit/s Extension
MU183040B-010	1ch ED
MU183040B-020	2ch ED
Retrofit Options	
MU183040B-101	32 Gbit/s Extension Retrofit
MU183040B-110	1ch ED Retrofit
MU183040B-120	2ch ED Retrofit
Standard Accessories for MU183040B-x10	
J1341A	Open: 2 pcs
J1359A	Coaxial Adaptor (K-P, K-J, SMA): 2 pcs
J1451A	Coaxial Attenuator (6 dB): 2 pcs
Standard Accessories for MU183040B-x20	
J1341A	Open: 4 pcs
J1359A	Coaxial Adaptor (K-P, K-J, SMA): 4 pcs
J1451A	Coaxial Attenuator (6 dB): 4 pcs
Maintenance Service	
MU183040B-ES310	Three Years Extended Warranty Service
MU183040B-ES510	Five Years Extended Warranty Service

• MU183021A

Model/Order No.	Name
Unit/Module	
MU183021A	28G/32G bit/s 4ch PPG
Standard Accessories	
J1137	Terminator: 3 pcs
J1359A	Coaxial Adaptor (K-P, K-J, SMA): 1 pc
J1341A	Open: 1 pc
J1451A	Coaxial Attenuator (6 dB): 1 pc
Z0897A	MP1800A Manual CD: 1 pc
Z0918A	MX180000A Software CD: 1 pc
Options	
MU183021A-001	32G bit/s Extension
MU183021A-012	4ch 2.0 V Data Output
MU183021A-013	4ch 3.5 V Data Output
MU183021A-030	4ch Data Delay
Retrofit Options	
MU183021A-101	32G bit/s Extension Retrofit
MU183021A-112	4ch 2.0 V Data Output Retrofit
MU183021A-113	4ch 3.5 V Data Output Retrofit
MU183021A-130	4ch Data Delay Retrofit
Standard Accessories for MU183021A-x12, x13	
J1137	Terminator: 8 pcs
J1359A	Coaxial Adaptor (K-P, K-J, SMA): 8 pcs
Maintenance Service	
MU183021A-ES310	Three Years Extended Warranty Service
MU183021A-ES510	Five Years Extended Warranty Service

• **MU183041A**

Model/Order No.	Name
Unit/Module	
MU183041A	28G/32G bit/s 4ch ED
Standard Accessories	
J1137	Terminator: 2 pcs
J1341A	Open: 9 pcs
J1359A	Coaxial Adaptor (K-P, K-J, SMA): 8 pcs
Z0897A	MP1800A Manual CD: 1 pc
Z0918A	MX180000A Software CD: 1 pc
Options	
MU183041A-001	32G bit/s Extension
Retrofit Options	
MU183041A-101	32G bit/s Extension Retrofit
Maintenance Service	
MU183041A-ES310	Three Years Extended Warranty Service
MU183041A-ES510	Five Years Extended Warranty Service

• **MU183041B**

Model/Order No.	Name
Unit/Module	
MU183041B	28G/32G bit/s 4ch High Sensitivity ED
Standard Accessories	
J1137	Terminator: 3 pcs
J1341A	Open: 9 pcs
J1359A	Coaxial Adaptor (K-P, K-J, SMA): 8 pcs
J1451A	Coaxial Attenuator (6 dB): 8 pcs
Z0897A	MP1800A Manual CD: 1 pc
Z0918A	MX180000A Software CD: 1 pc
Options	
MU183041B-001	32 Gbit/s Extension
Retrofit Options	
MU183041B-101	32 Gbit/s Extension Retrofit
Maintenance Service	
MU183041B-ES310	Three Years Extended Warranty Service
MU183041B-ES510	Five Years Extended Warranty Service

• **Optional Accessories**

Model/Order No.	Name	Remarks
J1449A	Measurement Kit	J1439A: 2 pcs, J1342A: 2 pcs, J1343A: 1 pc
J1343A	Coaxial Cable 1 m	SMA, DC to 18 GHz
J1342A	Coaxial Cable 0.8 m	APC3.5, DC to 27.5 GHz
J1439A	Coaxial Cable (0.8 m, K connector)	K, DC to 40 GHz
J1550A	Coaxial Skew Match Cable (0.8 m, APC3.5)	APC3.5, DC to 27.5 GHz, Skew < 3 ps
J1551A	Coaxial Skew Match Cable (0.8 m, K)	K, DC to 40 GHz, Skew < 3 ps
Z0306A	Wrist Strap	
J1137	Coaxial Terminator	
J1359A	Coaxial Adaptor (K-P, K-J, SMA)	
W3594AE	MU183020A/MU183021A Operation Manual	Printed version
W3595AE	MU183040A/MU183041A/ MU183040B/MU183041B Operation Manual	Printed version
J1450A	Coaxial Attenuator (3 dB)	41KC-3
J1451A	Coaxial Attenuator (6 dB)	41KC-6
J1452A	Coaxial Attenuator (10 dB)	41KC-10
J1453A	Coaxial Attenuator (20 dB)	41KC-20

• **MZ1834A**

Model/Order No.	Name
Main Frame	
MZ1834A	4PAM Converter
Standard Accessories	
J1359A	Coaxial Adaptor (K-P, K-J, SMA): 2 pcs
Z0897A	MP1800A Manual CD: 1 pc

• **MZ1838A**

Model/Order No.	Name
Main Frame	
MZ1838A	8PAM Converter
Standard Accessories	
J1359A	Coaxial Adaptor (K-P, K-J, SMA): 2 pcs
Z0897A	MP1800A Manual CD: 1 pc



Note:



Note:

● **United States**

Anritsu Company

1155 East Collins Blvd., Suite 100, Richardson,
TX 75081, U.S.A.
Toll Free: 1-800-267-4878
Phone: +1-972-644-1777
Fax: +1-972-671-1877

● **Canada**

Anritsu Electronics Ltd.

700 Silver Seven Road, Suite 120, Kanata,
Ontario K2V 1C3, Canada
Phone: +1-613-591-2003
Fax: +1-613-591-1006

● **Brazil**

Anritsu Eletrônica Ltda.

Praça Amadeu Amaral, 27 - 1 Andar
01327-010 - Bela Vista - São Paulo - SP - Brazil
Phone: +55-11-3283-2511
Fax: +55-11-3288-6940

● **Mexico**

Anritsu Company, S.A. de C.V.

Av. Ejército Nacional No. 579 Piso 9, Col. Granada
11520 México, D.F., México
Phone: +52-55-1101-2370
Fax: +52-55-5254-3147

● **United Kingdom**

Anritsu EMEA Ltd.

200 Capability Green, Luton, Bedfordshire, LU1 3LU, U.K.
Phone: +44-1582-433200
Fax: +44-1582-731303

● **France**

Anritsu S.A.

12 avenue du Québec, Bâtiment Iris 1- Silic 612,
91140 VILLEBON SUR YVETTE, France
Phone: +33-1-60-92-15-50
Fax: +33-1-64-46-10-65

● **Germany**

Anritsu GmbH

Nemetschek Haus, Konrad-Zuse-Platz 1
81829 München, Germany
Phone: +49-89-442308-0
Fax: +49-89-442308-55

● **Italy**

Anritsu S.r.l.

Via Elio Vittorini 129, 00144 Roma, Italy
Phone: +39-6-509-9711
Fax: +39-6-502-2425

● **Sweden**

Anritsu AB

Kistagången 20B, 164 40 KISTA, Sweden
Phone: +46-8-534-707-00
Fax: +46-8-534-707-30

● **Finland**

Anritsu AB

Teknobulevardi 3-5, FI-01530 VANTAA, Finland
Phone: +358-20-741-8100
Fax: +358-20-741-8111

● **Denmark**

Anritsu A/S (Service Assurance)

Anritsu AB (Test & Measurement)

Kay Fiskers Plads 9, 2300 Copenhagen S, Denmark
Phone: +45-7211-2200
Fax: +45-7211-2210

● **Russia**

Anritsu EMEA Ltd.

Representation Office in Russia

Tverskaya str. 16/2, bld. 1, 7th floor.

Russia, 125009, Moscow
Phone: +7-495-363-1694
Fax: +7-495-935-8962

● **United Arab Emirates**

Anritsu EMEA Ltd.

Dubai Liaison Office

P O Box 500413 - Dubai Internet City
Al Thuraya Building, Tower 1, Suit 701, 7th Floor
Dubai, United Arab Emirates
Phone: +971-4-3670352
Fax: +971-4-3688460

● **India**

Anritsu India Private Limited

2nd & 3rd Floor, #837/1, Binnamangla 1st Stage,
Indiranagar, 100ft Road, Bangalore - 560038, India
Phone: +91-80-4058-1300
Fax: +91-80-4058-1301

● **Singapore**

Anritsu Pte. Ltd.

11 Chang Charn Road, #04-01, Shriro House
Singapore 159640
Phone: +65-6282-2400
Fax: +65-6282-2533

● **P.R. China (Shanghai)**

Anritsu (China) Co., Ltd.

Room 2701-2705, Tower A,
New Caohejing International Business Center
No. 391 Gui Ping Road Shanghai, 200233, P.R. China
Phone: +86-21-6237-0898
Fax: +86-21-6237-0899

● **P.R. China (Hong Kong)**

Anritsu Company Ltd.

Unit 1006-7, 10/F., Greenfield Tower, Concordia Plaza,
No. 1 Science Museum Road, Tsim Sha Tsui East,
Kowloon, Hong Kong, P.R. China
Phone: +852-2301-4980
Fax: +852-2301-3545

● **Japan**

Anritsu Corporation

8-5, Tamura-cho, Atsugi-shi, Kanagawa, 243-0016 Japan
Phone: +81-46-296-1221
Fax: +81-46-296-1238

● **Korea**

Anritsu Corporation, Ltd.

502, 5FL H-Square N B/D, 681
Sampyeong-dong, Bundang-gu, Seongnam-si,
Gyeonggi-do, 463-400 Korea
Phone: +82-31-696-7750
Fax: +82-31-696-7751

● **Australia**

Anritsu Pty. Ltd.

Unit 21/270 Ferntree Gully Road, Notting Hill,
Victoria 3168, Australia
Phone: +61-3-9558-8177
Fax: +61-3-9558-8255

● **Taiwan**

Anritsu Company Inc.

7F, No. 316, Sec. 1, NeiHu Rd., Taipei 114, Taiwan
Phone: +886-2-8751-1816
Fax: +886-2-8751-1817

Please Contact: