MP1632A/C

3.2 Gb/s Digital Data Analyzer

ANRITSU Corporation
Measurement Solutions
Digital.com Div.
Marketing Dept.

About MP1632A/C

Digital Data Analyzer

Commercialization

July, 1998

50MHz to 3.2GHz Operating Range

Compact Portable

High Input Sensitivity

Burst Signal Measurement

Eye Margin Measurement

Eye Contour Mapping

TARGET MARKET

R&D and Manufacturing

- **SONET/SDH Component**
  - E/O, O/E Modules
  - Clock Recovery Modules
  - Mux/Demux
  - Modulators
- **Undersea System**
- **WDM Component and System**
  - Grating Filters, EDFAs
  - Next Generation Fiber
- **Gigabit Ethernet and Fiber Channel**
- **General purpose digital IC and High-Speed IC**
  - GaAs, ASIC/FPGA, RAM etc.

Linking the World

MP1632A/C Product Outline

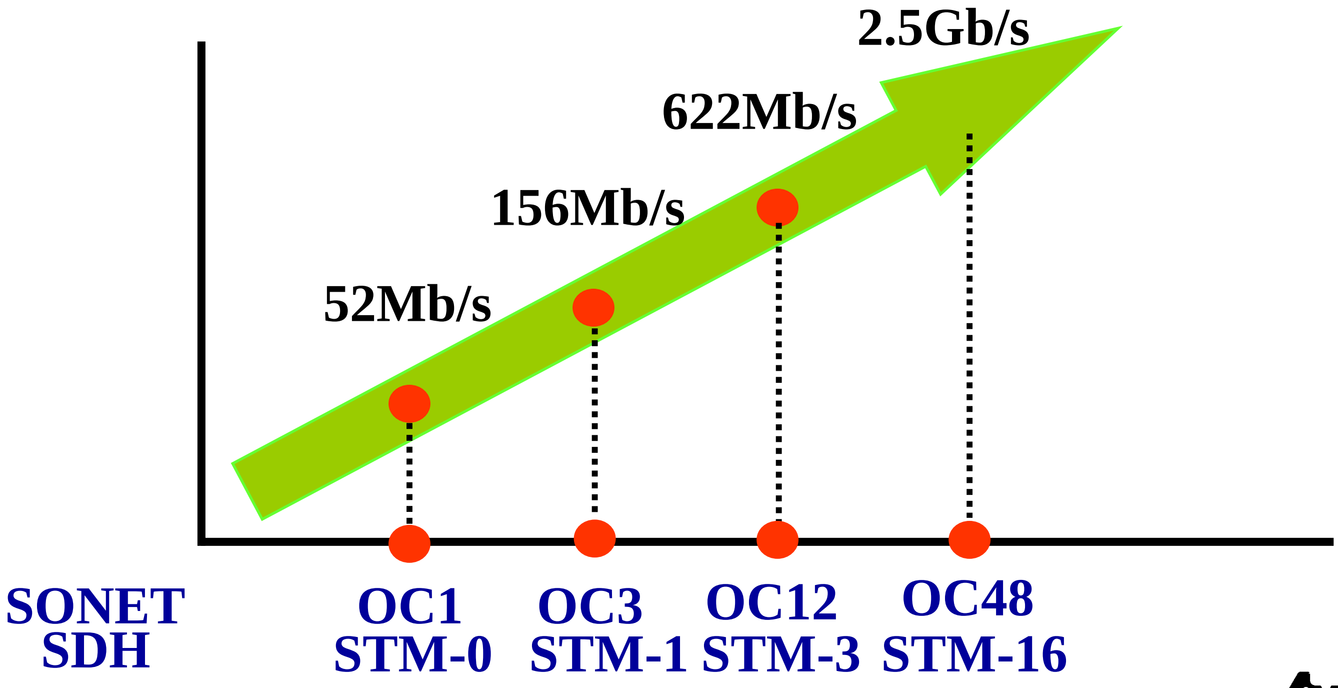
MP1632A/C	Mainframe
MP1632A/C*01	GPIB Remote Control
MP1632A/C*02	Ethernet Remote Control
MP1632A/C*03	3.2 GHz Internal Synthesizer
MP163220A/C	3.2 Gb/s Pulse Pattern Generator
MP163240A/C	3.2 Gb/s Error Detector

Linking the World

FEATURE

Wide Operation Range

- 50 MHz to 3.2 GHz with Internal Clock
- 10 MHz to 3.2 GHz with External Clock
- Covers STS-1 thru STS-48, Gigabit Ethernet Rates



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FEATURE

Compact Size

- **PPG, ED, and Clock Source In One Chassis**
- **1/2 Size of MP1652/53**
- **64 lbs vs. 150 lbs for MP1652/1653**

3.2GHz Internal Synthesizer

Empty Slot

Error Detector (ED)

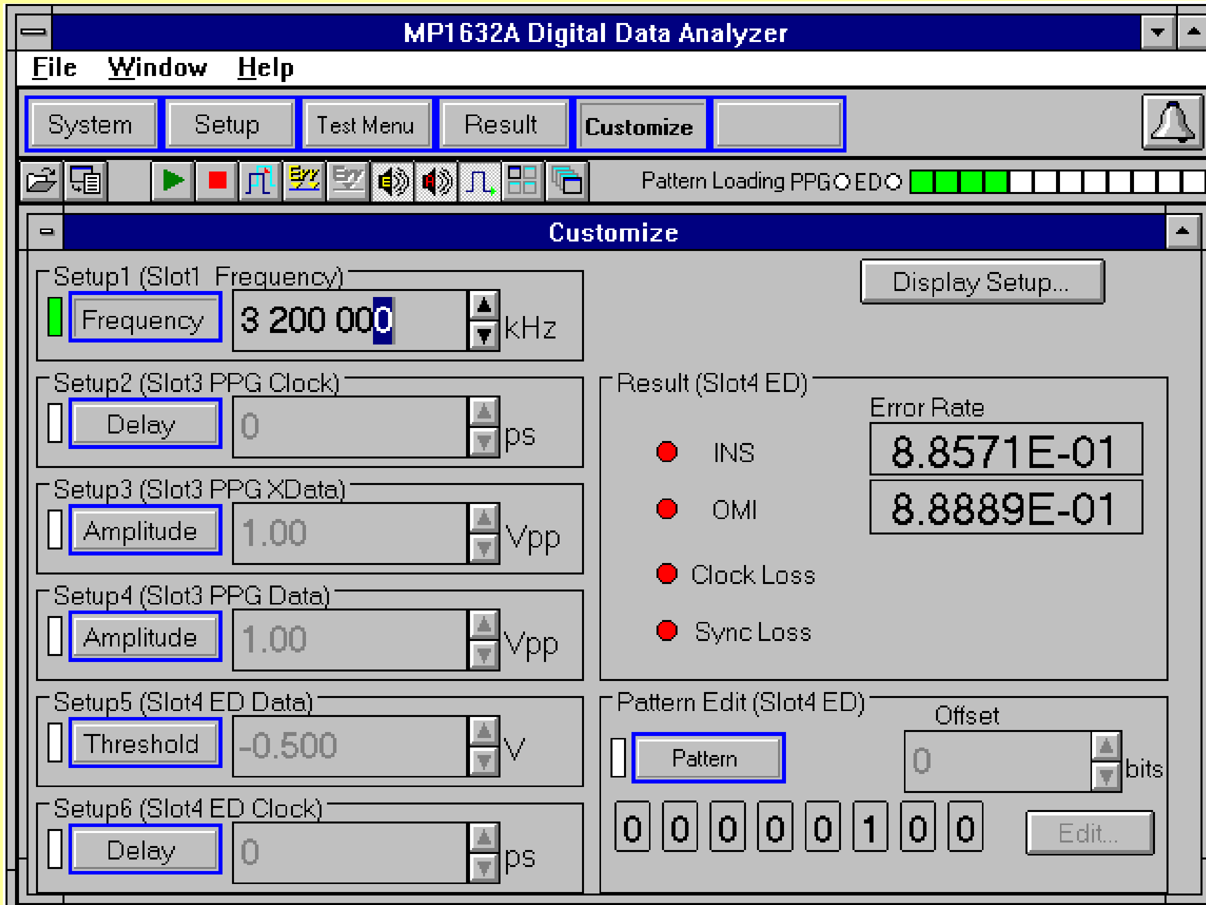
Pulse Pattern Generator (PPG)

Linking the World

FEATURE

One Key/One parameter operation

Customize Screen enables one key / one parameter



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Linking the World

FEATURE

Large Selection of Patterns

- **PRBS 2^n -1, n= 7, 9, 11, 15, 20, 23, 31**
  - **It has true PRBS mark ratio variable pattern**
- **Zero Substitution, 2n, n= 7, 9, 11, 15**
- **User Programmable, 2 bits to 8 Mbits**

Pattern Length		Resolution
**		
2 bits to 181072 bits	-	1 bit
181.072K to 262.144K	-	2 bits
262.144K to 524.288K	-	4 bits
524.288K to 1.048576M	-	8 bits
1.048576M to 2.097152M	-	16 bits
2.097152M to 4.194304M	-	32 bits
4.194304M to 8.388608M	-	64 bits

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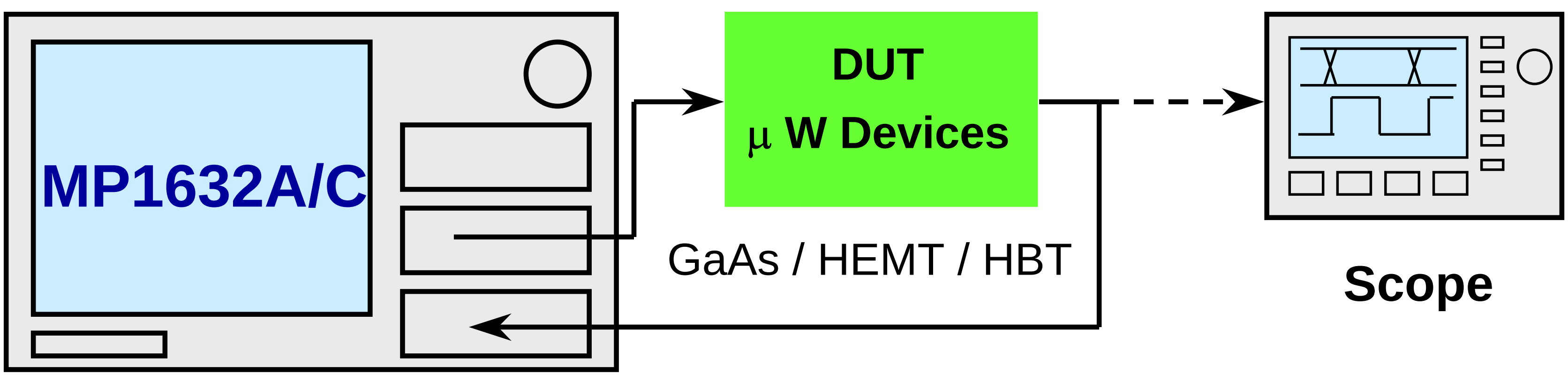
FEATURE

PRBS Pattern

Bit Length:	**2^N - 1 (N = 7, 9, 11, 15, 20, 23, 31)**
Mark Ratio:	**0/8, 1/8, 1/4, 1/2, 1/2, 3/4, 7/8, 8/8**

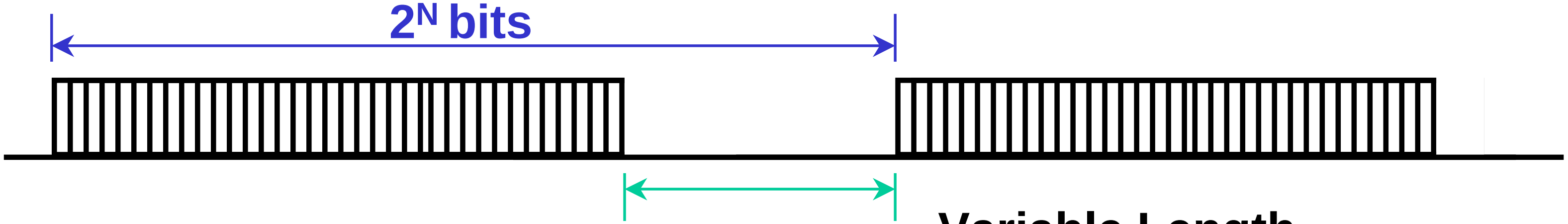
Testing DUTs Under Rigorous Conditions



Mark Ratio Stress Pattern

FEATURE

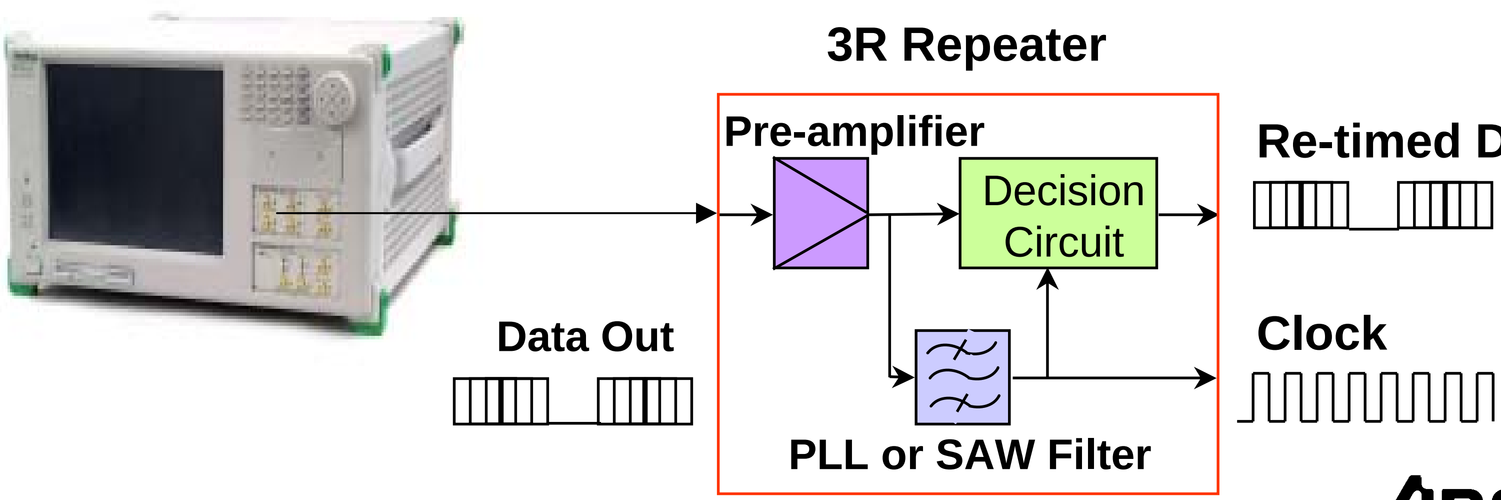
Zero Substitution Pattern



N = 7,9,11,15

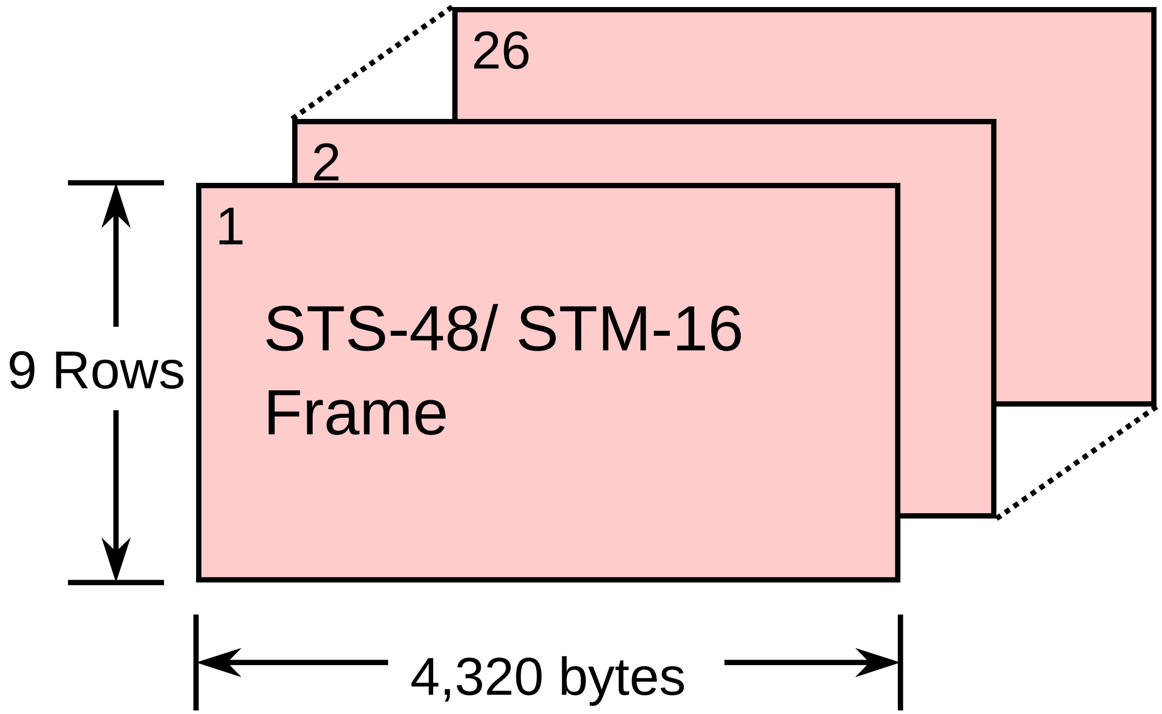
Variable Length 0 Substitution

Testing the Clock Regeneration of a 3R Repeater



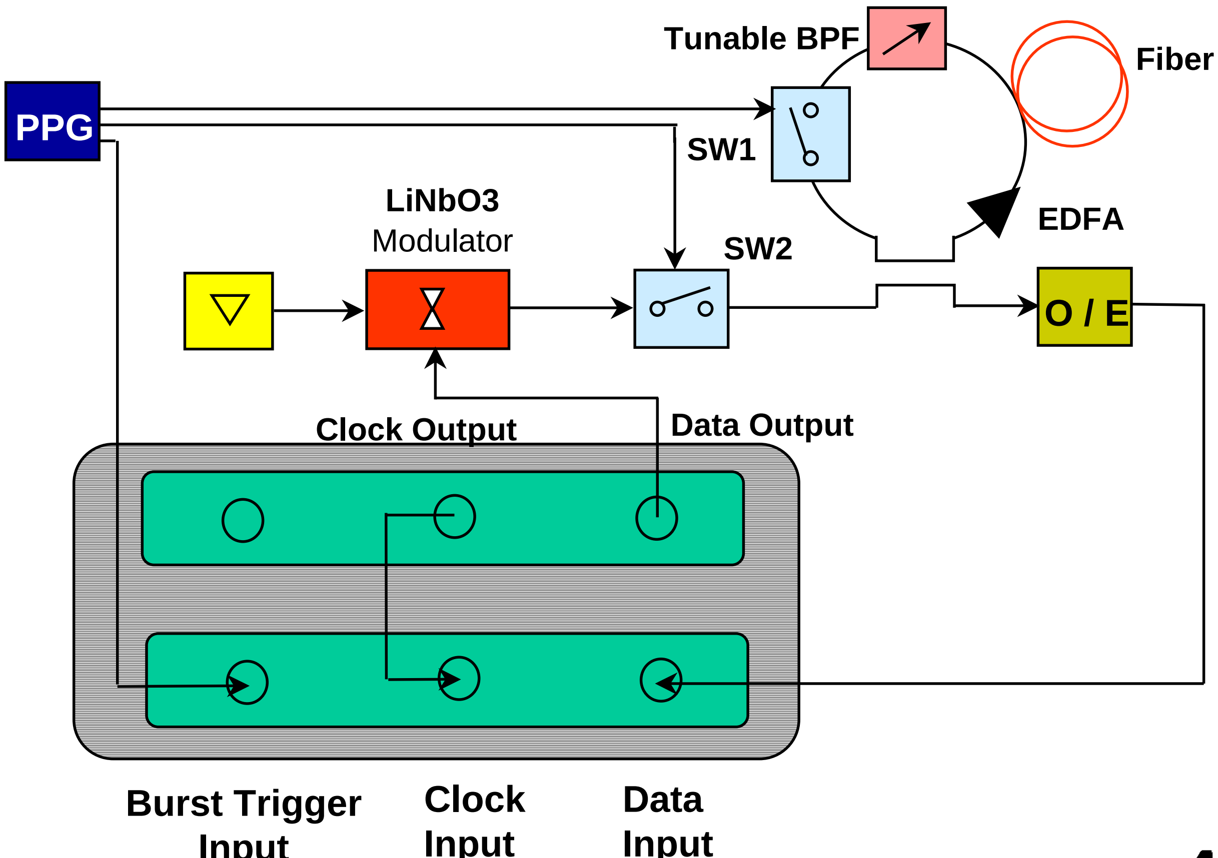
Programmable Pattern

(26 frames of STS-48/ STM-16)



Burst Signal Measurements

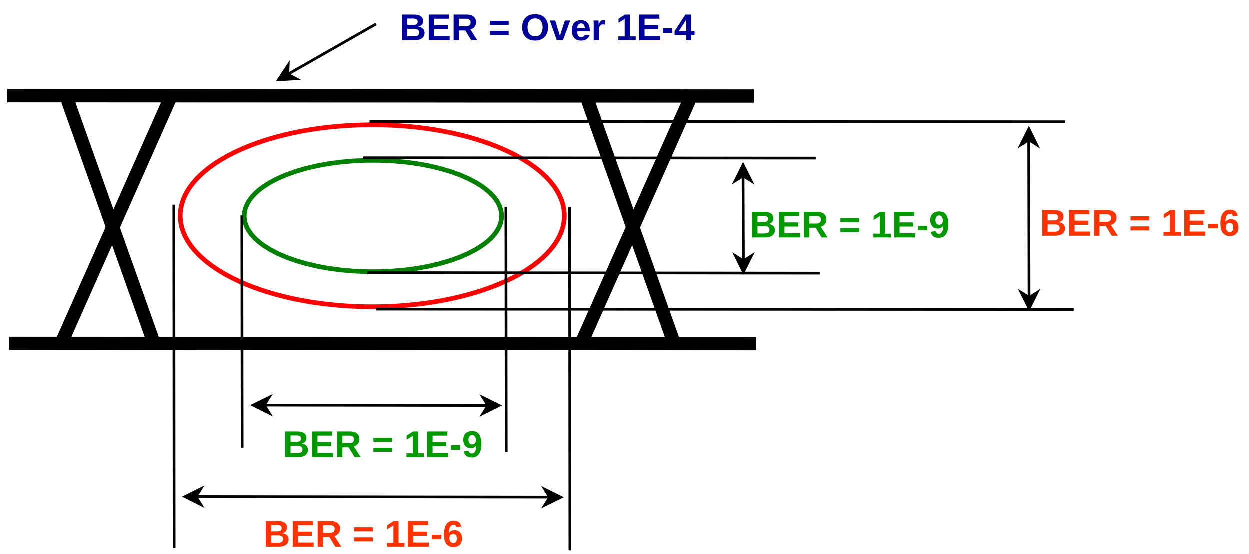
- **PPG has built-in gating signal**



FEATURE

Eye Margin Measurements

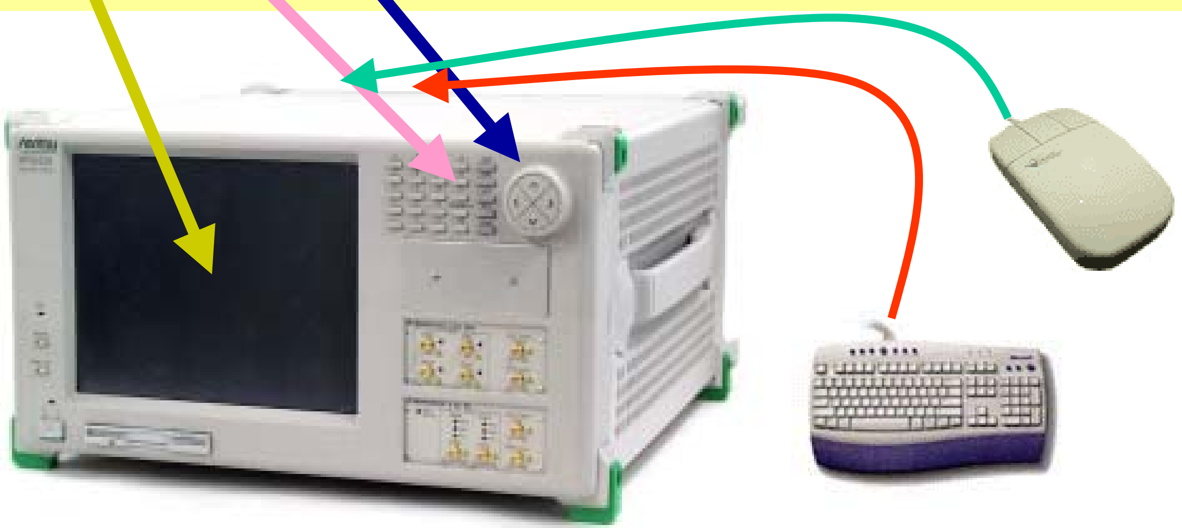
- Eye margin at center
- Eye Contour Diagram



FEATURE

Easy Operation

- Mouse & Keyboard
- Rotary Key
- Key Pad
- Touch Screen



FEATURE

Remote Control Operation

- GPIB
- RS-232c
- Ethernet (10 Base-T)

Other Features

- Familiar Windows 3.1 user interface
- Self-Check Diagnostic Mode
- Built-in Floppy Disk Drive / Hard Drive

MU163220A/C PPG

High Quality Data Output

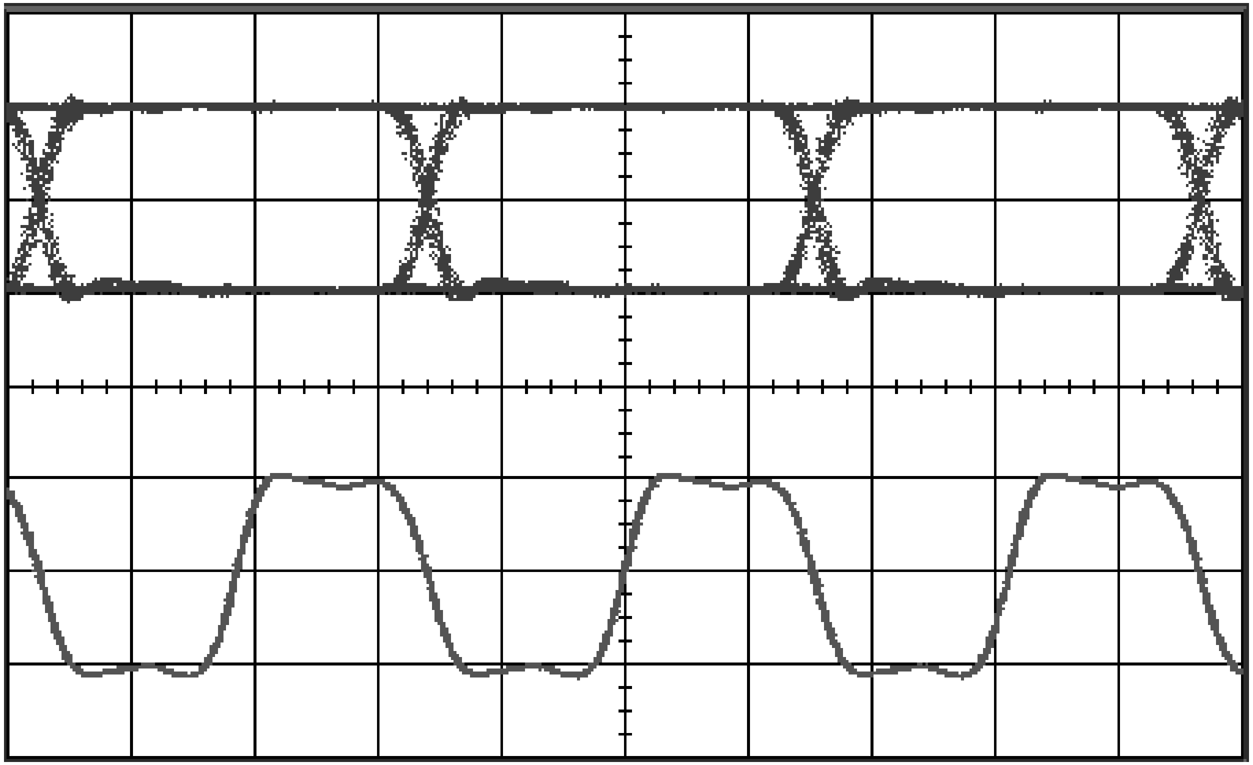
- Rise/Fall Time $\leq$ 80 ps
- Low Distortion Due to Internal Back Termination
- $\leq$ 30 ps p-p Pattern Jitter
- 0.5 to 2V p-p Amplitude Range
- Independent Data/Data Bar Amplitudes
- Internal Crosspoint Adjustment

MU163220A/C PPG

High Quality Clock Output

- Rise/Fall Time $\leq$ 80 ps
- Low Distortion Due to Internal Back Termination
- 0.5 to 2 V p-p Amplitude Range
- Independent Clock/Clock Bar Amplitudes
- Clock Duty Cycle Adjustment
- Adjustable Clock Delay

High Quality Data & Clock Wave-form



Data Output

Clock Output

H:100ps/div V:1V/div @3.2Gb/s

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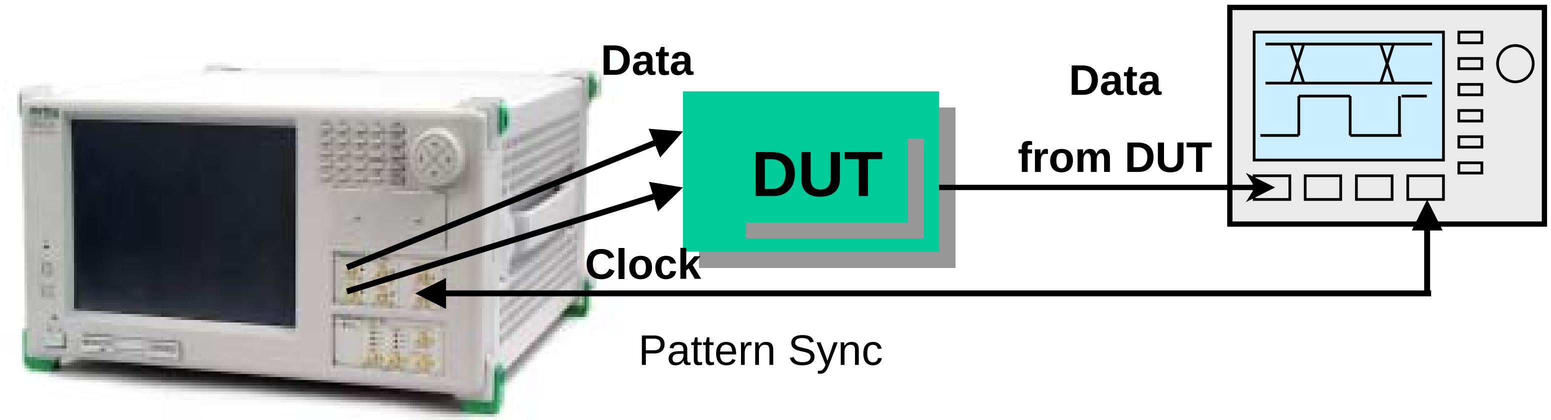
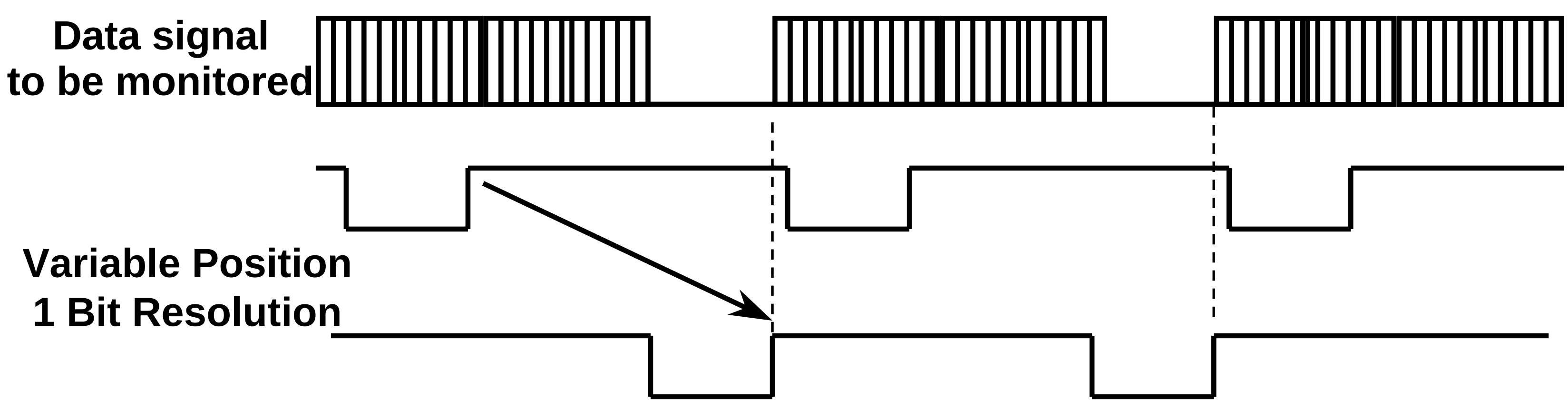
MU163220A/C PPG

Trigger Output





MU163240A/C ED

Error Detector Key Features

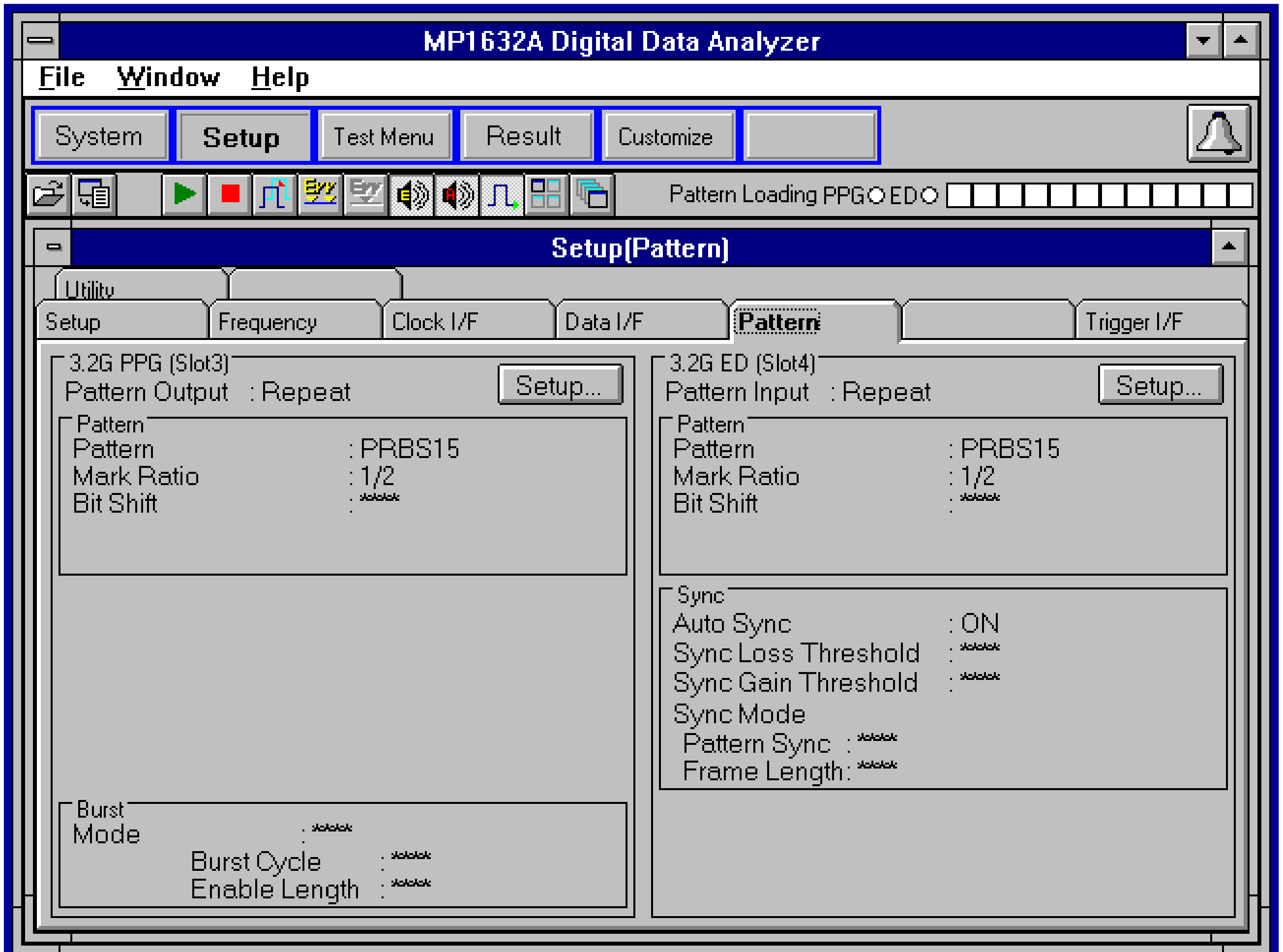
- High Input Sensitivity: 25 mV @ 3Gb/s, 2^{23}-1
- Wide Phase Margin: 250 ps @ 3Gb/s, 2^{23}-1
- Auto Search Functions
- Can Mask Channels from Error Detection
- Supports GND, ECL (-2V), and PECL (+3 V)
- Simultaneous Measurement of Insertion/Omission Errors

MP1632A/C Operation

Pattern Interface Setup Screen

LEVEL 1

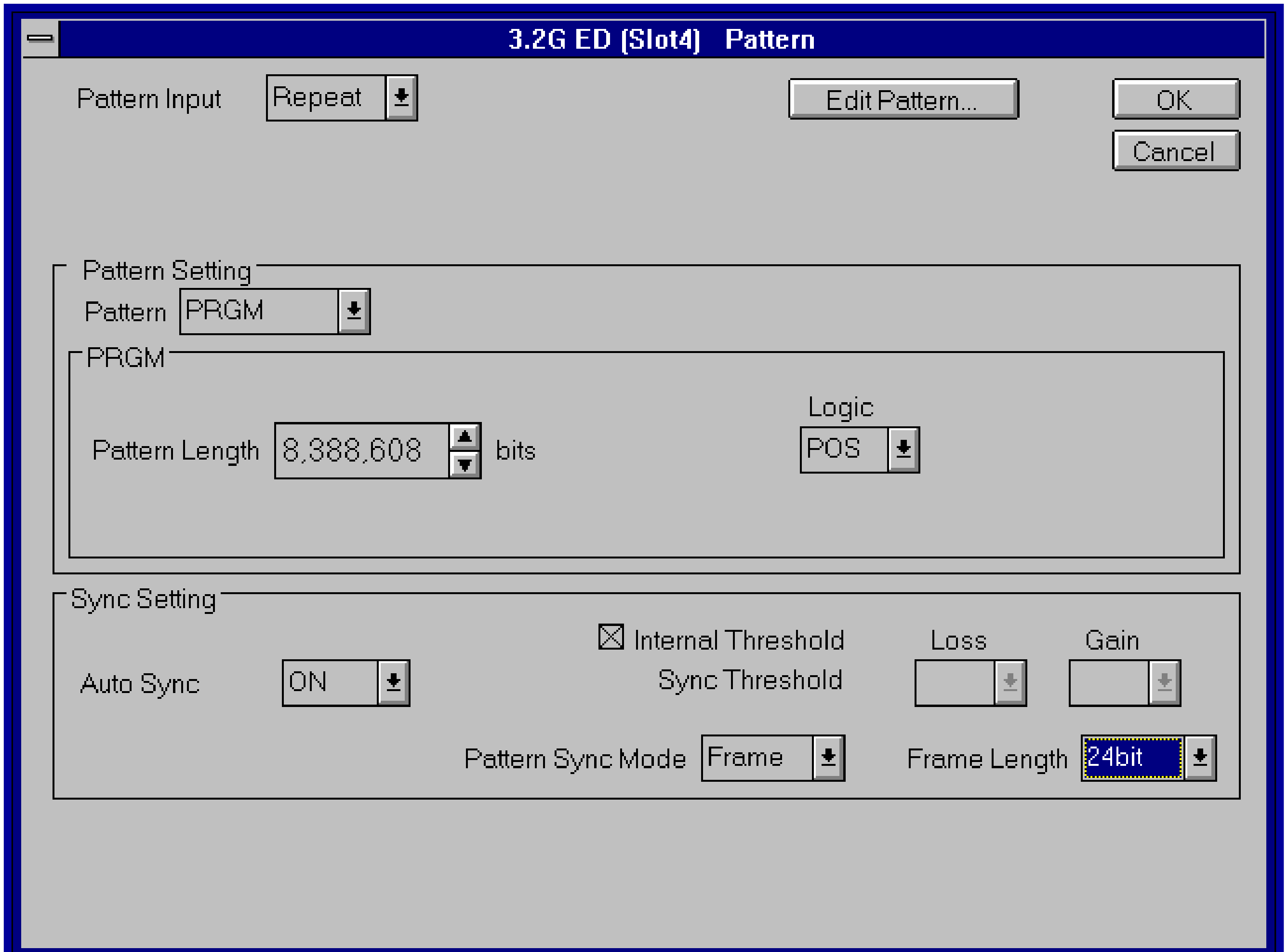
1



Pattern Interface Setup Screen

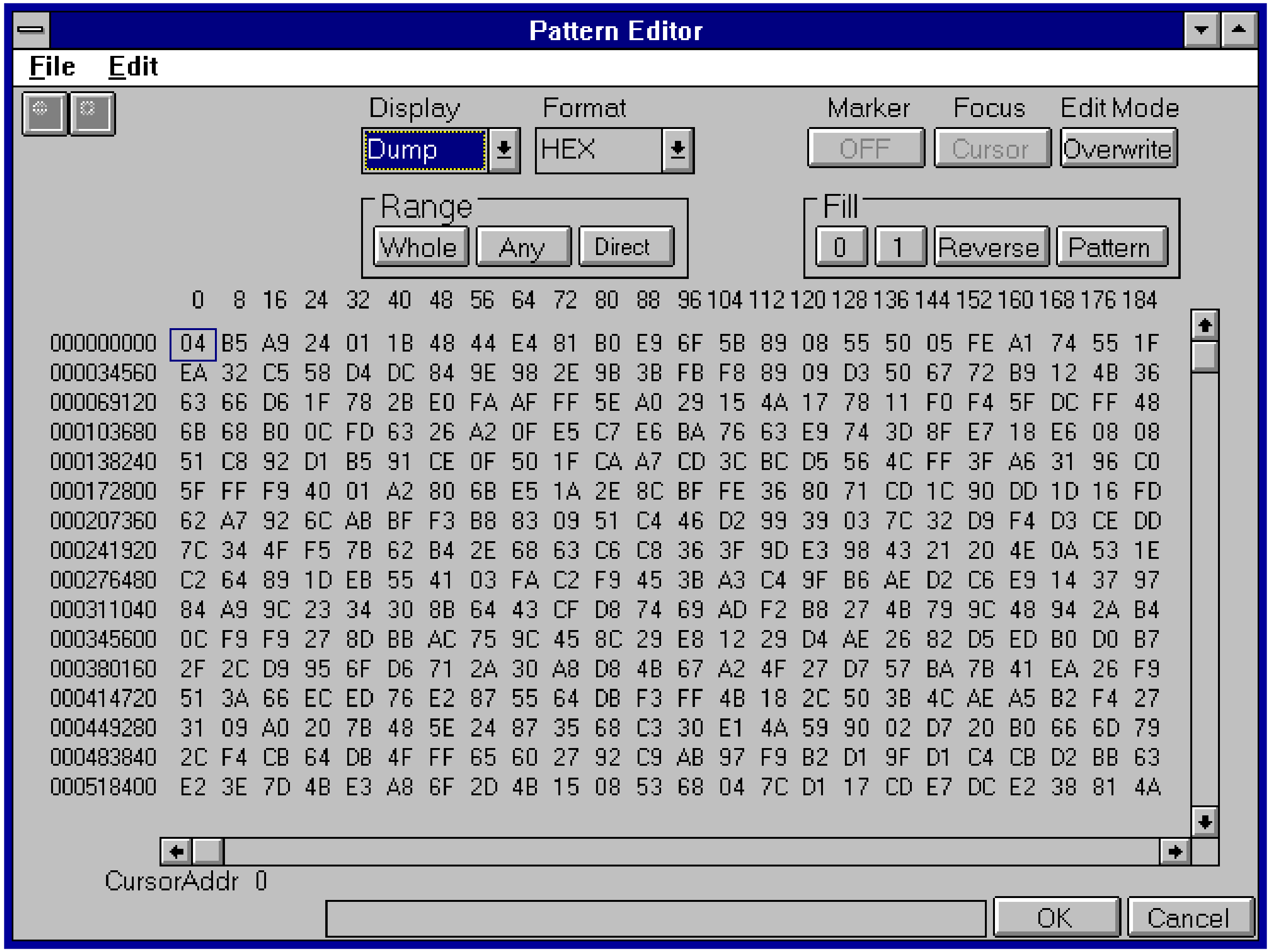
2

L E V E L 2



MP1632A/C Operation

On Screen Programmable Pattern Editor



	0	8	16	24	32	40	48	56	64	72	80	88	96	104	112	120	128	136	144	152	160	168	176	184
000000000	04	B5	A9	24	01	1B	48	44	E4	81	B0	E9	6F	5B	89	08	55	50	05	FE	A1	74	55	1F
000034560	EA	32	C5	58	D4	DC	84	9E	98	2E	9B	3B	FB	F8	89	09	D3	50	67	72	B9	12	4B	36
000069120	63	66	D6	1F	78	2B	E0	FA	AF	FF	5E	A0	29	15	4A	17	78	11	F0	F4	5F	DC	FF	48
000103680	6B	68	B0	0C	FD	63	26	A2	0F	E5	C7	E6	BA	76	63	E9	74	3D	8F	E7	18	E6	08	08
000138240	51	C8	92	D1	B5	91	CE	0F	50	1F	CA	A7	CD	3C	BC	D5	56	4C	FF	3F	A6	31	96	C0
000172800	5F	FF	F9	40	01	A2	80	6B	E5	1A	2E	8C	BF	FE	36	80	71	CD	1C	90	DD	1D	16	FD
000207360	62	A7	92	6C	AB	BF	F3	B8	83	09	51	C4	46	D2	99	39	03	7C	32	D9	F4	D3	CE	DD
000241920	7C	34	4F	F5	7B	62	B4	2E	68	63	C6	C8	36	3F	9D	E3	98	43	21	20	4E	0A	53	1E
000276480	C2	64	89	1D	EB	55	41	03	FA	C2	F9	45	3B	A3	C4	9F	B6	AE	D2	C6	E9	14	37	97
000311040	84	A9	9C	23	34	30	8B	64	43	CF	D8	74	69	AD	F2	B8	27	4B	79	9C	48	94	2A	B4
000345600	0C	F9	F9	27	8D	BB	AC	75	9C	45	8C	29	E8	12	29	D4	AE	26	82	D5	ED	B0	D0	B7
000380160	2F	2C	D9	95	6F	D6	71	2A	30	A8	D8	4B	67	A2	4F	27	D7	57	BA	7B	41	EA	26	F9
000414720	51	3A	66	EC	ED	76	E2	87	55	64	DB	F3	FF	4B	18	2C	50	3B	4C	AE	A5	B2	F4	27
000449280	31	09	A0	20	7B	48	5E	24	87	35	68	C3	30	E1	4A	59	90	02	D7	20	B0	66	6D	79
000483840	2C	F4	CB	64	DB	4F	FF	65	60	27	92	C9	AB	97	F9	B2	D1	9F	D1	C4	CB	D2	BB	63
000518400	E2	3E	7D	4B	E3	A8	6F	2D	4B	15	08	53	68	04	7C	D1	17	CD	E7	DC	E2	38	81	4A

T
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3

MP1632A/C Operation

On Screen Programmable Pattern Editor

4

T
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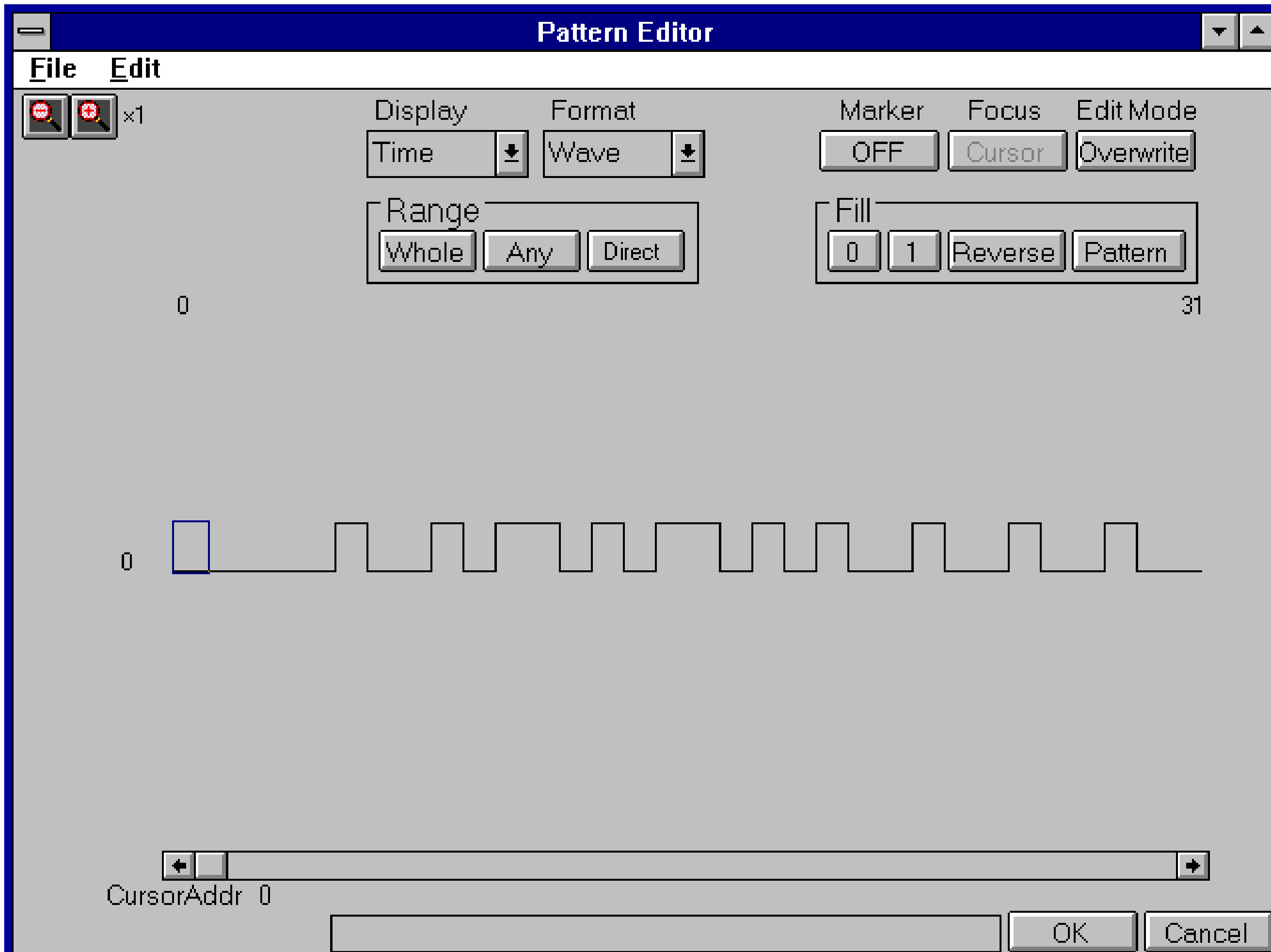
M
E



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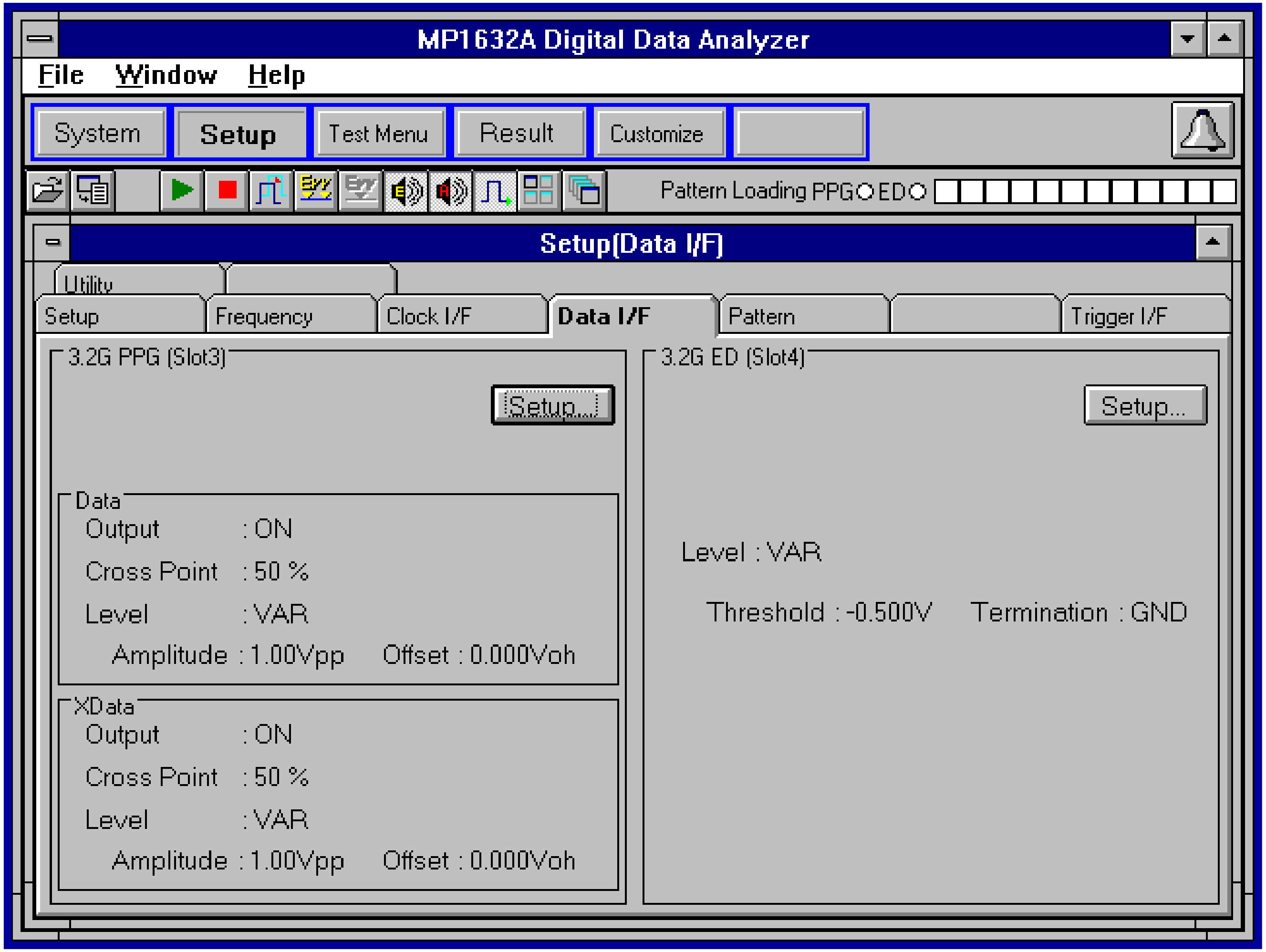
MP1632A/C Operation

Data Interface Setup Screen

5

LEVEL 1



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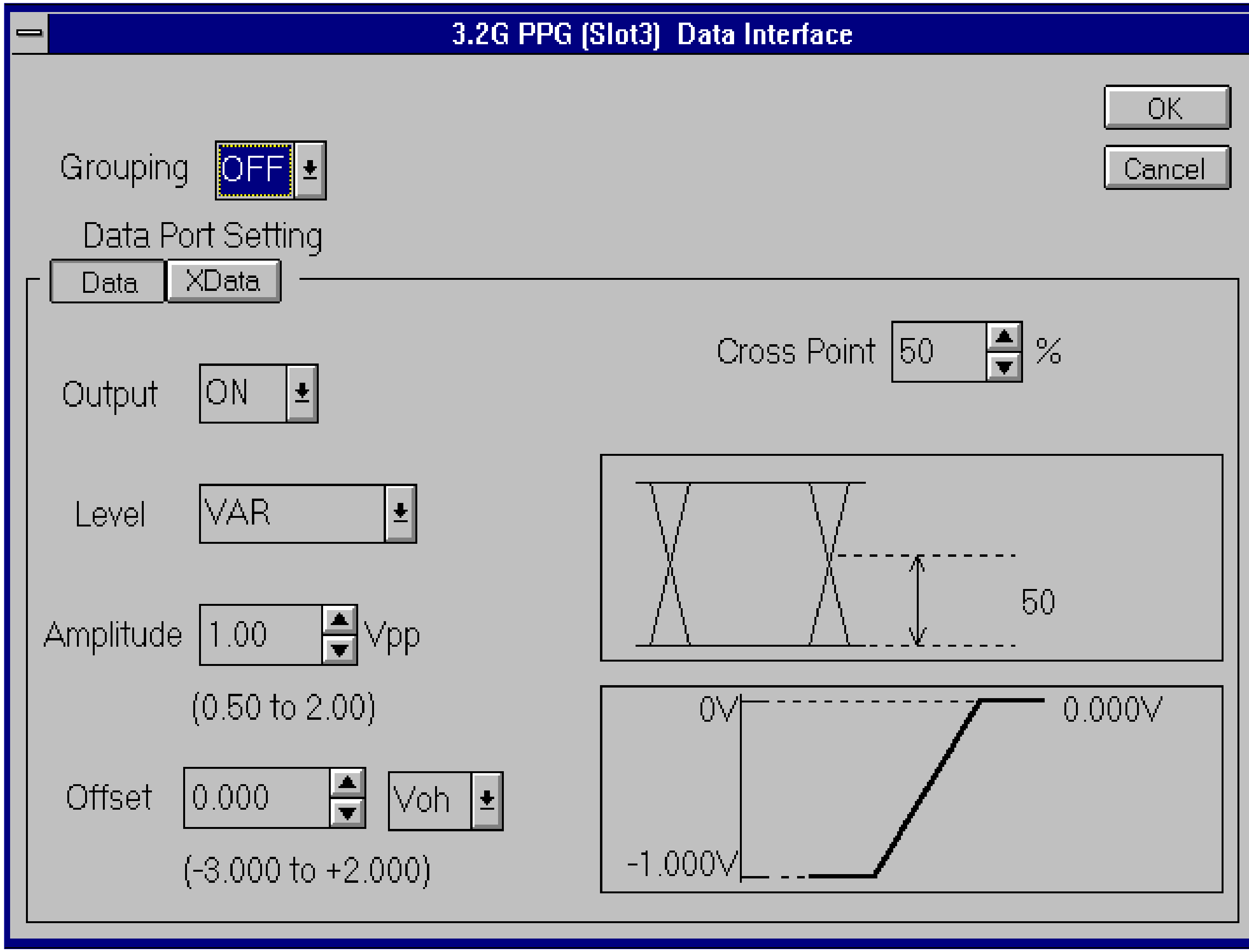
Data Interface Setup Screen

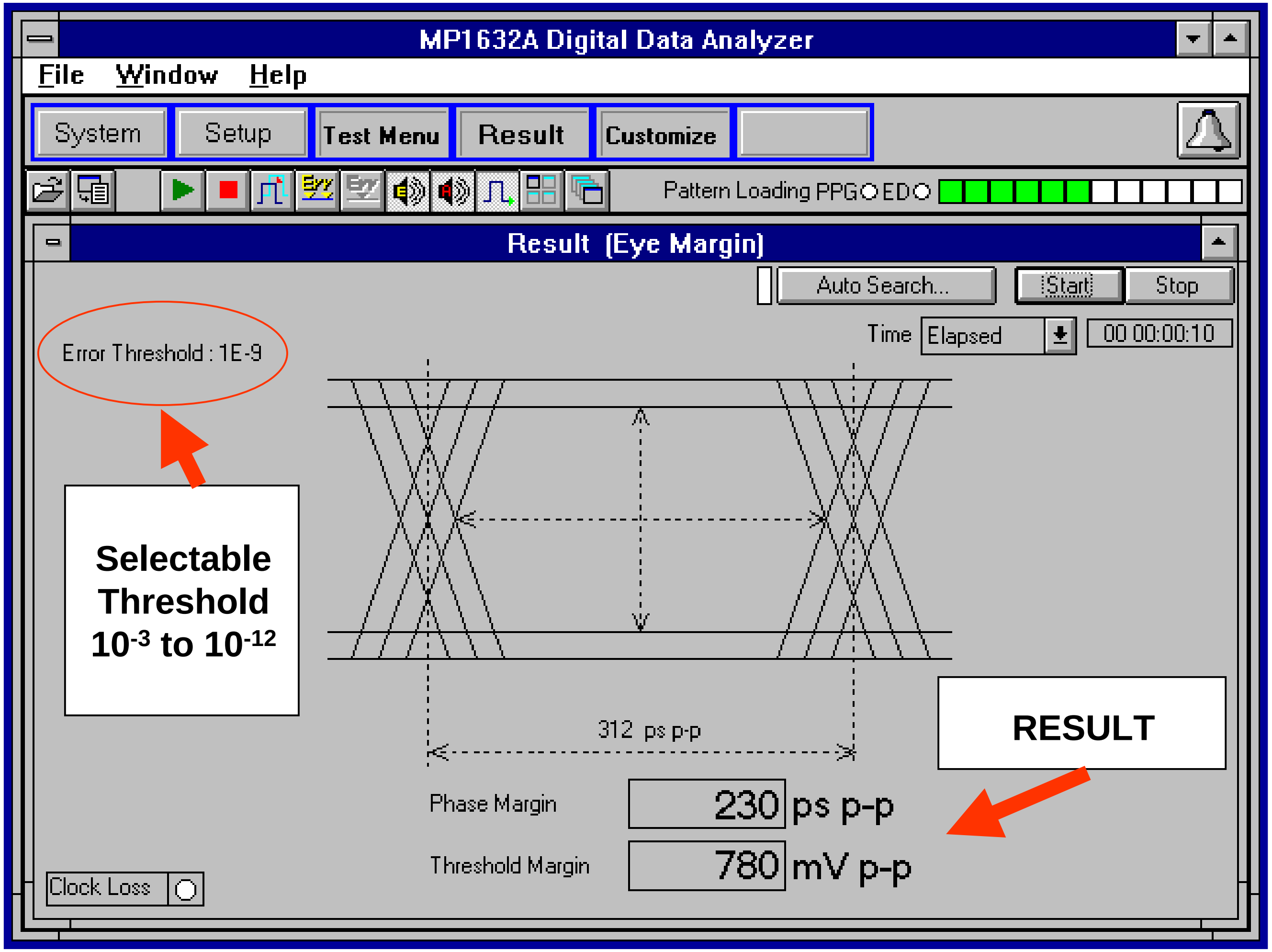
6

LEVEL 2



MP1632A/C Operation

Eye Margin at Center

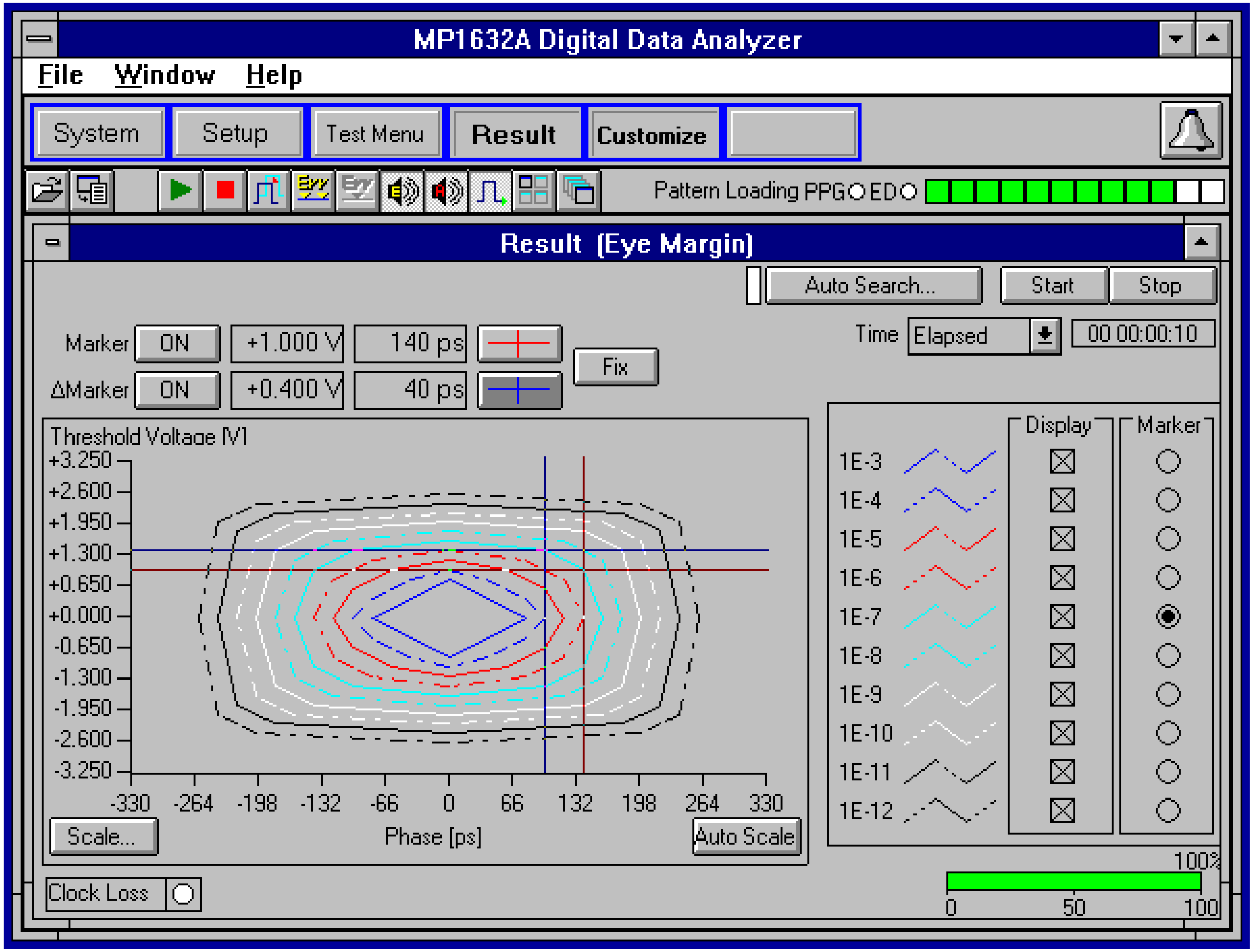


7

MP1632A/C Operation

Eye Contour Diagram

8



Results for 10^{-3} through 10^{-12}

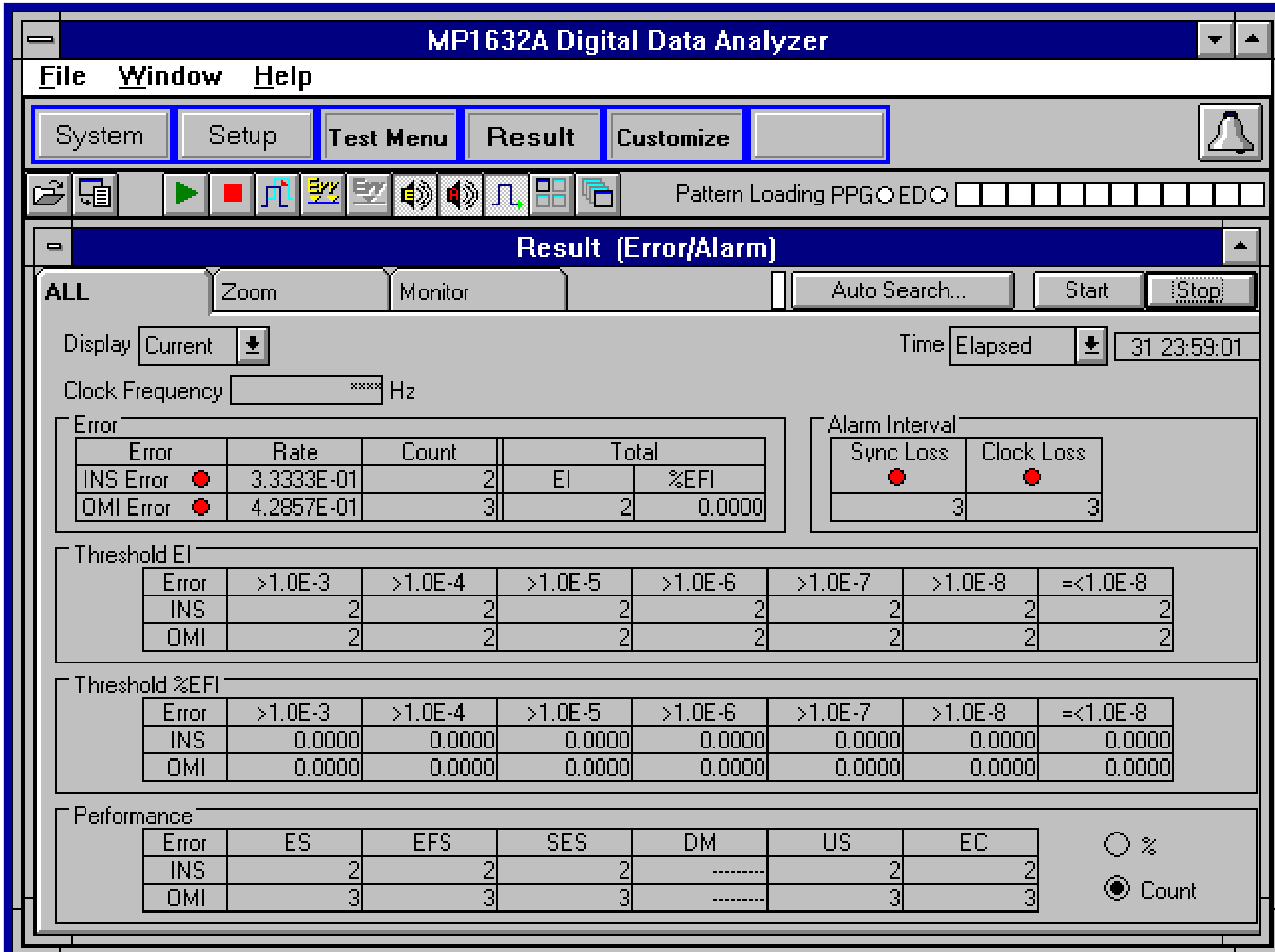
MP1632A/C Operation

Result Screen

9

A
L
L

M
O
D
E

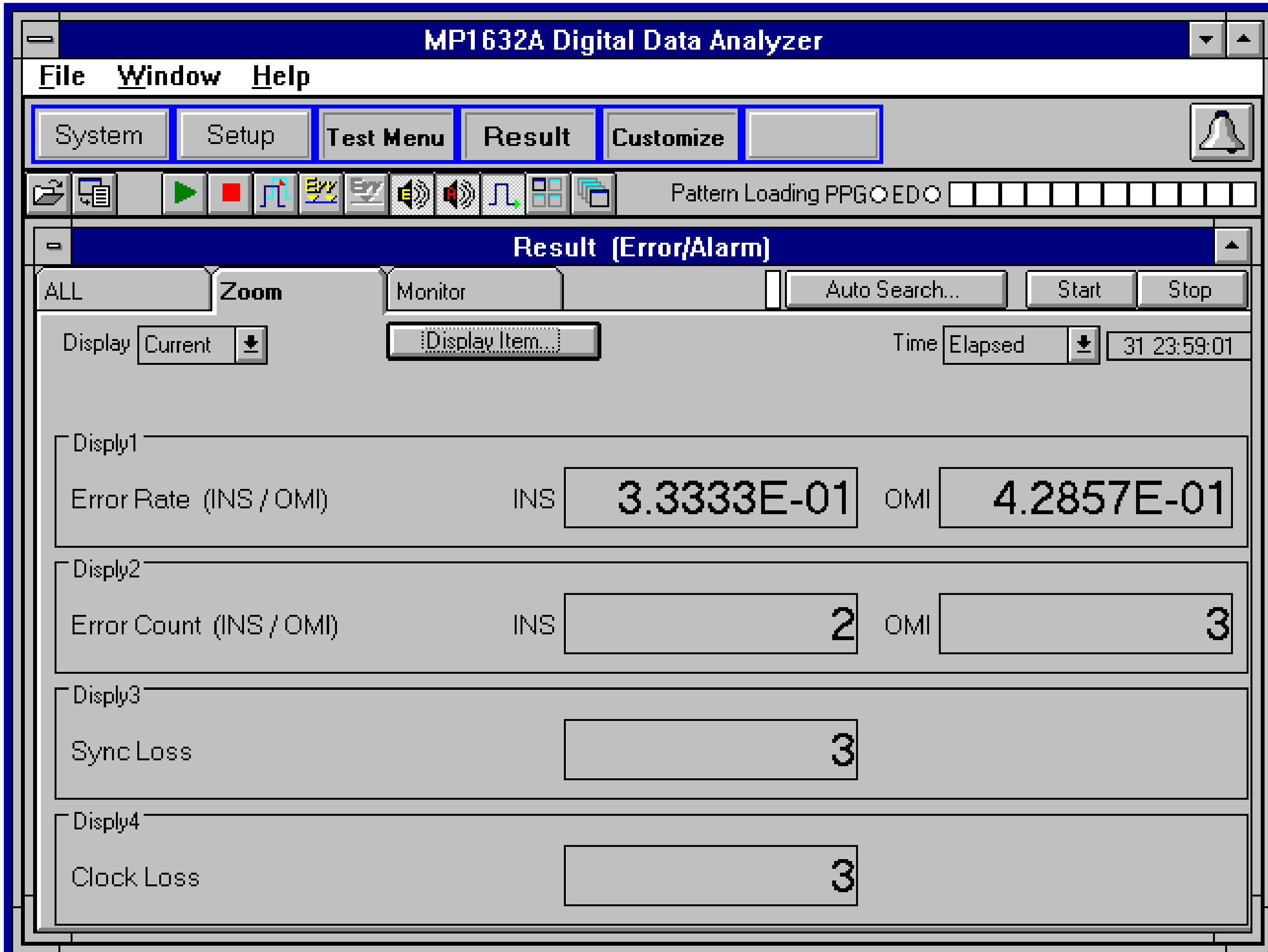


MP1632A/C Operation

Result Screen

10

Z O O M   M O D E



Key Points to Remember

- 50MHz to 3.2GHz Operation Range
- Supports Burst Signal Measurements
- High Quality Data & Clock Waveforms
- ED Has 25 mVp-p of Sensitivity
- Eye Margin & Eye Contour Mapping
- 8Mb Programmable Pattern
- PRBS up to 2^{31}-1 with Variable Mark Ratio
- Compact size, Portable & Lightweight

BERTS Basics

ANRITSU Corporation
Measurement Solutions
Digital.com Div.
Marketing Dept.

Topics

- Test Patterns
- Oscilloscope Measurements
- Synchronization
- Margin Measurements
- Masking
- Burst Measurements
- Jitter Measurements

Test Patterns

- Pre-Defined Test Patterns
  - PRBS
  - Variable Mark Ratio Quasi-PRBS
  - Zero Substitution
- User-Defined Test Patterns
  - Programmed (PRGM)
  - Alternating
  - Mixed

BERT Test Patterns

- **A Test Pattern is the Pre-Defined sequence of Bits output by a Pulse Pattern Generator (PPG), stored as reference in the Error Detector (ED)**
- **There are two categories of test patterns:**
  - Pre-Defined Test Patterns
    - PRBS
    - Variable Mark Ratio Quasi-PRBS
    - Zero Substitution
  - User-Defined Test Patterns
    - Programmed (PRGM)
    - Alternating
    - Mixed

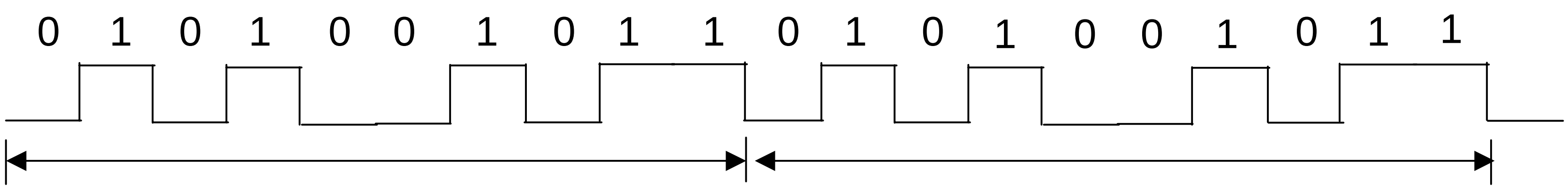
PRBS Patterns

Pseudo-**R**andom **B**inary **S**equence are pre-defined test patterns used to assess the performance of digital transmission equipment.

- **Pseudo-Random Binary Sequences are the most commonly used type of BERT test pattern.**
- **PRBS patterns are designed to Simulate Real Traffic**
- **PRBS patterns have a 2^n-1 Length**
- **Most Common n values are 7, 9, 11, 15, 20, 23, 31**
- **They are ITU defined patterns and are recognized throughout the telecom industry**
- **PRBS patterns are generated with Shift Register stages, XOR gates**
- **Contains n number of ONE's and n-1 number of ZERO's**

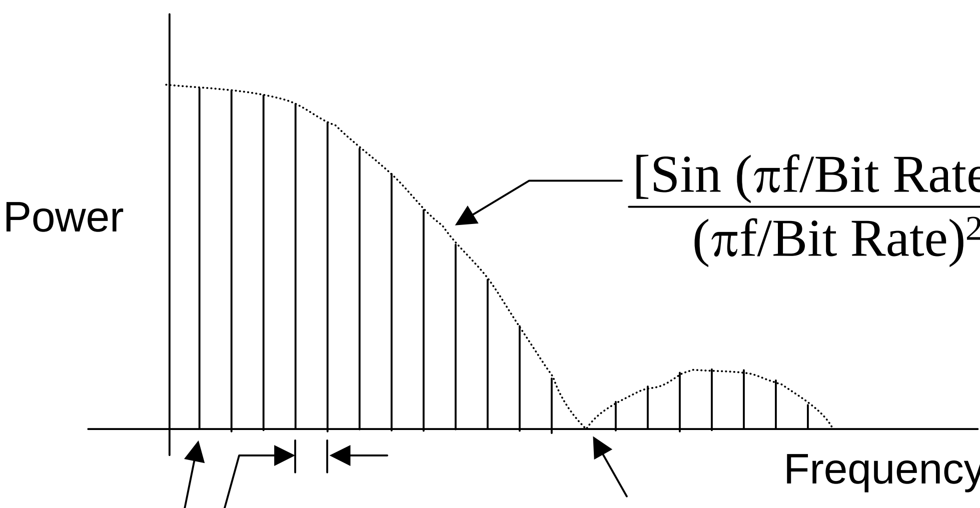
PRBS Spectral Content

PRBS "n" value (Pattern Length) effects Spectral Content



Pattern Repetition Period = (# of Bits in Pattern) x Bit Period

= (# of Bits in Pattern) / Bit Rate



$$\frac{[\mathrm{Sin}\ (\pi f/\mathrm{Bit\ Rate})]^2}{(\pi f/\mathrm{Bit\ Rate})^2}$$

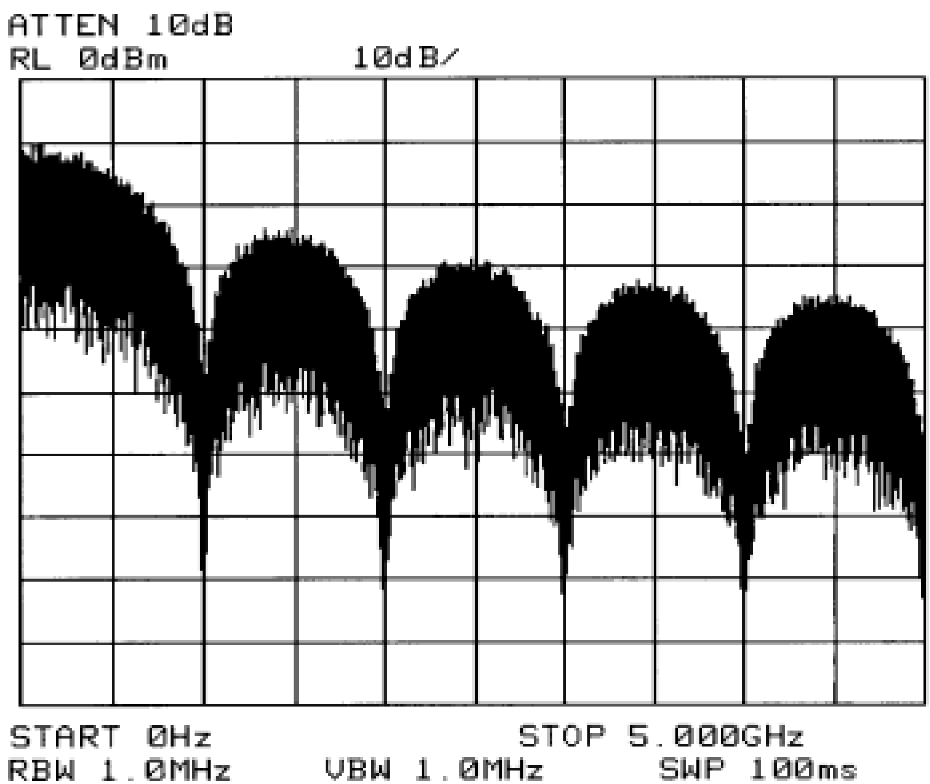
Pattern Repetition Frequency
Bit Rate / (# of Bits in Pattern)

The Higher the "n" Value, the Smaller the Spectral Line Spacing

Note: Number of Spectra from 0 Hz to Bit Rate = 2^n-1

PRBS Spectral Content

Spectrum of 2^{15}-1 Pattern at 1 Gbit



Nulls at 1G, 2G, etc.

PRBS Spectral Content

Example 1: 10 G Rate, 2^{15}-1 Pattern

Spectral Line Spacing = 10 G / 32,767 = **305,185 Hz**

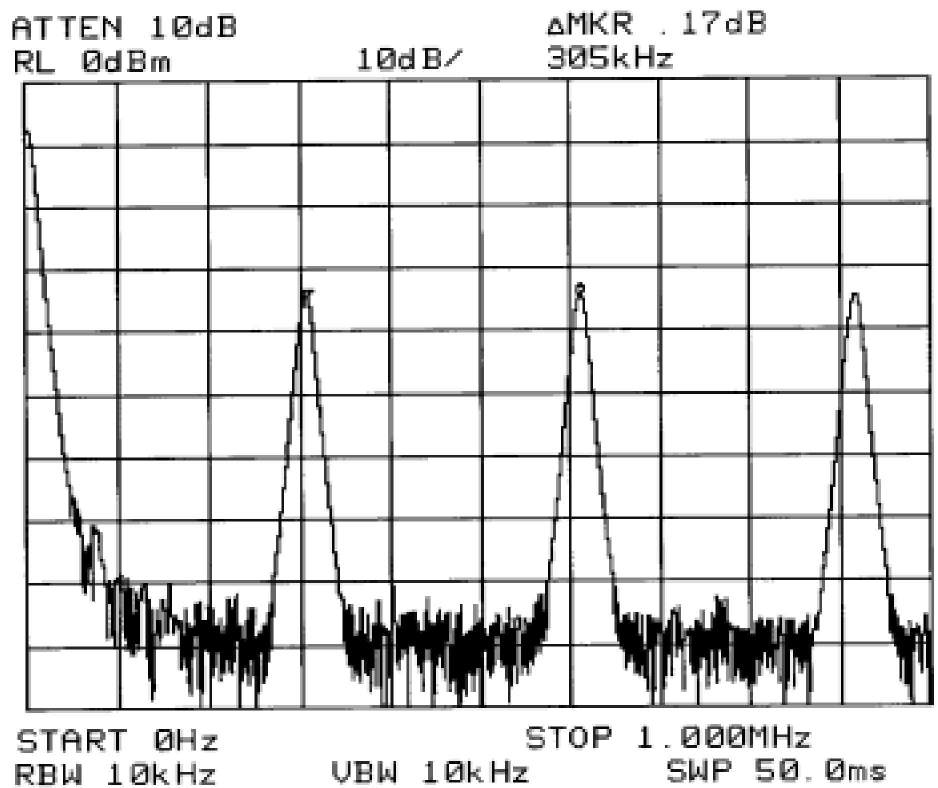
Example 2: 10 G Rate, 2^{31}-1 Pattern

Spectral Line Spacing = 10 G / 2,147,483,647 = **4.65 Hz**

Longer PRBS Patterns have Greater Spectral Content.
They Contain Lower Frequency Components.
Therefore, Longer Patterns are more Stressful.

2^{15}-1 PRBS Spectral Content

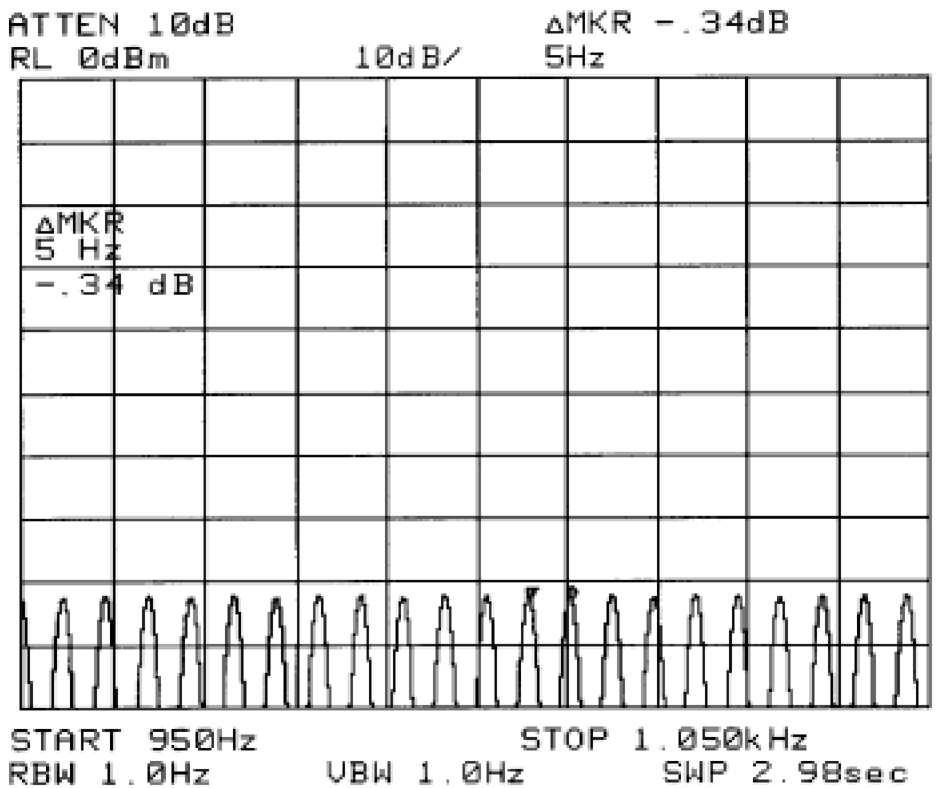
Spectrum of 2^{15}-1 Pattern at 10 Gbit



Spectral Spacing is approx. 305 kHz

2^{31}-1 PRBS Spectral Content

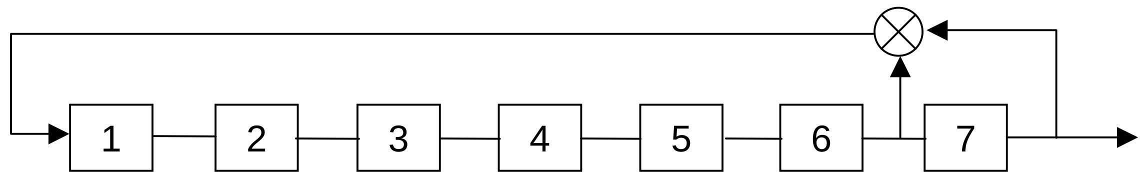
Spectrum of 2^{31}-1 Pattern at 10 Gbit



Spectral Spacing is approx. 5 Hz

2^7-1 PRBS Pattern

2^7-1 **127 bits long, Generation Polynomial: $1 + x^6 + x^7$**



1st Bit Sent → 6 Consecutive 0's

0 0 0 0 0 0 1 0 0 0 0 0 1 1 0 0
0 0 1 0 1 0 0 0 1 1 1 1 0 0 1 0
0 0 1 0 1 1 0 0 1 1 1 0 1 0 1 0
0 1 1 1 1 1 0 1 0 0 0 0 1 1 1 0
0 0 1 0 0 1 0 0 1 1 0 1 1 0 1 0
1 1 0 1 1 1 1 0 1 1 0 0 0 1 1 0
1 0 0 1 0 1 1 1 0 1 1 1 0 0 1 1
0 0 1 0 1 0 1 0 1 1 1 1 1 1 1

17th Bit Sent

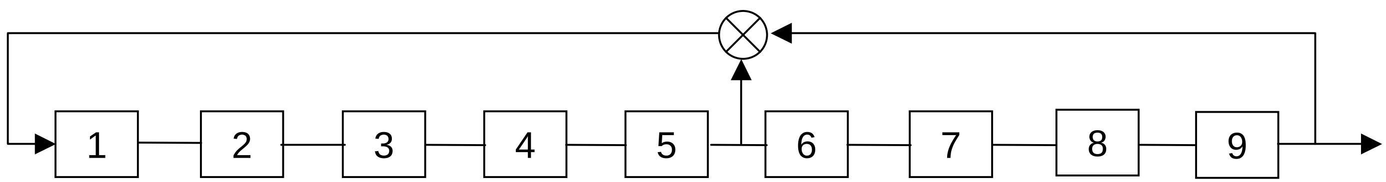
7 Consecutive 1's

Repeat 1st Bit

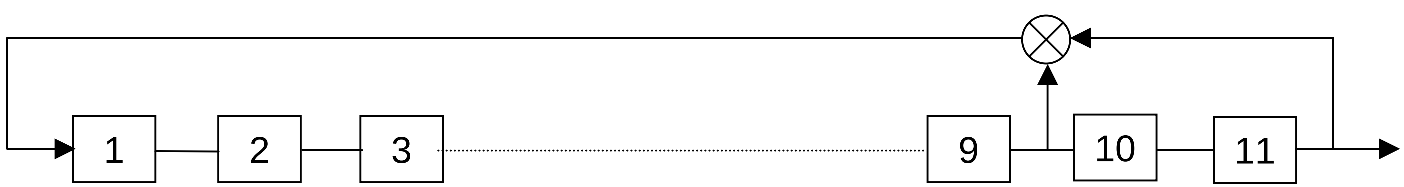
64 ONEs
63 ZEROs

2^9-1, 2^{11}-1 PRBS Patterns

2^9-1 **511 bits long, Generation Polynomial: $1 + x^5 + x^9$**

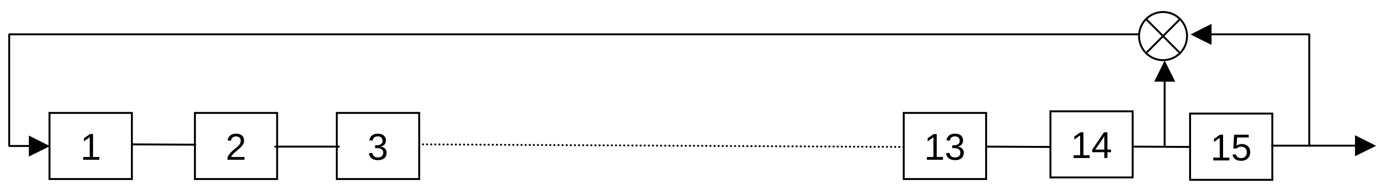


2^{11}-1 **2047 bits long, Generation Polynomial: $1 + x^9 + x^{11}$**

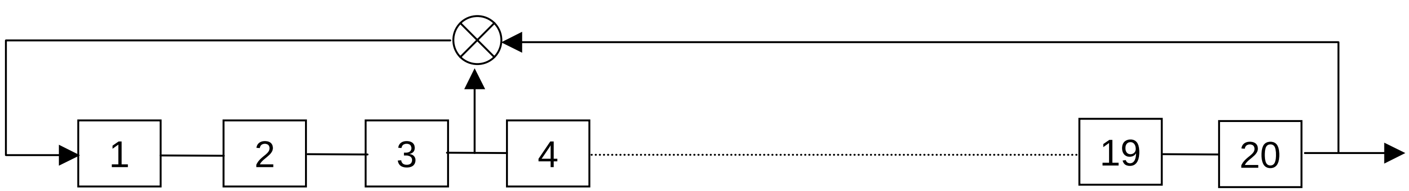


2^{15}-1, 2^{20}-1 PRBS Patterns

2^{15}-1 **32,767 bits long, Generation Polynomial: $1 + x^{14} + x^{15}$**

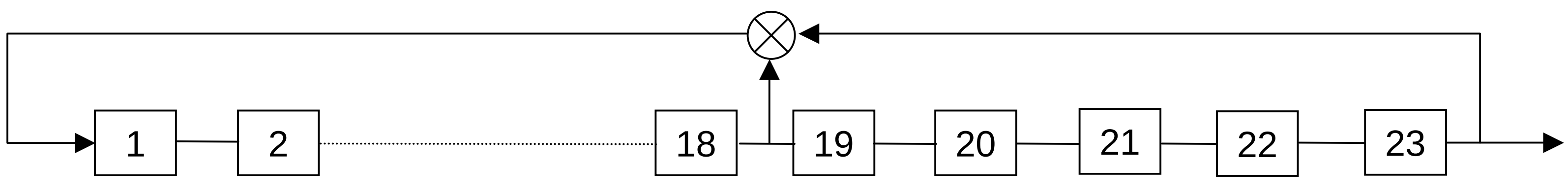


2^{20}-1 **1,048,575 bits long, Generation Polynomial: $1 + x^{3} + x^{20}$**

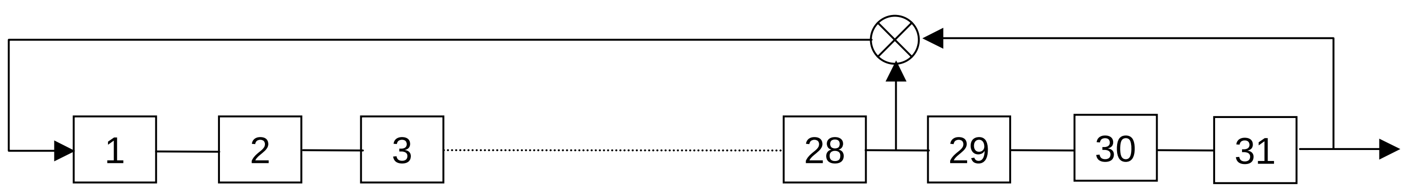


2^{23}-1, 2^{31}-1 PRBS Patterns

2^{23}-1 **8,388,607 bits long, Generation Polynomial: $1 + x^{18} + x^{23}$**



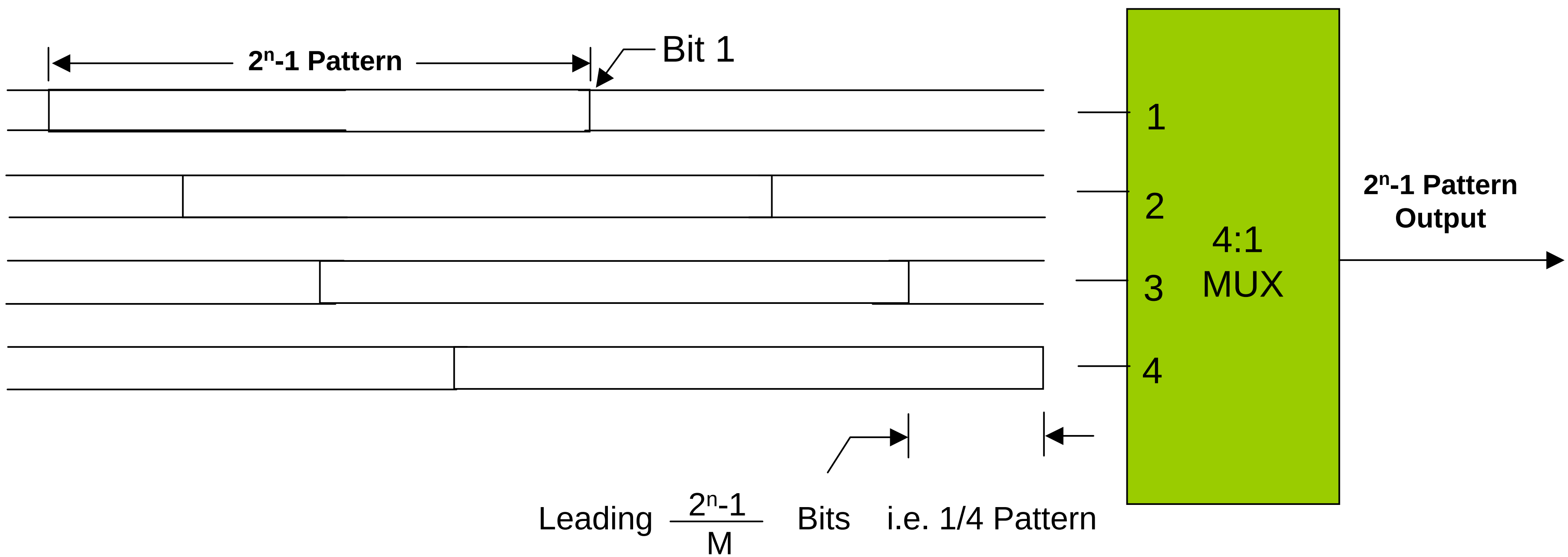
2^{31}-1 **2,147,483,647 bits long, Generation Polynomial: $1 + x^{28} + x^{31}$**



PRBS for Testing MUX

PRBS Patterns have a Property Useful for Testing Bit Interleaved MUX Circuits:

M "Parallel" PRBS patterns can be combined to give the same PRBS pattern. The patterns must be time delayed with respect to each other by (Pattern Length / M) bits



PRBS for MUX Testing

Example: 8:1 MUX

Channel 1 Input
7/8 Pattern Delay
w.r.t Channel 8

Same as Pattern Across Rows

Pattern Down Columns

0	0	0	0	0	0	1	0	0	0	0	0	1	1	0	0
0	0	1	0	1	0	0	0	1	1	1	1	0	0	1	0
0	0	1	0	1	1	0	0	1	1	1	0	1	0	1	0
0	1	1	1	1	1	0	1	0	0	0	0	1	1	1	0
0	0	1	0	0	1	0	0	1	1	0	1	1	0	1	0
1	1	0	1	1	1	1	0	1	1	0	0	0	1	1	0
1	0	0	1	0	1	1	1	0	1	1	1	0	0	1	1
0	0	1	0	1	0	1	0	1	1	1	1	1	1	1	

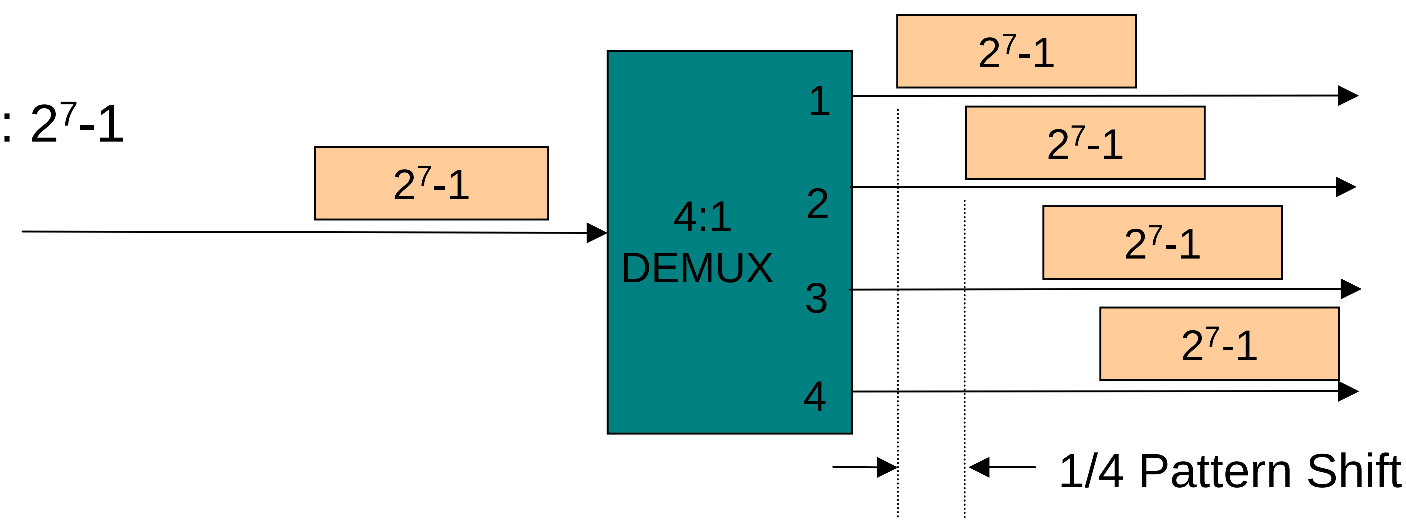
Channel 8 Input

PRBS for DEMUX Testing

PRBS Patterns have a useful property for testing Bit Interleaved DEMUX circuits:
When PRBS Patterns are DEMUXed by a Bit Interleave DEMUX Circuit, each DEMUX Channel Carries the complete input PRBS Pattern, staggered with respect to each other.

Each DEMUX Channel carries the SAME PATTERN !

Example: 2^7-1



PRBS for DEMUX Testing(1)

Example: 16:1 DEMUX

Channel 1 Output
15/16 Pattern Delay
w.r.t. Channel 16

Same as Pattern
Across Rows

Pattern Down
Columns

0 0 0 0 0 0 1 0 0 0 0 0 1 1 0 0
0 0 1 0 1 0 0 0 1 1 1 1 0 0 1 0
0 0 1 0 1 1 0 0 1 1 1 0 1 0 1 0
0 1 1 1 1 1 0 1 0 0 0 0 1 1 1 0
0 0 1 0 0 1 0 0 1 1 0 1 1 0 1 0
1 1 0 1 1 1 1 0 1 1 0 0 0 1 1 0
1 0 0 1 0 1 1 1 0 1 1 1 0 0 1 1
0 0 1 0 1 0 1 0 1 1 1 1 1 1 1

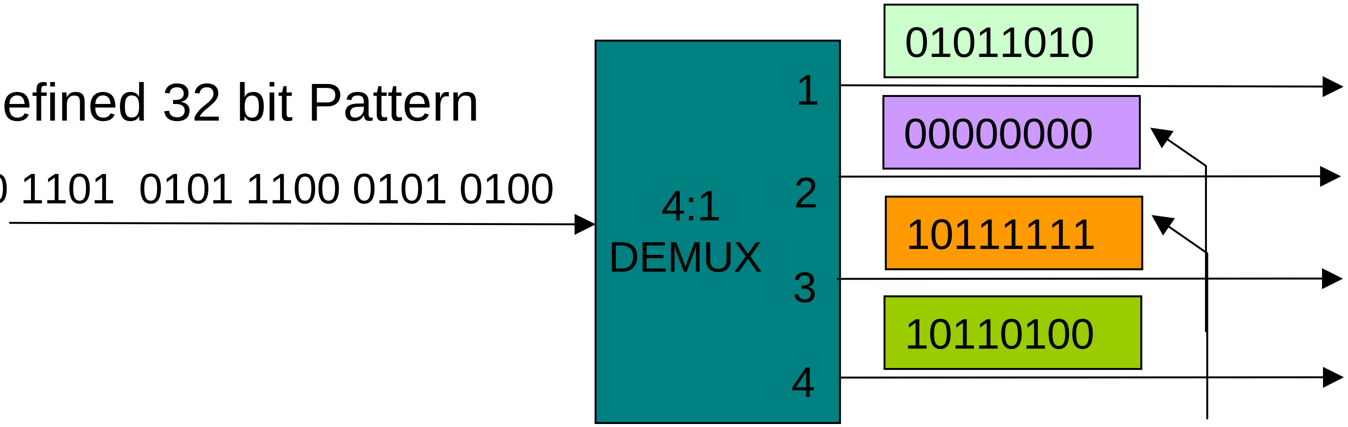
Non-PRBS Pattern for Testing DEMUX

- **A Non-PRBS Pattern (example: User-Defined Pattern) may result in DEMUX channels that carry "Non-Random" DATA.**

Each DEMUX Channel carries a DIFFERENT PATTERN !

Example: User Defined 32 bit Pattern

1100 0001 1100 1101 0101 1100 0101 0100



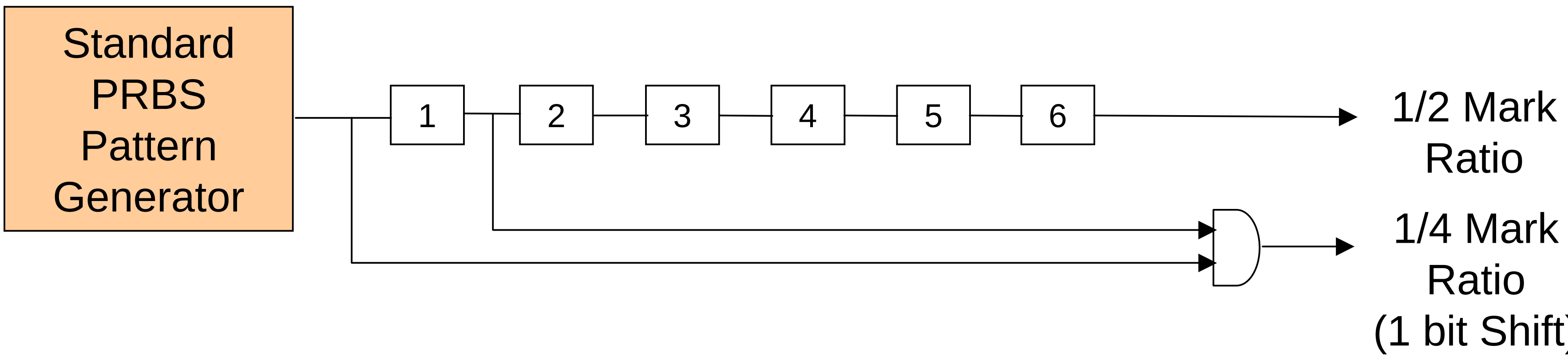
Channel 2 and 3 have Non-Random DATA

Variable Mark Ratio Quasi-PRBS

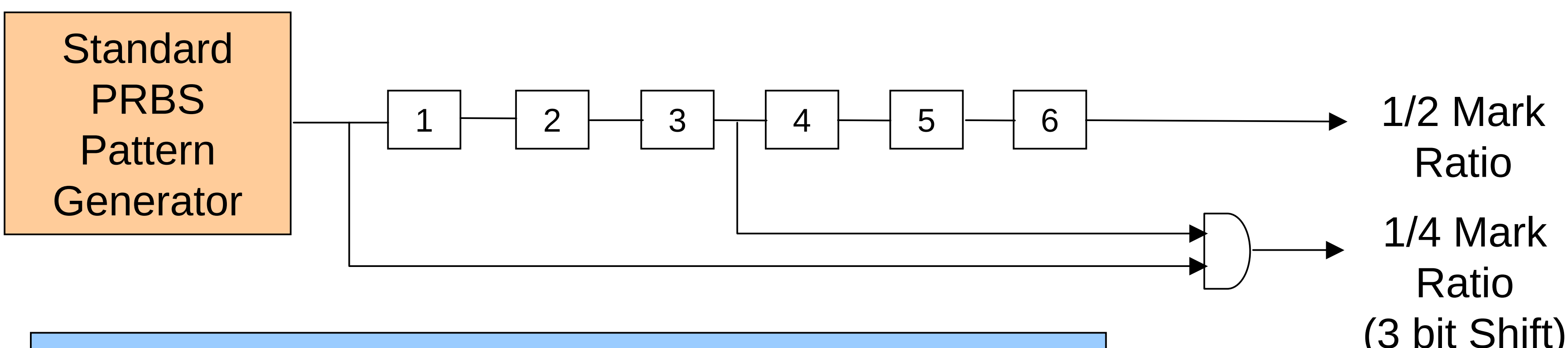
- **Variable Mark Ratio Can Be Adjusted to Create Patterns with High ONEs Density or High Zero's Density**
  - Purpose is to stress the Devices Under Test (DUT)
  - Variable Mark Ratio PRBS are not Standard PRBS Patterns
  - Derived from Standard PRBS patterns
  - Variable Mark Ratio patterns are implemented by adding one or more AND gates at the output of the standard PRBS pattern generation circuitry.
  - The most common available Mark Ratios are 1/8, 1/4, 3/4 and 7/8.
  - A given mark ratio can be generated using either a 1 Bit Shifted or 3 Bit Shifted technique.

Realization of 1/4 Mark Ratio Quasi-PRBS

Realization of 1/4 Mark Ratio with 1 Bit Shift



Realization of 1/4 Mark Ratio with 3 Bit Shift



3/4 Mark Ratio is Achieved by Inverting 1/8 Mark Ratio Pattern

Example of 1/4 Mark Ratio Quasi-PRBS

Example of 1 Bit Shift and 3 Bit Shift 1/4 Mark Ratio Pattern

2^7-1
1/4 Mark Ratio
1 Bit Shift

0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0
0 0 0 0 0 0 0 0 0 1 1 1 0 0 0 0
0 0 0 0 1 0 0 0 1 1 0 0 0 0 0 0
0 0 1 1 1 1 0 0 0 0 0 0 0 1 1 0
0 0 0 0 0 0 0 0 0 1 0 0 1 0 0 0
0 1 0 0 1 1 1 0 0 1 0 0 0 0 1 0
0 0 0 0 0 0 1 1 0 0 1 1 0 0 0 1
0 0 0 0 0 0 0 0 0 1 1 1 1 1 1

32 ONEs, 95 ZEROs
No "101" Patterns

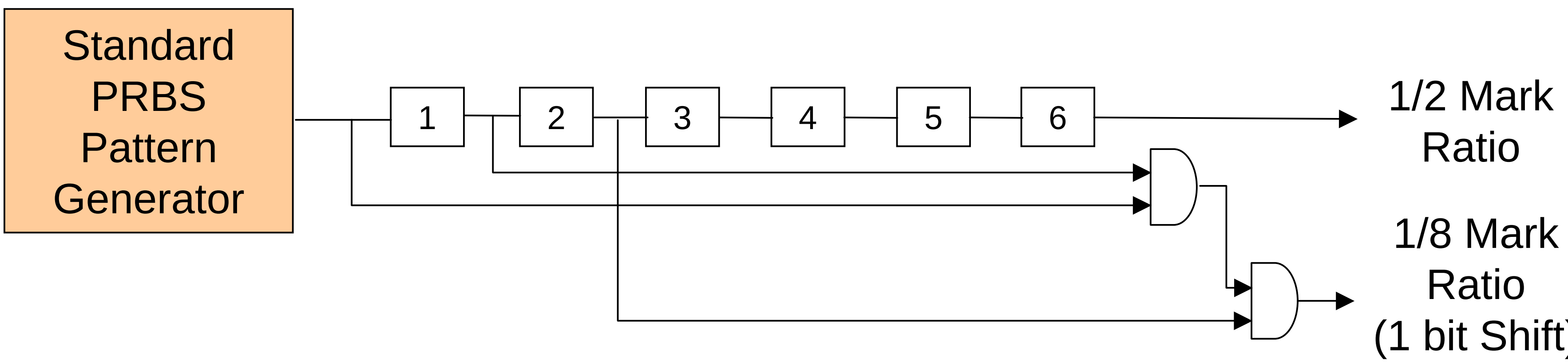
2^7-1
1/4 Mark Ratio
3 Bit Shift

0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 1 0 0 1 0
0 0 0 0 0 1 0 0 1 0 0 0 1 0 0 0
0 1 0 0 1 **1 0 1** 0 0 0 0 0 0 0 0
0 0 0 0 0 1 0 0 1 0 0 1 **1 0 1** 0
0 **1 0 1 1 0 1 0 1** 1 0 0 0 0 0 0
1 0 0 1 0 0 1 0 0 1 1 0 0 0 1 0
0 0 1 0 0 0 0 0 0 **1 0 1** 1 1 1

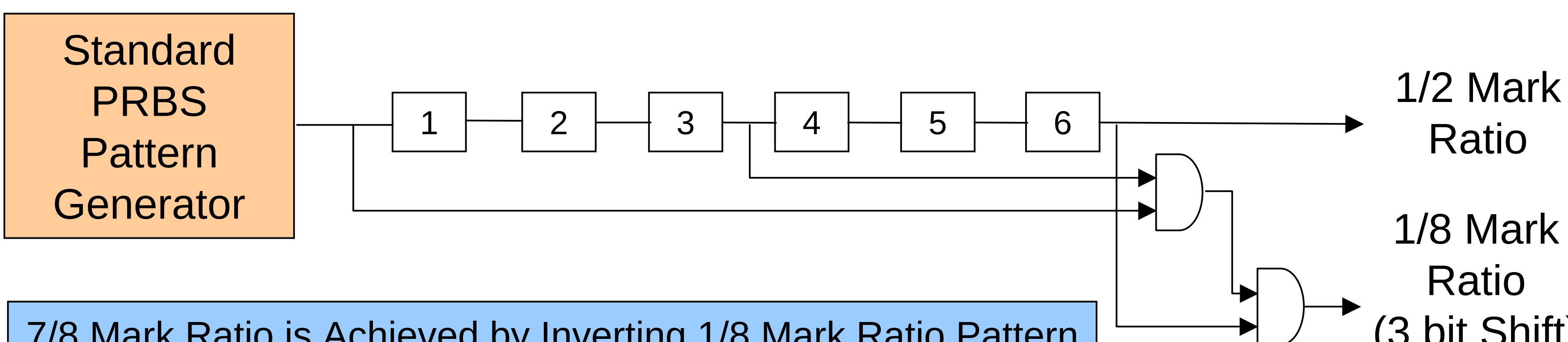
32 ONEs, 95 ZEROs
Contains "101" Patterns

Realization of 1/8 Mark Ratio Quasi-PRBS

Realization of 1/8 Mark Ratio with 1 Bit Shift



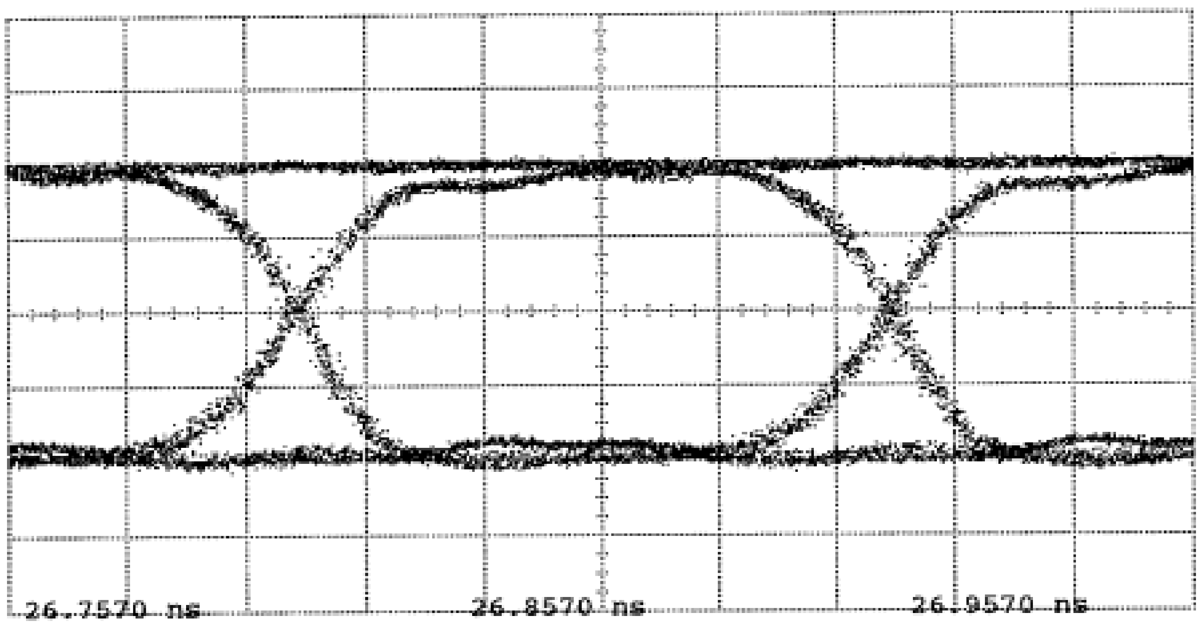
Realization of 1/8 Mark Ratio with 3 Bit Shift



7/8 Mark Ratio is Achieved by Inverting 1/8 Mark Ratio Pattern

Eye Diagram of 1/2 Mark Ratio PRBS

1/2 Mark Ratio

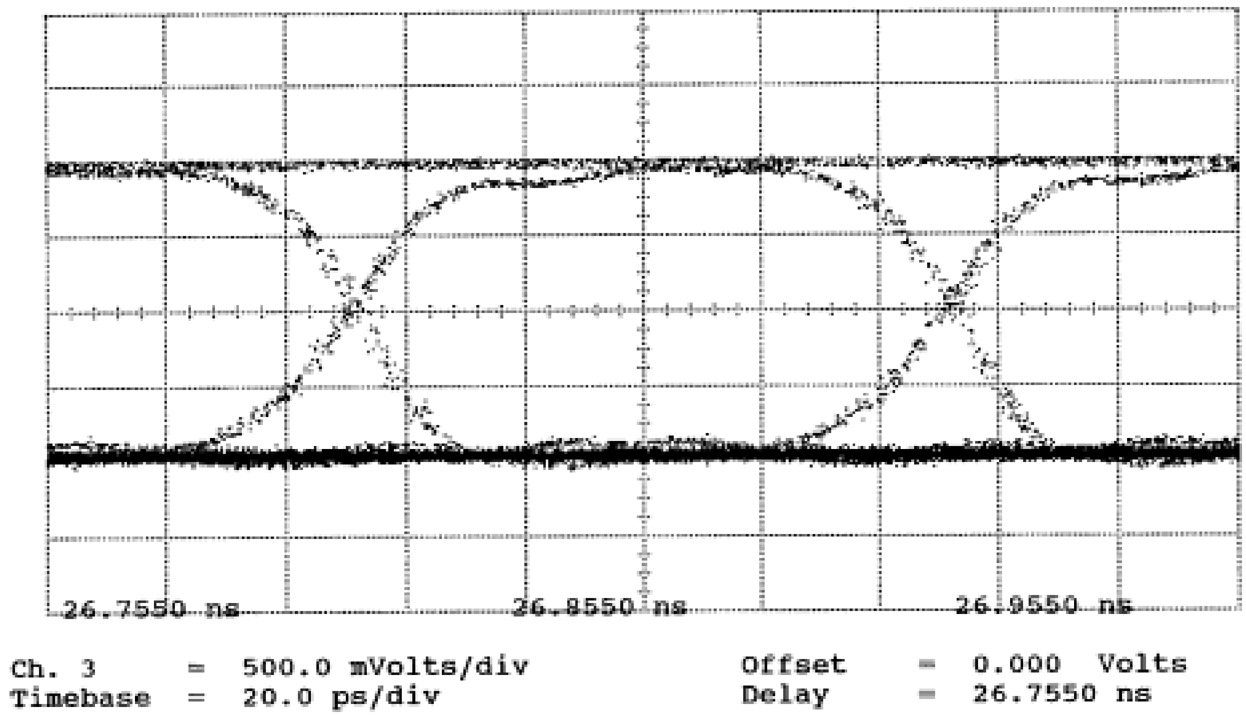


Ch. 3	=	500.0 mVolts/div	Offset	=	0.000 Volts
Timebase	=	20.0 ps/div	Delay	=	26.7570 ns

2^{31}-1 Pattern, 10G rate

Eye Diagram of 1/8 Mark Ratio Quasi-PRBS

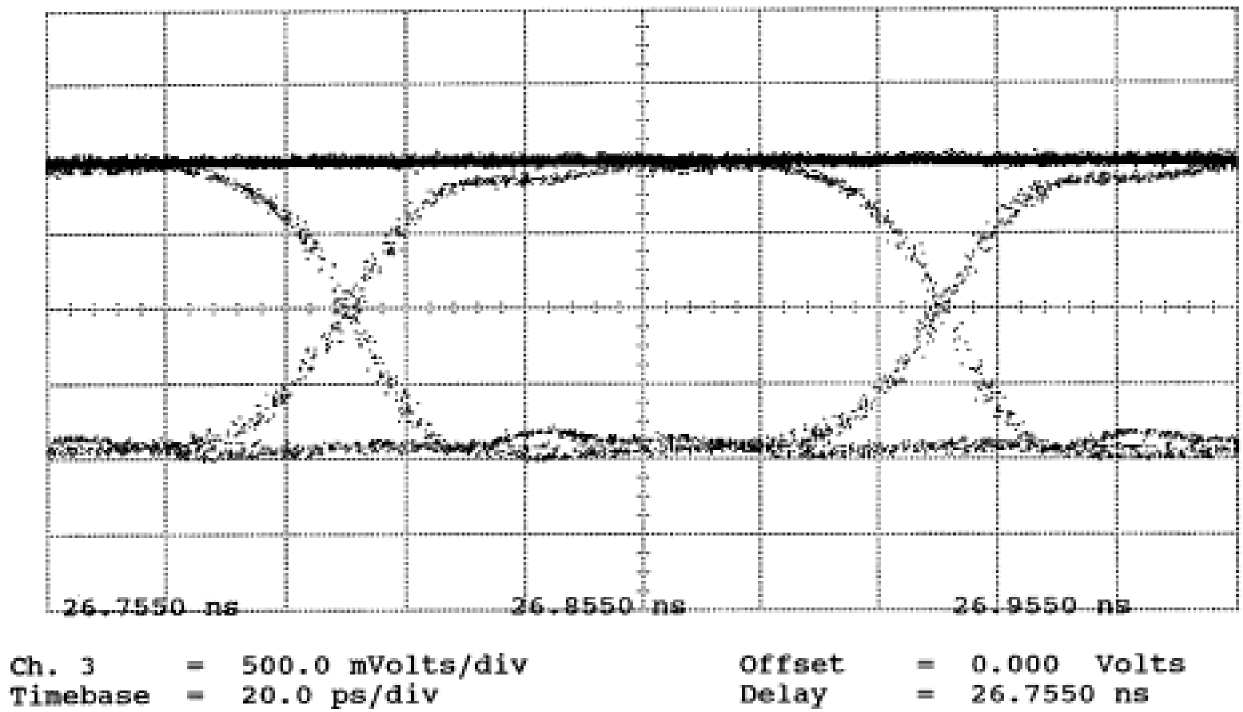
1/8 Mark Ratio



2^{31}-1 Pattern, 10G rate

Eye Diagram of 7/8 Mark Ratio Quasi-PRBS

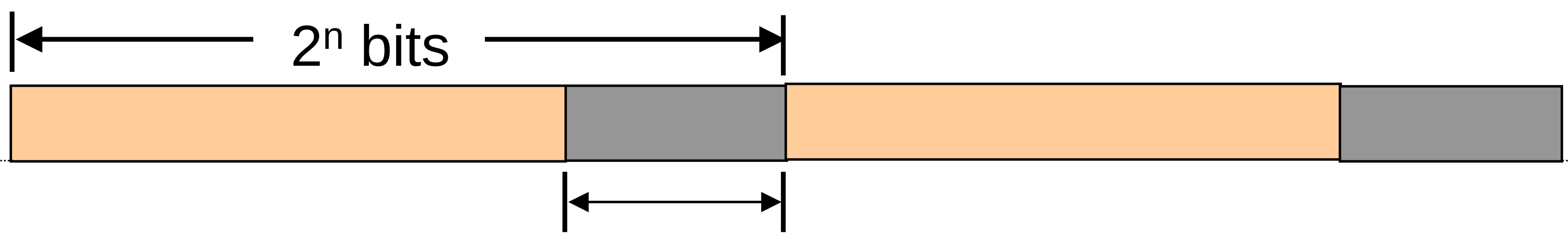
7/8 Mark Ratio



2^{31}-1 Pattern, 10G rate

Zero Substitution Patterns

- **The Zero Substitution (ZS) pattern is similar to a standard PRBS pattern, but it contains a longer maximum string of consecutive ZEROS (longer than n-1).**
  - Length of ZERO string is Variable
  - The patterns are not implemented using the standard PRBS pattern generation circuitry. Rather, they are pre-stored in system memory.
  - Memory resolution restrictions require that the pattern be an even length.
  - Zero Substitution Patterns designed for Testing Clock Recovery Circuits
  - Can be inverted to give Consecutive ONEs string



Consecutive Zeros
Length is User-Selectable

Example of 2^7 Zero Substitution Pattern

Standard 2^7 -1 PRBS Pattern

0 0 0 0 0 0 1 0 0 0 0 1 1 0 0
0 0 1 0 1 0 0 0 1 1 1 1 0 0 1 0
0 0 1 0 1 1 0 0 1 1 1 0 1 0 1 0
0 1 1 1 1 1 0 1 0 0 0 0 1 1 1 0
0 0 1 0 0 1 0 0 1 1 0 1 1 0 1 0
1 1 0 1 1 1 1 0 1 1 0 0 0 1 1 0
1 0 0 1 0 1 1 1 0 1 1 1 0 0 1 1
0 0 1 0 1 0 1 0 1 1 1 1 1 1 1

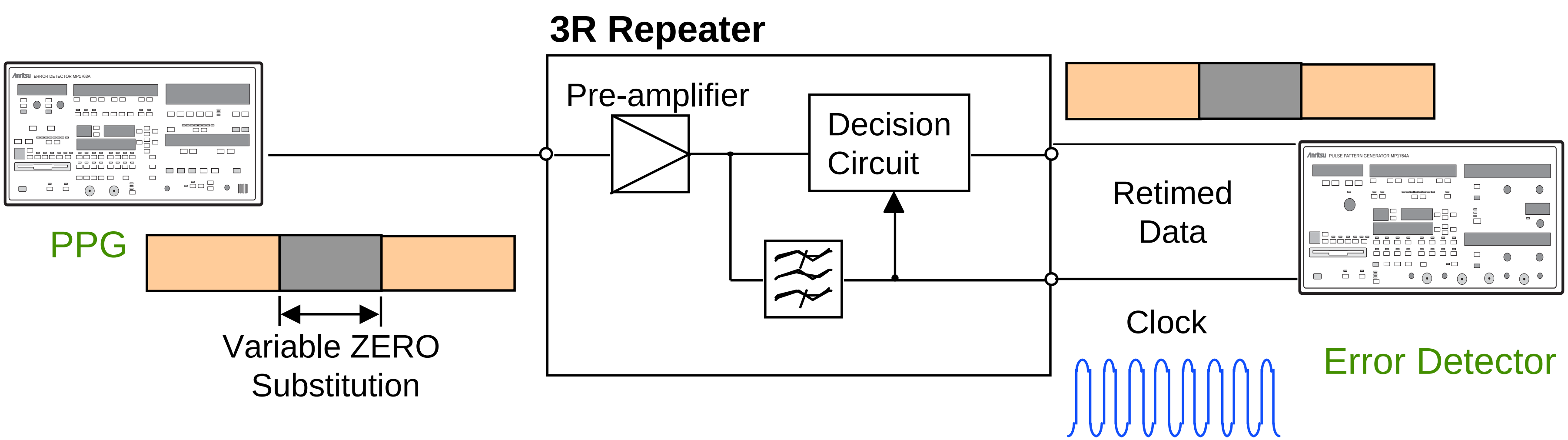
Example of 2^7 Zero Sub Pattern with string of 10 Consecutive ZEROs

0 0 0 0 0 0 0 0 0 0 1 0 1 1 0 0
0 0 1 0 1 0 0 0 1 1 1 1 0 0 1 0
0 0 1 0 1 1 0 0 1 1 1 0 1 0 1 0
0 1 1 1 1 1 0 1 0 0 0 0 1 1 1 0
0 0 1 0 0 1 0 0 1 1 0 1 1 0 1 0
1 1 0 1 1 1 1 0 1 1 0 0 0 1 1 0
1 0 0 1 0 1 1 1 0 1 1 1 0 0 1 1
0 0 1 0 1 0 1 0 1 1 1 1 1 1 1 **1**

Adds an extra 1 at end of pattern

Zero Substitution Pattern Application

Testing Clock Regeneration of a Network Element Receiver



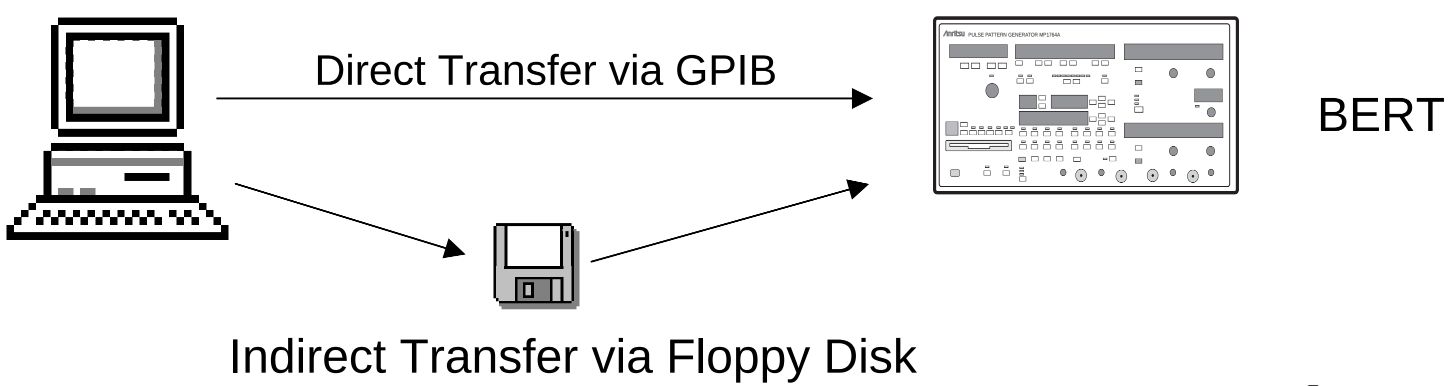
The user can determine the ZERO string length which causes the PLL circuit in the CDR to lose lock.

Programmed (User-Defined) Pattern

- **Programmed or User-Defined patterns are dictated by the user.**
  - Typically, users will program patterns that emulate popular transmission protocols, including:
    - SONET
    - ATM
    - IP
    - Gigabit Ethernet
- **Programmed patterns can be manually entered on the front panel of the BERT or downloaded via GPIB or floppy disk.**

Programmed SONET Frames

- **To facilitate the downloading of lengthy SONET frames, Anritsu developed accessory SONET Frame Editor software.**
  - This softwarehas Default SONET Overhead, Payload
    - Typically, User Changes only a Few Bytes
  - The # of SONET Frames that can be downloaded is limited by BERT Memory Size
    - 8 Mbit Can Hold 6 OC-192 Frames, 26 OC-48 Frames



Programmed Pattern Length Restrictions

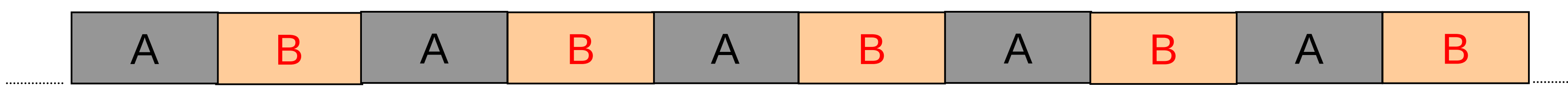
Pattern Length Restrictions: Odd Length Patterns above 65,536 are not allowed in Anritsu 12 Gbit BERT.

Pattern Length	Pattern Resolution
1 to 65,536	1
65,536 to 131,072	2
131,072 to 262,144	4
262,144 to 524,288	8
524,288 to 1,048,576	16
1,048,576 to 2,097,152	32
2,097,152 to 4,194,304	64
4,194,304 to 8,388,608	128

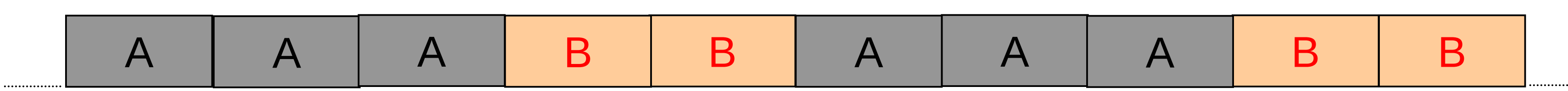
Alternating Patterns

- **Alternating Patterns are a special class of User-Defined pattern that outputs two independent (different content) "A" and "B" patterns.**
- **Number of Repetitions is Settable by the user.**

A: 1 Repetition, B: 1 Repetition



A: 3 Repetitions, B: 2 Repetitions

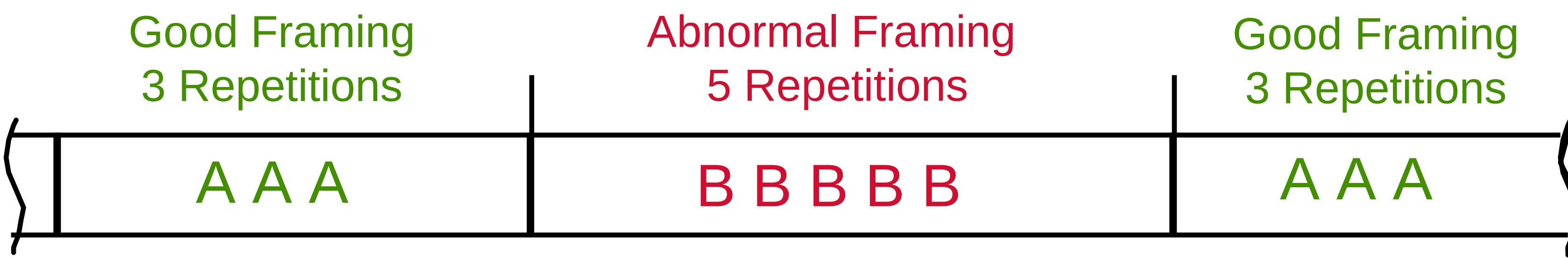


Alternating Pattern Application

An application for Alternating Pattern mode is the verification of a SONET receivers ability to correctly detect alarms.

Example Application: OC-192 "OOF" Alarm Stress Test

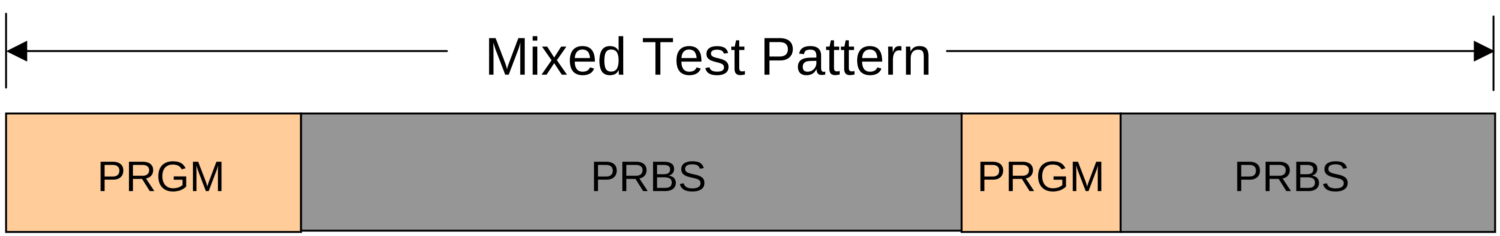
Pattern “A” contains an OC-192 Frame with good framing Characteristics
Pattern “B” contains an OC-192 Frame with bit errors in the framing



This Transmitted OC-192 Pattern will Generate an OOF Condition in a Network element.

Mixed Pattern

- **Mixed Patterns are a Combination of User Patterns and PRBS Patterns.**
  - Useful for Generating SONET, ATM, IP, and other complex Protocol Test Sequences
  - Overhead is generated with Programmable Pattern (PRGM)
  - Payload is simulated with PRBS Pattern
  - Can Interleave Multiple Blocks of PRGM and PRBS Patterns

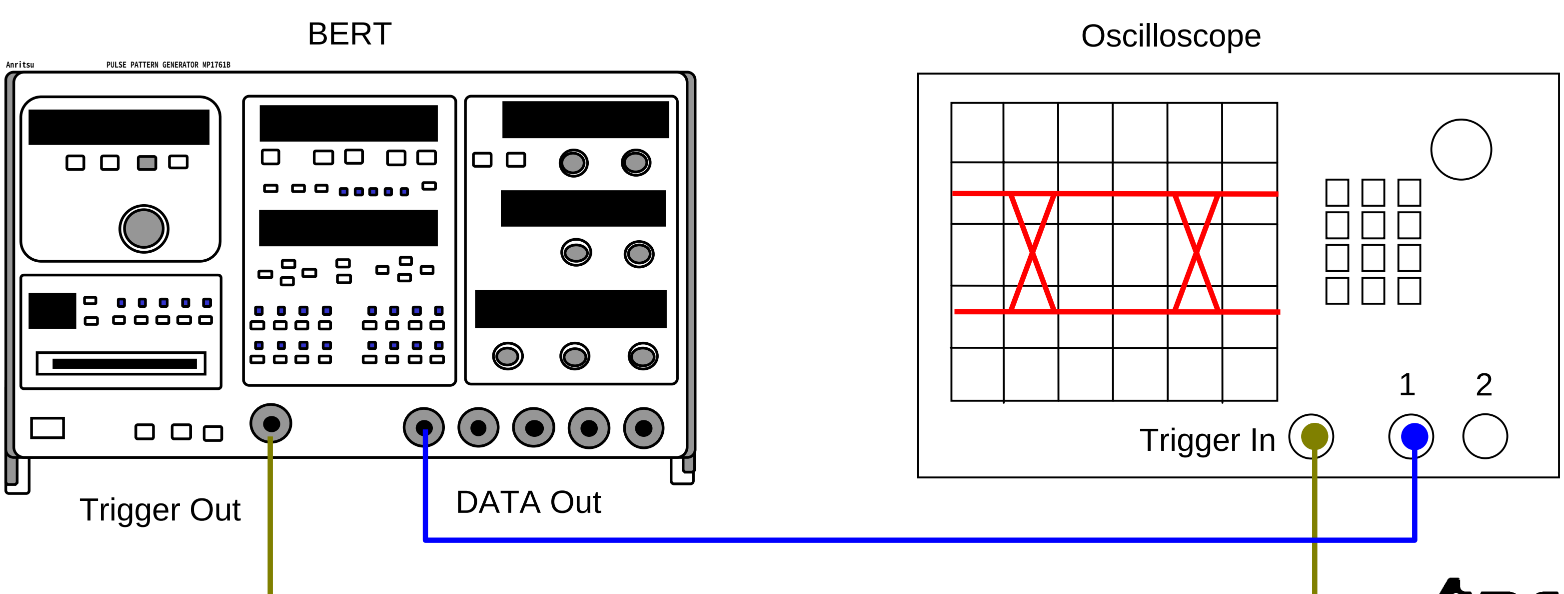


Summary

- **There are two types of Test Patterns:**
  - Pre-Defined Test Patterns
    - PRBS
    - Variable Mark Ratio Quasi-PRBS
    - Zero Substitution
  - User-Defined Test Patterns
    - Programmed (PRGM)
    - Alternating
    - Mixed
- **Test patterns are designed to test the performance of Network Elements.**

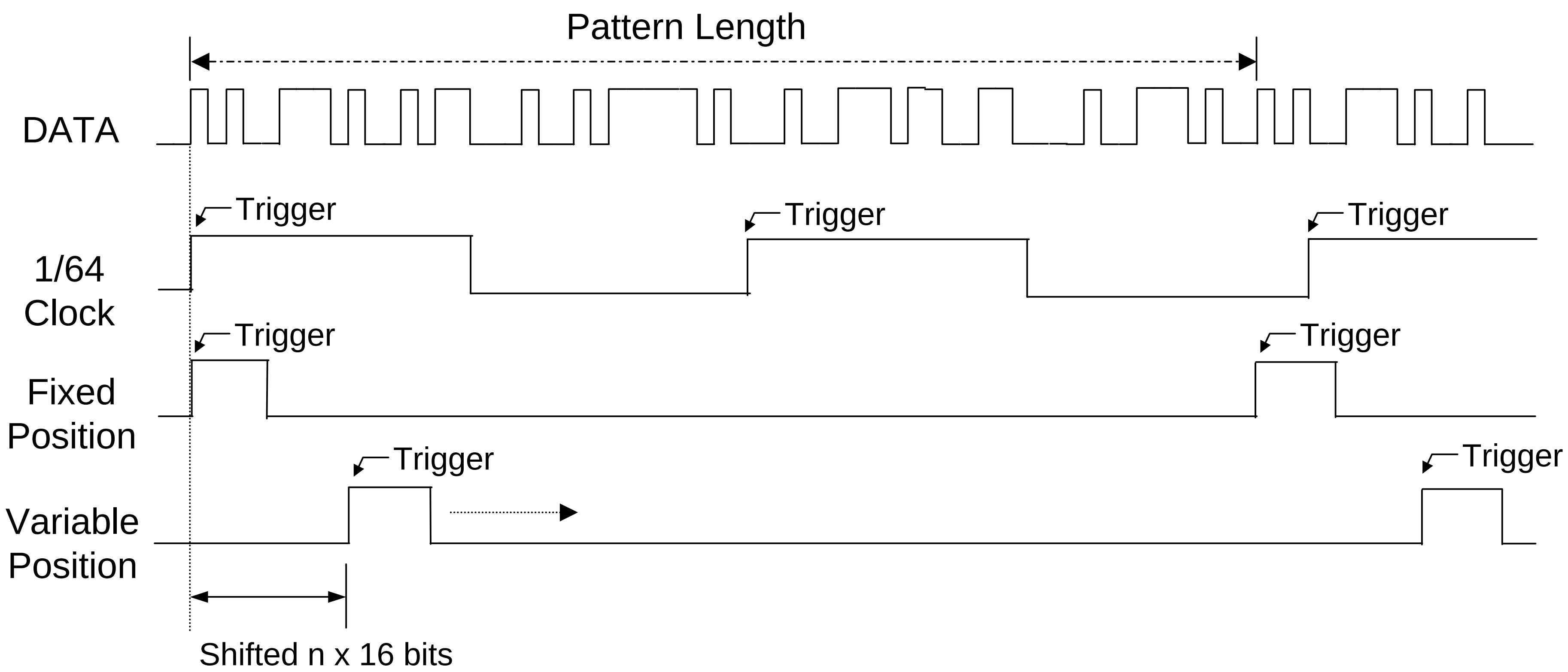
Using BERTs with Oscilloscope

- **BERTs Provide Two Types of Scope Trigger Outputs:**
  - Sub-Rate Clock Output for Generating Eye Diagrams
    - Example: 1/64 Clock, 1/8 Clock
  - Pattern Trigger for Viewing Individual Bit Sequences or Pulse Trains
    - Fixed Position: Trigger aligns with Bit 1 of Pattern
    - Variable Position: Trigger occurs at User-Selected Bit Position in Pattern
- **Anritsu provides Trigger Outputs on both the PPG and ED**



BERT Scope Triggers

Timing Diagram



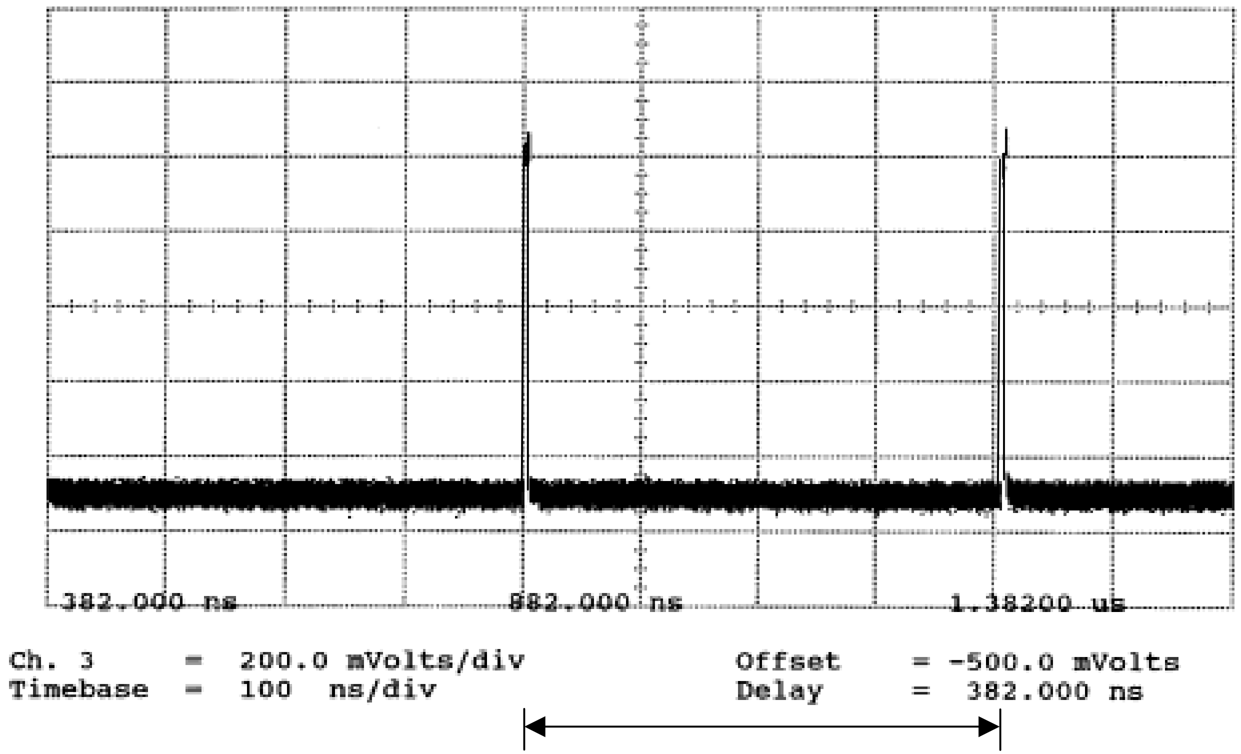
1/64 Clock provides 1 Trigger Every 64 Bits
Fixed & Variable Position provides 1 Trigger Every Pattern Repetition

Pattern Trigger Repetition Period

- **Fixed Position & Variable Position Trigger Repetition Period Depends on Pattern Length**
  - PRBS Pattern the Trigger Occurs Once Every 32nd Pattern Repetition.
  - Zero Substitution Pattern the Trigger Occurs Once Every Pattern Repetition
  - User Pattern > 65,535 Bits the Trigger Occurs Once Every Pattern Repetition
  - User Pattern < 65,535 Bits the Trigger Occurs Once Every Pattern Repetition if Pattern is a Multiple of 128 Bits. Otherwise, Trigger Occurs "At the Least Common Multiple Between 128 and Pattern Length".
    - For Example: For a Pattern 200 bits Long, Trigger Occurs every 3200 Bits.

Note: In Fixed Position/Variable Position Mode, Scope Update Times Can be Very Slow for Long PRBS (n > 9) and PRGM patterns.   For Example, a 2^{31}-1 Pattern has a Trigger Interval of 6.87 Seconds @ 10 Gbit rate.

Example of Pattern Trigger Repetition Period

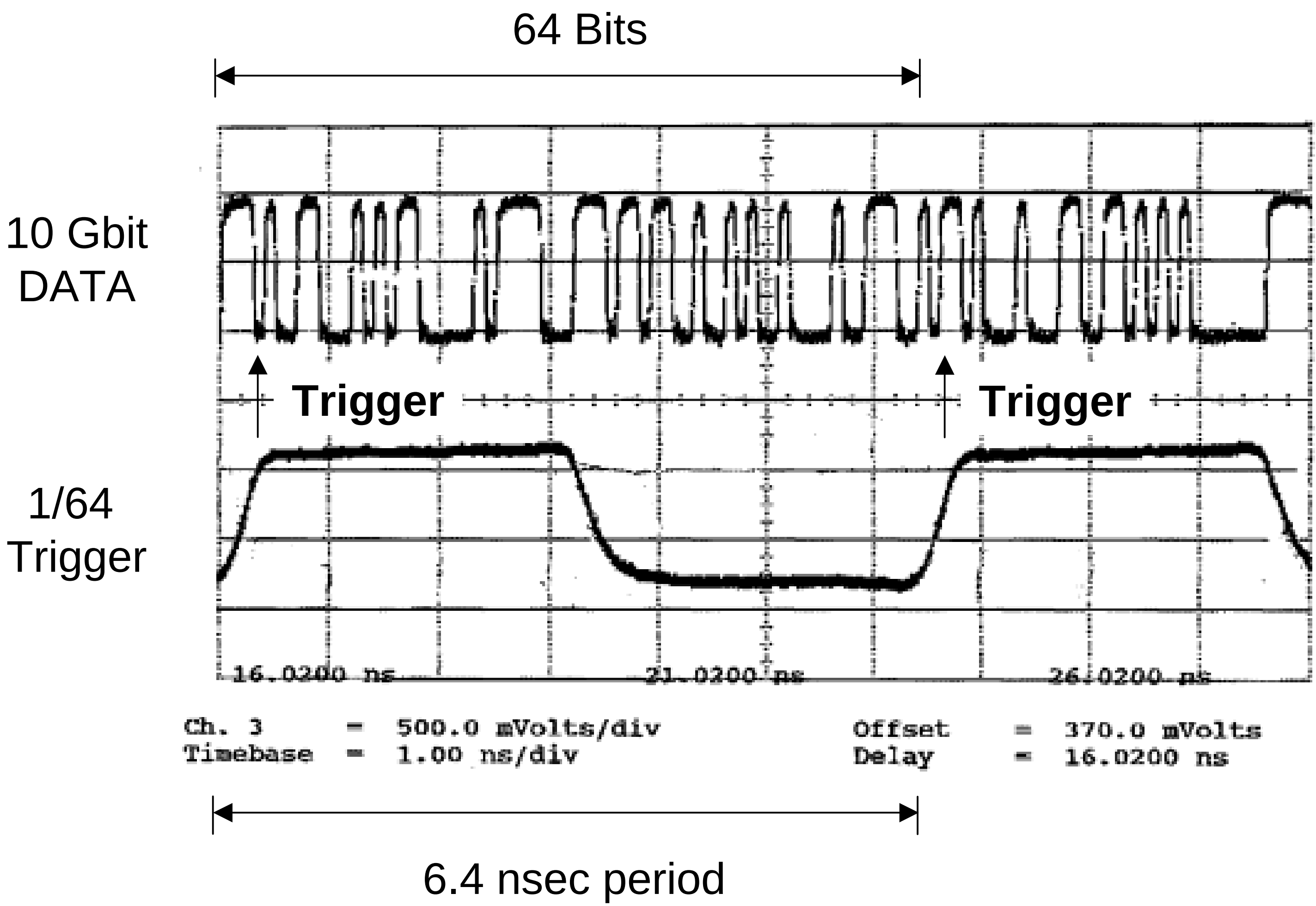


Trigger Repetition Period

Trigger Repetition Period for PRBS 2^7-1 @ 10 G= 127 Bits x 100 ps x 32 = 406 ns

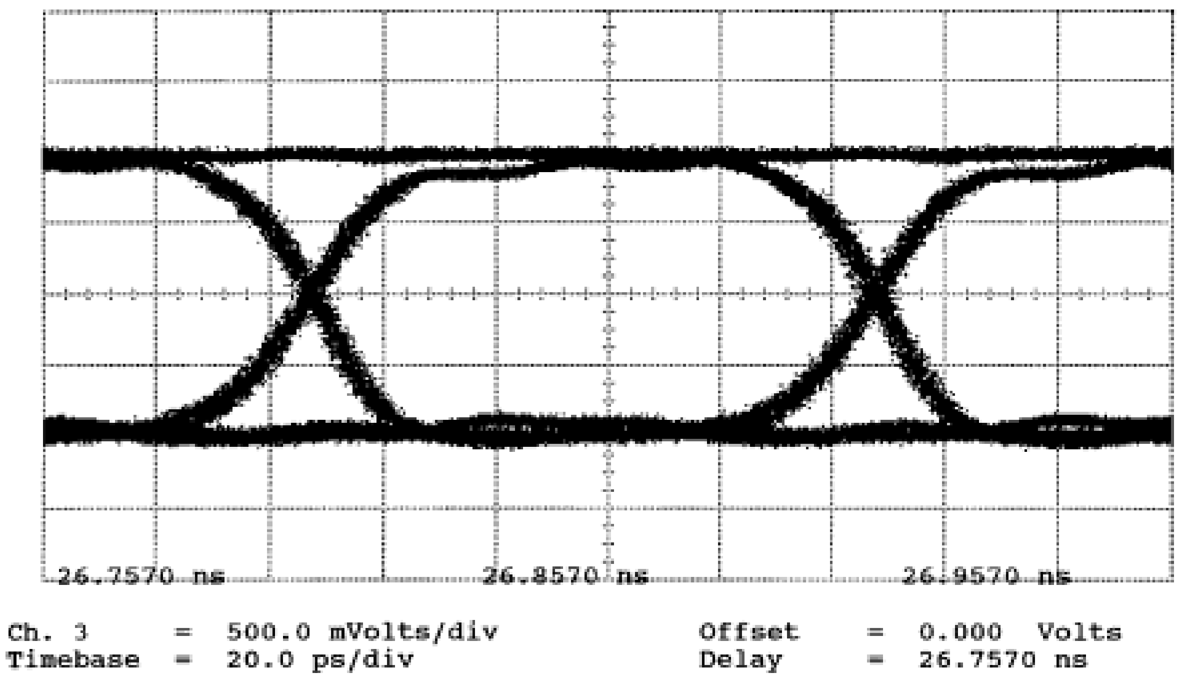
Sub-Rate Clock Trigger

Trigger occurs every 64 bits



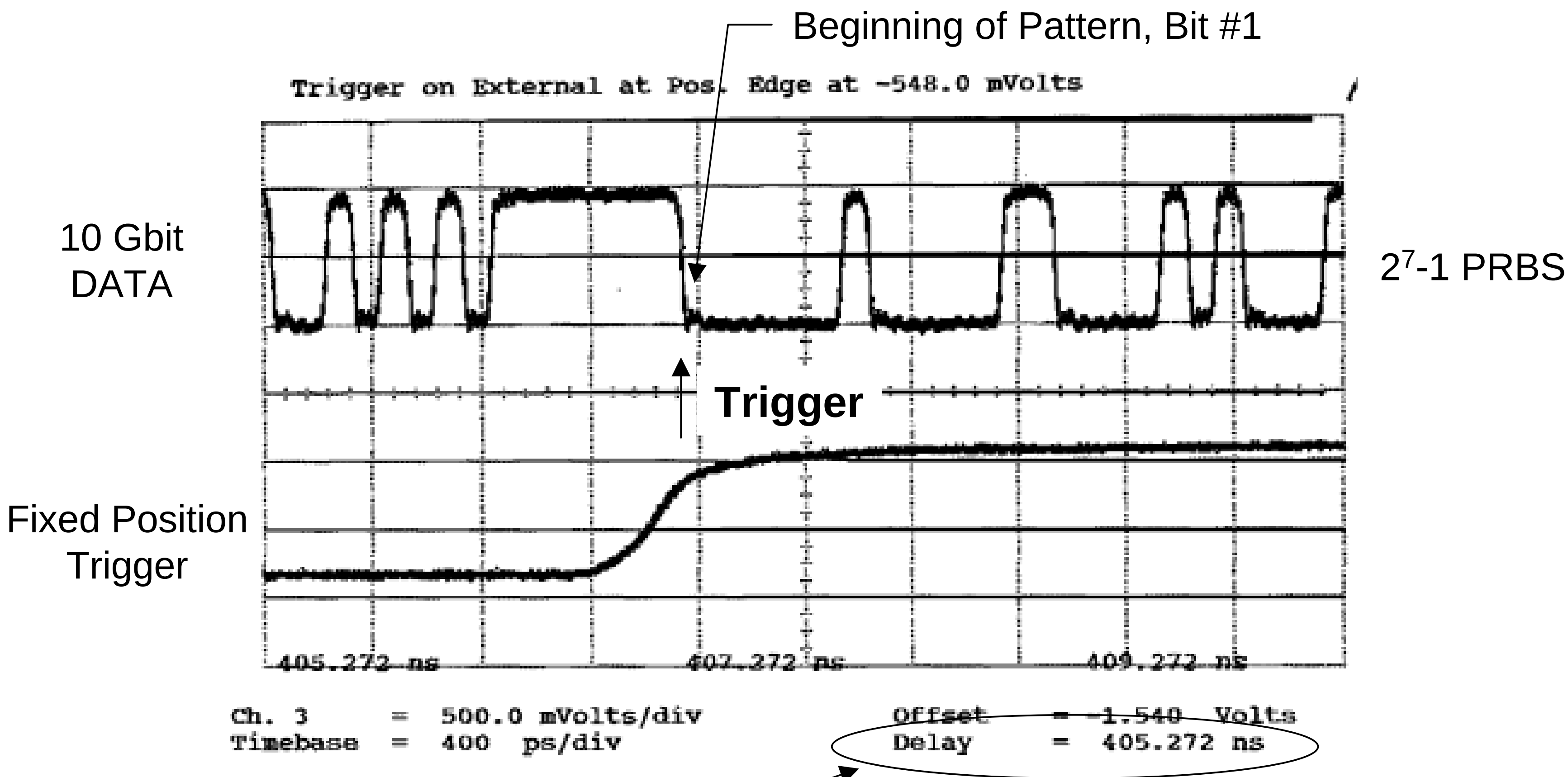
Eye Diagram

10 G Eye Diagram Generated with Sub-Rate Trigger (1/64 Clock)



Fixed Position Pattern Trigger

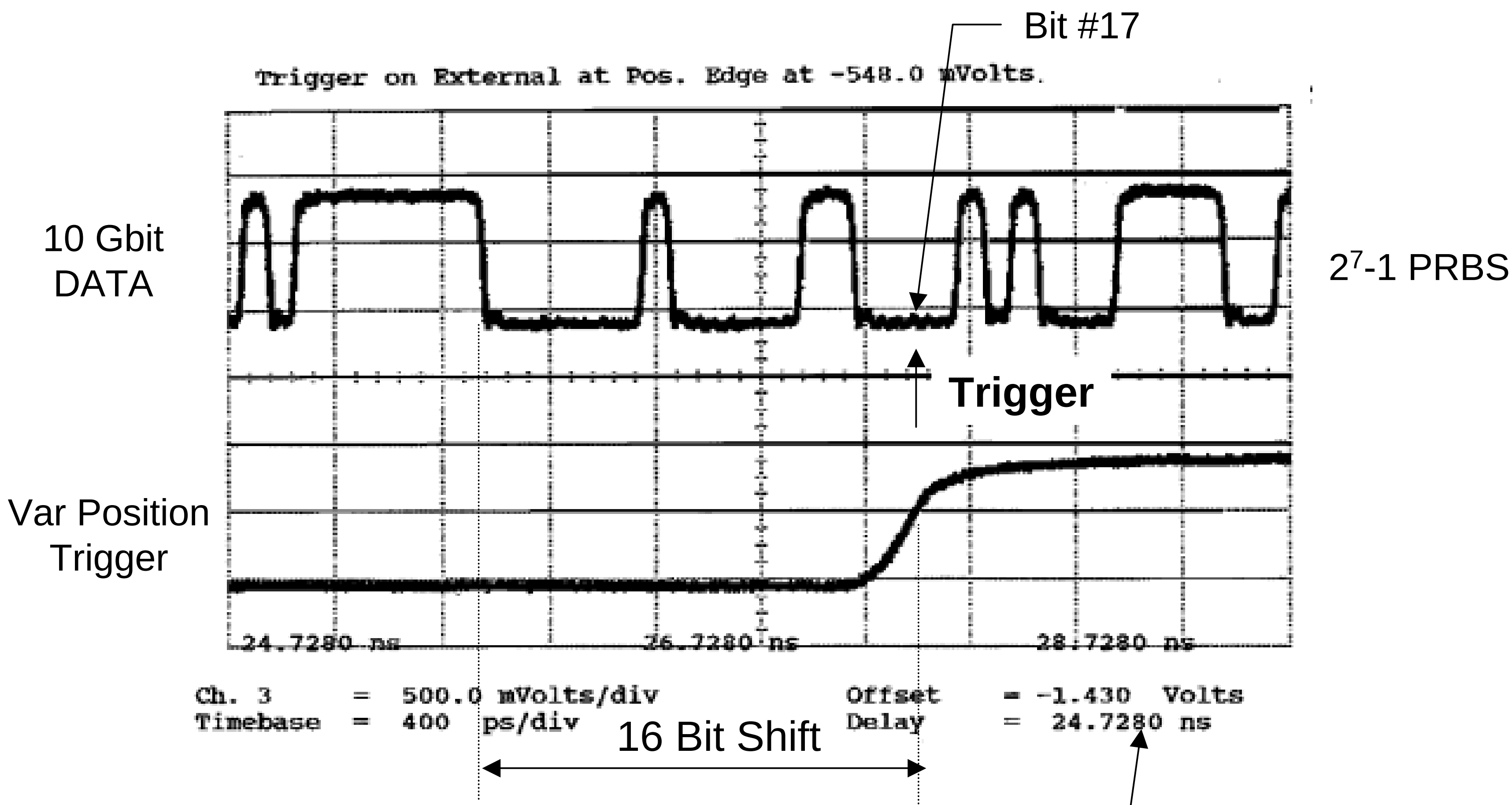
The trigger rising edge corresponds to bit 1 in the pattern sequence.



Will need to adjust delay to display bit 1 on scope

Variable Position Pattern Trigger

In this example, the variable position trigger was set to bit 17.



Scope Delay Adjustment Can Also Be Used to View Different Portions of Pattern

Scope Limitations

- **Viewing a high speed waveform requires adequate scope bandwidth.**
  - A bandwidth of twice the maximum bit rate is recommended for viewing DATA.
- **Viewing the CLOCK signal requires a bandwidth of 3 times the bit rate.**
  - The scope bandwidth should be greater than 30 GHz for viewing 10 Gbit DATA/CLOCK
- **Low sampling speeds and sampling noise limit a scopes ability to make accurate Margin measurements and Q measurements.**
- **Use Attenuator on Scope Input if Voltage Exceeds 1 Vpp**
  - ⇨ Prevents Non-Linear Response

Note: Use Good Quality Coax Cables Rated for Twice the Clock Rate

Synchronization

- **Synchronization is the alignment of the Reference Pattern in the Error Detector with the Incoming DATA Pattern.**
- **Synchronization is Required before valid BER Measurements Can Begin**
- **Synchronization Time Depends on Pattern Length & Bit Rate**
  - Longer the Pattern ⇨ Longer the Sync Time
  - Lower the Bit Rate ⇨ Longer the Sync Time due to increased bit periods
- **Sync Times can range from μs to minutes**

Incoming DATA ⇦ 1000111100110100111010001111001101001111

Reference Pattern 0110100111010001111O

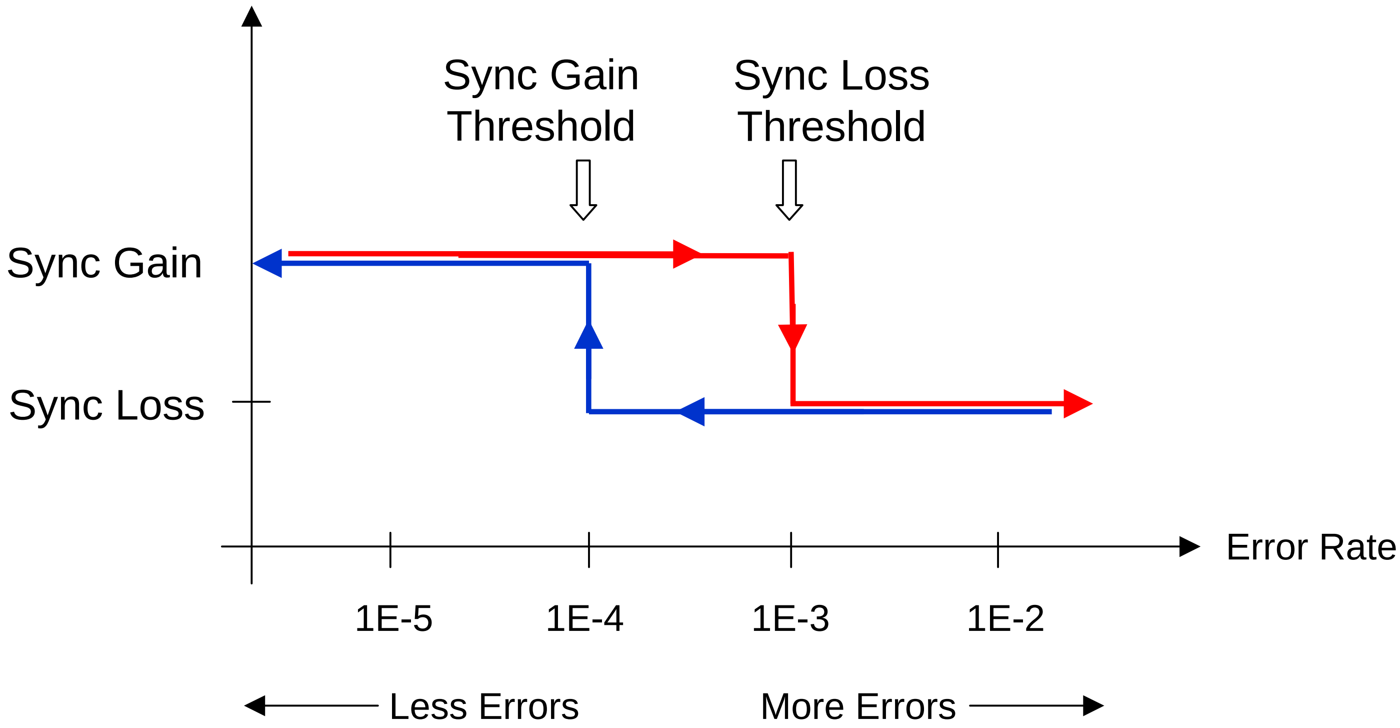
0110100111010001111O

Synchronization Threshold

- **Synchronization Threshold is the Nominal Error Rate at which the Error Detector Gains Sync and Loses Sync**
- **Generally, BER Measurements cannot be made at Errors Rates Exceeding the Sync Threshold**
  - Sync Thresholds are adjustable in the range 10^{-2} to 10^{-8}.
  - 10^{-2} is a "relaxed" Sync criteria. False Sync is possible at this setting.
  - 10^{-8} is a "rigid" Sync criteria. False Sync is unlikely at this setting
- **Some BERTs have an Internal Sync Threshold mode (INT) for User Patterns. The Sync Threshold varies automatically with Pattern Length**
- **Some BERTs allow separate setting of the Sync Gain Threshold and the Sync Loss Threshold. In other BERTs, the Sync Gain Thresholds and Sync Loss Thresholds are Coupled Together, i.e. cannot be independently set.**

Sync Gain/Loss Thresholds

Example: Sync Gain Threshold set to 1E-4, Sync Loss Threshold Set to 1E-3



Hysteresis is used to Avoid Unstable Sync Loss/Gain Conditions

Synchronization Methods

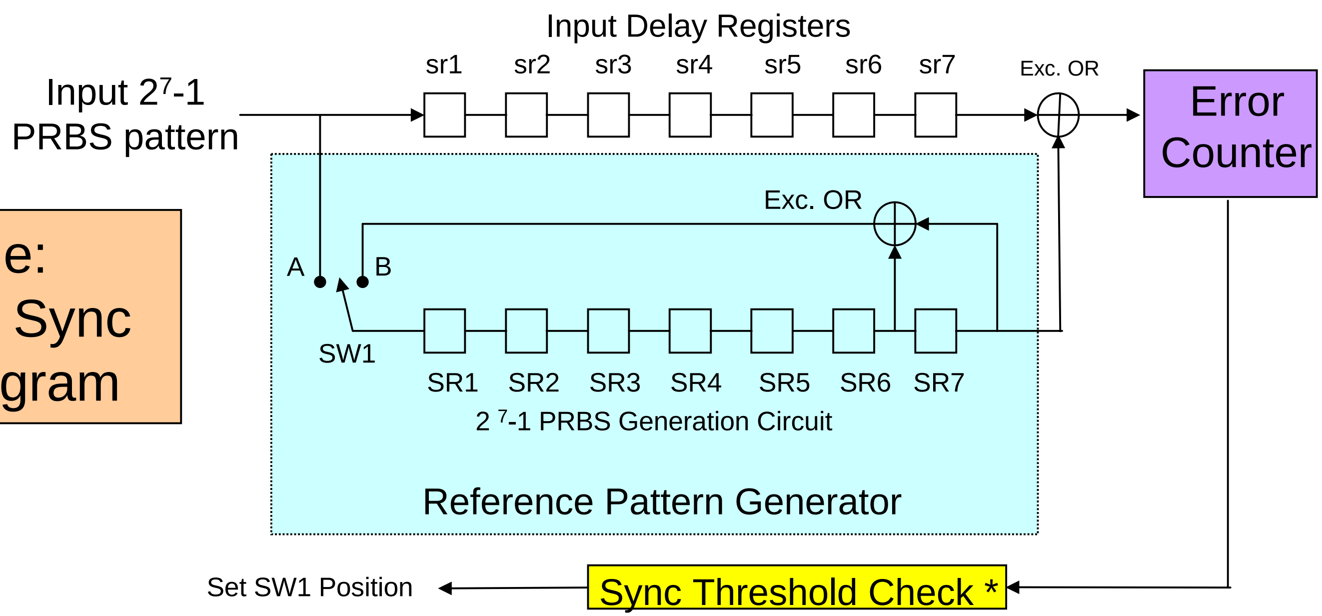
- PRBS Sync
- Normal Sync
- Frame Sync
- Quick Sync

Normal, Frame, and Quick Sync apply for Programmed Patterns (NOT PRBS Patterns)

PRBS Sync

- **The sync process for PRBS patterns involves generating the ED reference pattern from the incoming DATA**
- **Sync time is Very Fast, on the order of a micro-second for 10 Gbit.**

Example:
2^7-1 PRBS Sync
Circuit Diagram

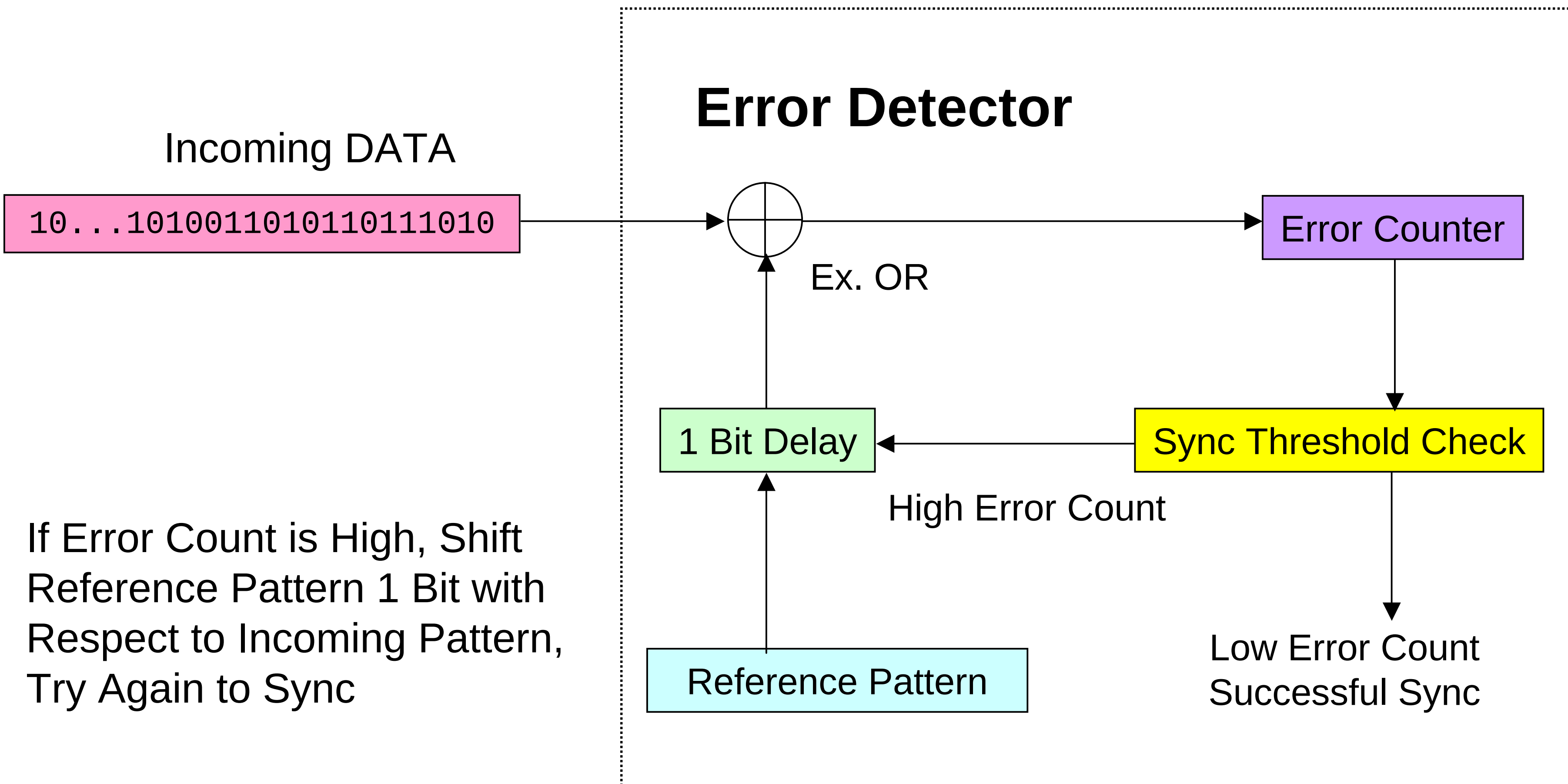


* If Error Count is low, keep switch in position B. Successful Sync.
If Error Count is high, return switch in position A and Re-Sync.

Normal Sync

- Normal sync compares the entire Reference Pattern with Incoming Data.
- Reference Pattern is Shifted with Respect to Incoming Data Until Match occurs
- The Chance of Sync occurring is 1/(Pattern Length)
- Sync Time can be Long (MINUTES !) especially for Long Patterns
- Normal Sync is Available for User, Alternating, and Zero Substitution Patterns

Normal Sync



If Error Count is High, Shift Reference Pattern 1 Bit with Respect to Incoming Pattern, Try Again to Sync

Normal Sync

First Sync Attempt

```
Incoming DATA       ←········1100 0010 1001 0111
                             ↑↑↑.....
Reference Pattern            1111 0000 1010 0101
```

HIGH ERROR COUNT
Try Again to Sync

Second Sync Attempt

```
Incoming DATA       ←········1100 0010 1001 0111
                             ↑↑↑.....
Reference Pattern            1110 0001 0100 1011
```

HIGH ERROR COUNT
Try Again to Sync

Third Sync Attempt

```
Incoming DATA       ←········1100 0010 1001 0111
                             ↑↑↑.....
Reference Pattern            1100 0010 1001 0111
```

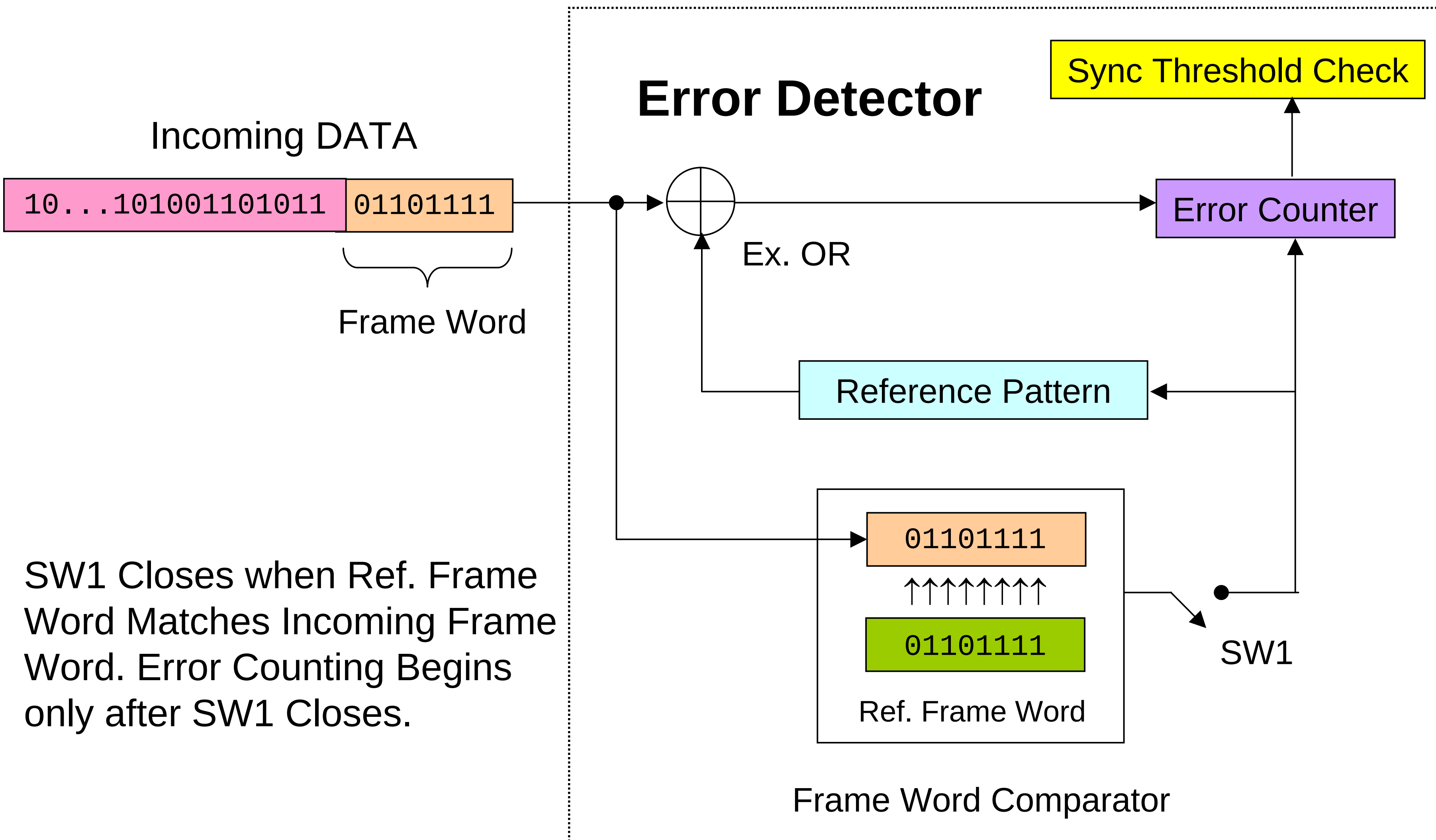
NO ERRORS
Successful Sync !

Underlined bits are errors

Frame Sync

- Frame Synchronization involves matching a pre-defined "unique" Frame Word at the beginning of the reference pattern with the similar Frame Word in the incoming pattern.
- Sync Time is Faster than Normal Sync for Framed Patterns.
- Frame sync is Useful for Rapid Sync on SONET/SDH Frames
- Available for User, Alternating, and Zero Substitution Patterns

Frame Sync



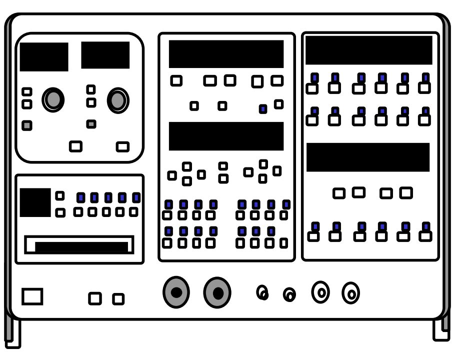
SW1 Closes when Ref. Frame Word Matches Incoming Frame Word. Error Counting Begins only after SW1 Closes.

Quick Sync

- During quick sync the Incoming Pattern Is Stored In Error Detector and Becomes Reference Pattern
- The Error Detector does not need a pre-stored reference pattern; only prior knowledge of the pattern length is required.
- Sync times are very rapid, on the order of us for 10 Gbit rates.
- Quick Sync is useful for sync on long patterns (> 100 kBit) and Burst Data.
- Available for User and Zero Substitution Patterns
- Use with Caution…Can give misleading results

Quick Sync

Step 1: Enter Pattern Length, N, into Error Detector
Step 2: Select Quick Sync
Step 3: Error Detector Captures next N bits and stores them as the Reference Pattern
Step 4: Error Detector Compares Next N Incoming Data Bits and Compares them to Reference



Error Detector

Example: N = 16

Compared to Reference Pattern

←·······1111 0000 1010 0101 1111 0000 1010 0101 1111 0000 ..

Stored as Reference Pattern

Margin Measurements

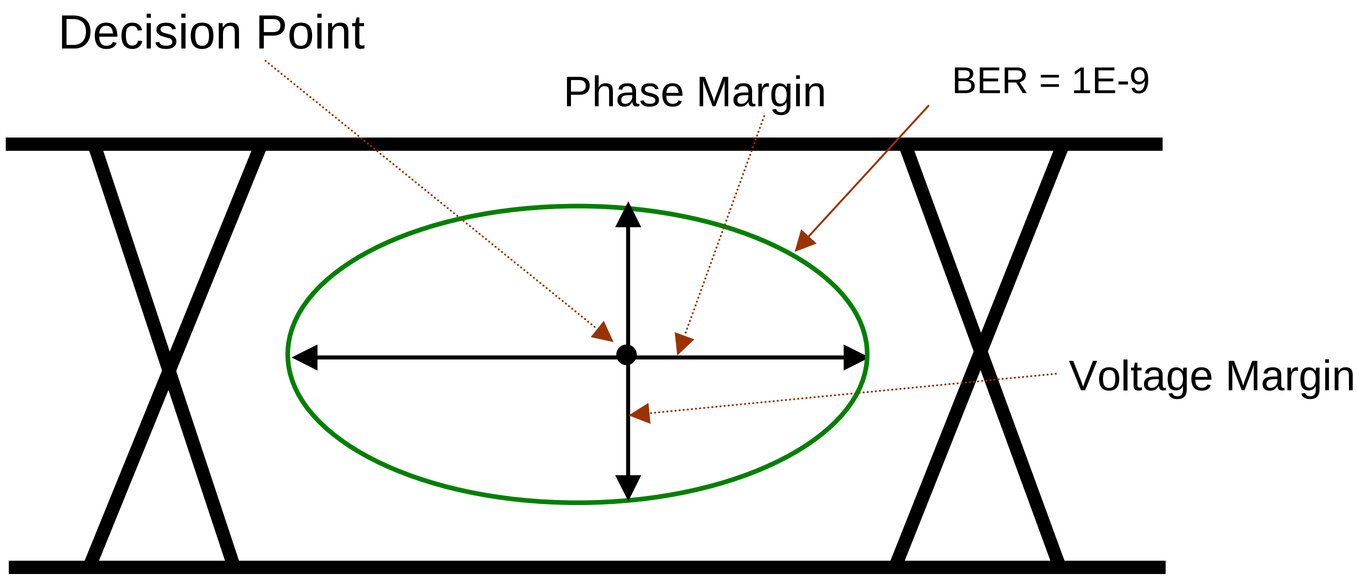
- **Threshold and Phase Margin measurements are important for predicting system performance. Generally, the higher the margins, the lower the system BER.**
- **Three Types of Margin Measurements can be made AUTOMATICALY with BERTs:**
  - Margin at a Decision Point
  - Eye Contour Maps*
  - Q Measurements*

* BERT May require external software to generate Eye Contour and Q Measurement. MP1763/64 12.5 G BERT requires MX2210A accessory software

Margin at a Decision Point

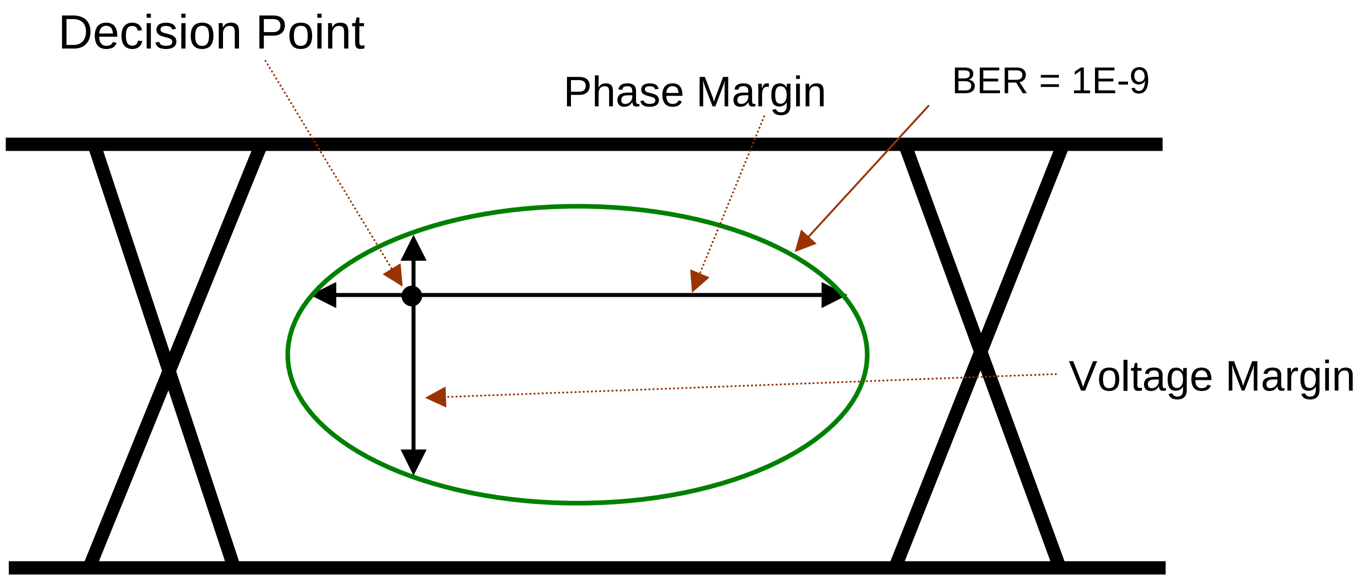
- All Anritsu BERTs Provide Automatic Margin at a Single Decision Point measurements
- This measurement provides a "fast and dirty" assessment of the margin. Testing time is typically 10 seconds.
- Measurement Procedure:
- Pre-Select Decision Point by adjusting Threshold and Delay.
- Select Error Rate Criteria
- Select Margin Measurement Start
- BERT Automatically Adjusts Threshold Up/Down, Delay Left/Right to Determine Margin Values
- Threshold Margin is given in Units of mV pp, Phase Margin is given in Units of ps pp
- Measurement takes about 10 seconds

Margin at a Decision Point



Example 1: 10 Gbit Rate, 1 Vpp DATA Input
Voltage Margin = 720 mVpp @ 1E-9
Phase Margin = 80 ps pp @ 1E-9

Margin at a Decision Point



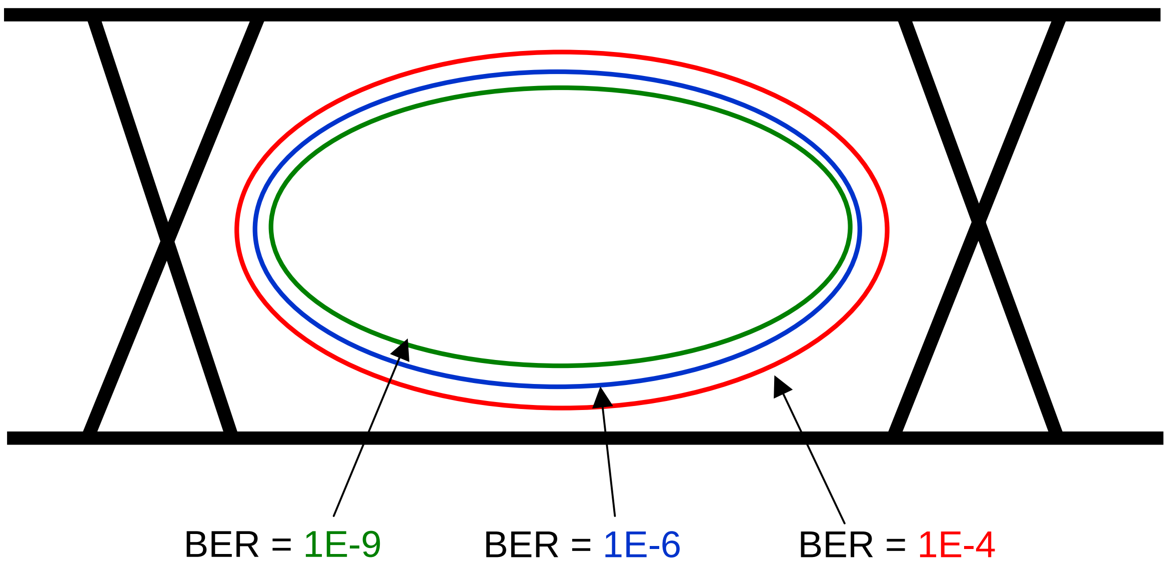
Example 2: 10 Gbit Rate, 1 Vpp DATA Input
Voltage Margin = 600 mVpp @ 1E-9
Phase Margin = 70 ps pp @ 1E-9

NOTE: Margin measurement can be of limited value if Decision Point is not near the eye center

Eye Contour Maps

- **Eye Contour Maps are An Extension to *Margin at a Decision Point* Measurements. Multiple Margin measurements are taken, creating a Contour**
- **Measurement Procedure:**
  - **Set Initial Decision Point. Position is not Critical**
  - **Select Number of Contours to be plotted (number of Error Rates)**
  - **Select Phase Adjustment Resolution in ps. This determines the number of points in contour**
  - **Press Start**
  - **For a given Phase Value, Threshold Is Adjusted Up/Down until reaching the designated Error Rate.**
  - **Plot Points**
  - **Repeat Threshold Adjustment Process at different Phase Values**
  - **Measurement Time Depends on Bit Rate, Phase Adjustment Resolution, Number of Contours**

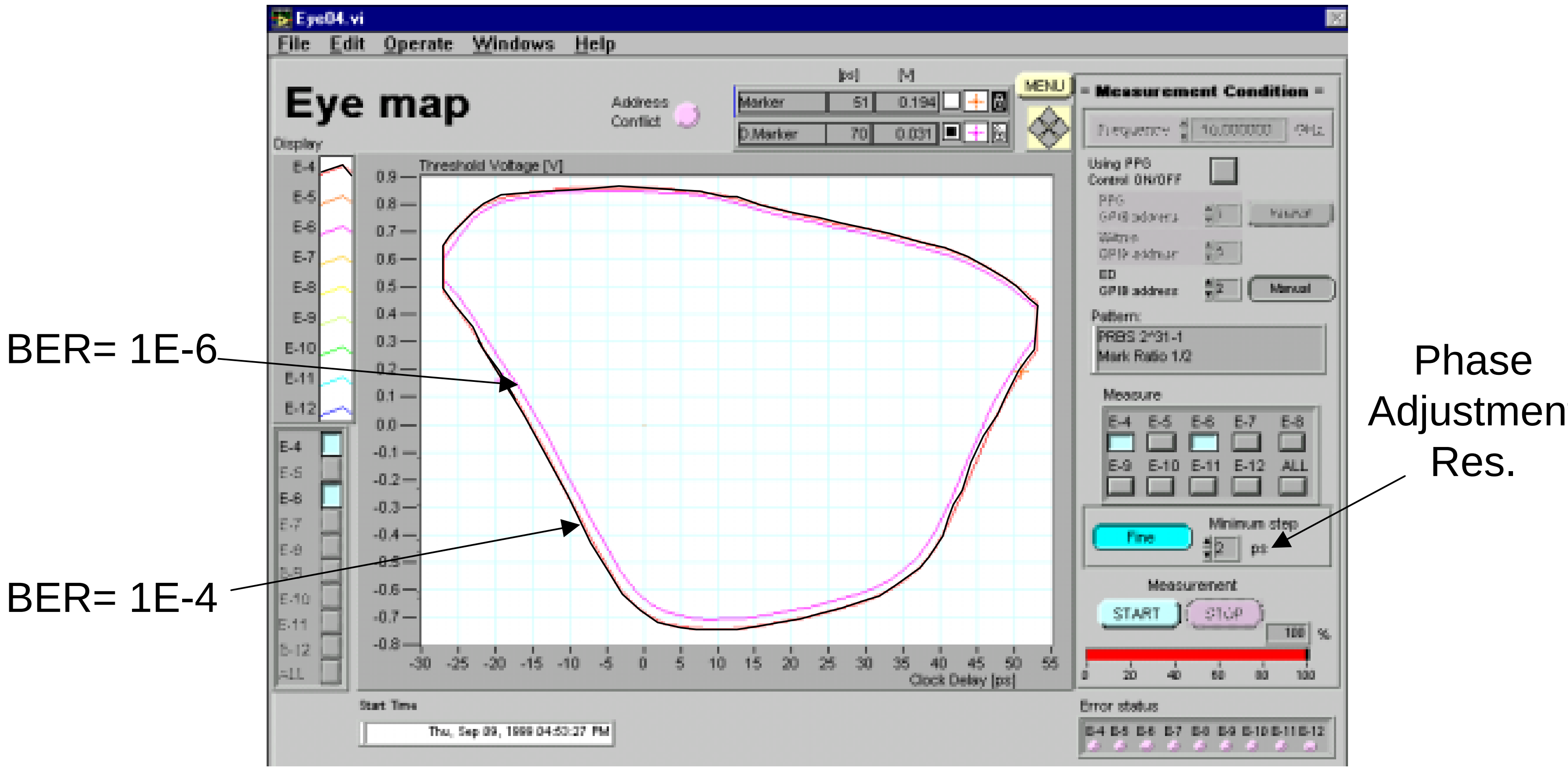
Eye Contour Map



Selectable Error Rate Range is 1E-4 to 1E-12 in 12.5 G BERT software. Lower Error Rates take longer time to complete.

Eye Contour Map Measurement Example

Conditions: 10Gbits, 2Vpp, 0 V Offset, 2^{31}-1 PRBS



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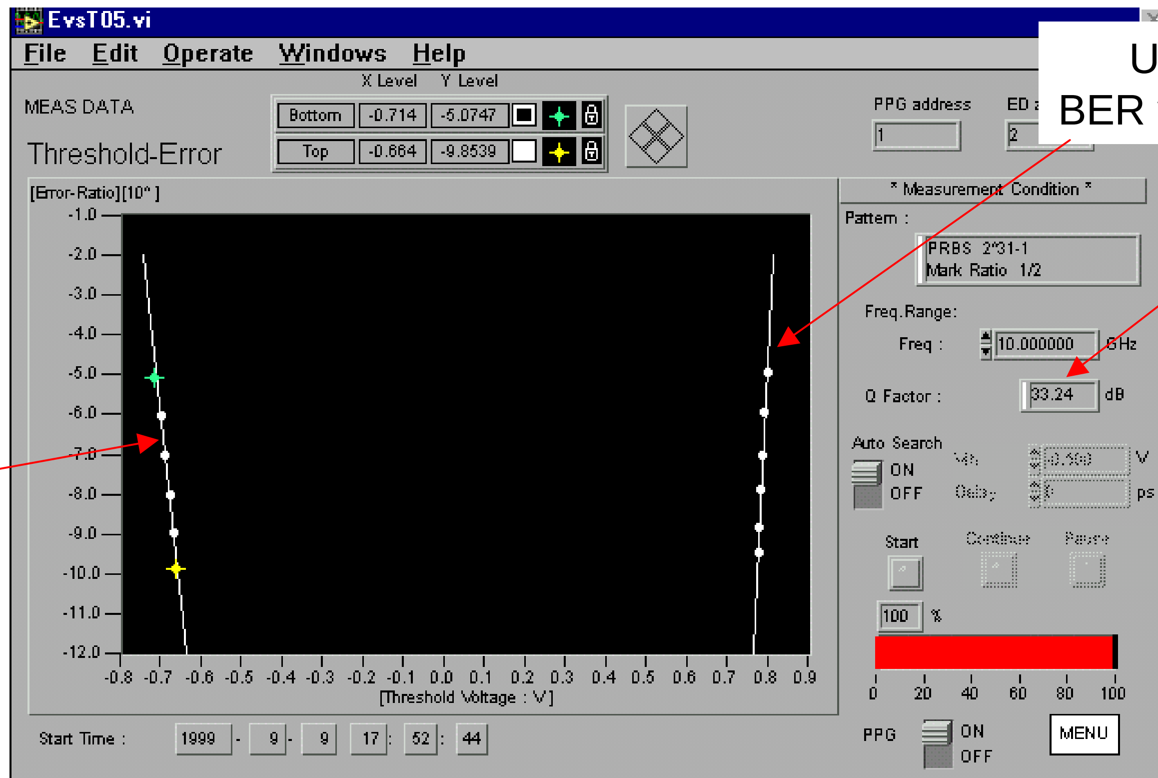
Q Factor Measurements

- Q Factor is a Quantitative Measure of the Quality of the Eye. The Higher the Q, the Less Noise on the Upper and Lower Rails. The Q factor is Useful for predicting very Low Error Rates.
- Measurement Procedure:
- Pre-Select a Decision Point
- Hold Phase Constant. Adjust Threshold Upward. Plot BER vs. Threshold values in range 1E-5 to 1E-10. Curve Fit to Generate Upper Rail BER vs. Threshold Line.
- Adjust Threshold Downward. Generate Lower Rail BER vs. Threshold Line
- Calculate μ_1, μ_0, σ_1, σ_0
- $Q = 20 \text{ Log } (\mu_1 - \mu_0)/(\sigma_1 + \sigma_0)$
- Measurement takes a few minutes

Q Factor Measurement Example

Conditions: 10Gbits, 2Vpp, 0V Offset, 2^{31}-1 PRBS



Upper Rail
BER vs. Threshold

Q Factor

Lower Rail
BER vs. Threshold

Data Taken with MX2210A and MP1763B/64A Back-to-Back

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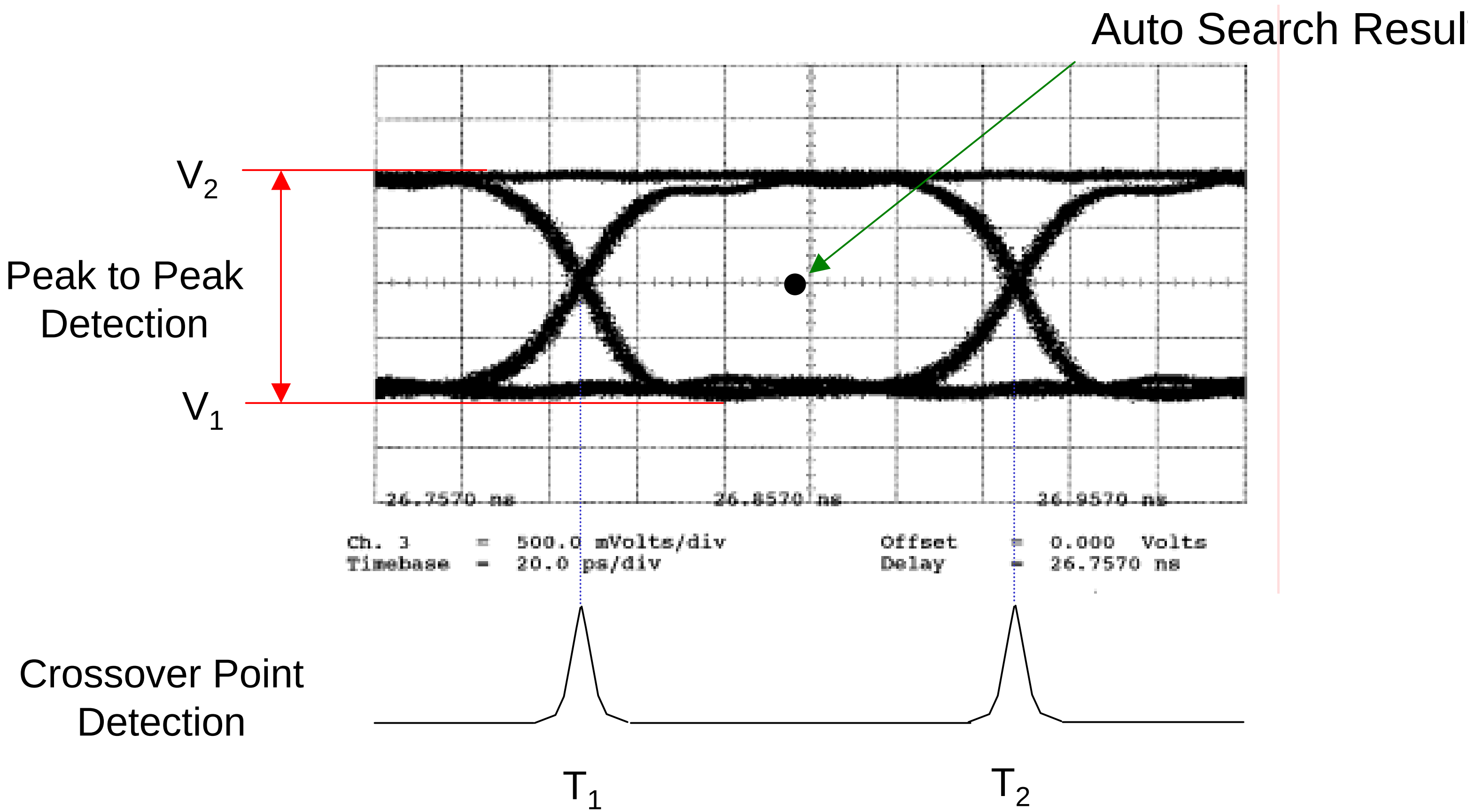
Auto Search

- **Auto Search is an Error Detector Function which automatically Locates the "Center" of the Eye**
  - Auto search automatically Adjusts both Threshold and Phase
  - Auto Search Time is about 10 Seconds
  - Provides good "First Cut" Decision Point Values.
  - MAY NOT FIND OPTIMUM CENTER, especially if there is asymmetry is the Eye Shape. Manual Adjustment will provide better results.
- **Threshold Location is determined by Peak to Peak Detection Circuit. Measure Peak Peak Voltage of Incoming Signal, divide by 2.**
- **Phase Location is determined by Crossover Detection Circuit. Measure difference between adjacent crossover peaks, divide by 2.**

Auto Search

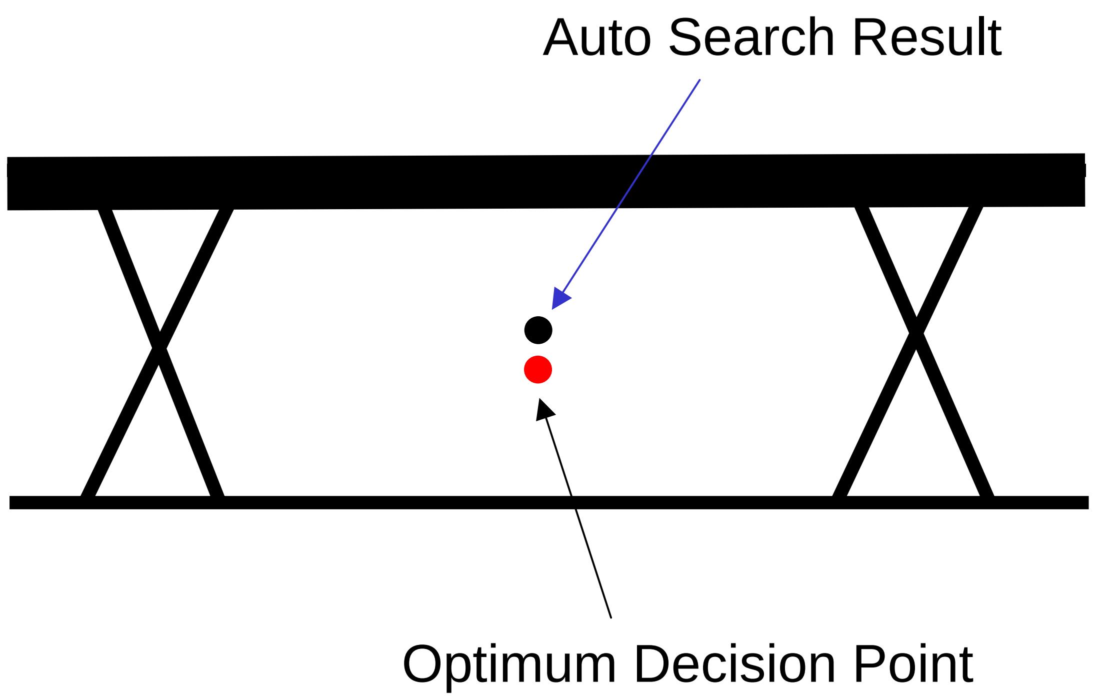


Auto Search Threshold = $(V_2 - V_1)/2$

Auto Search Phase = $(T_2 - T_1)/2$

Auto Search Limitations

Example: Asymmetric Eye due to Noise on Upper Rail



Masking

- **Masking refers to selecting portions of a pattern that will be ignored in measuring BER.**
  - Masks can be useful for tracking down pattern dependent errors. The user can access the portions of the pattern that are contributing to errors.
- **Two Types of Masks**
  - Block Mask: Masks a group of consecutive Bits. For 12.5 G BERT, the Block Mask is 32 bits.
  - Bit Mask: Masks one out of every N bits. For 12.5 G BERT, N= 32.
- **Multiple Block Masks and Bit Masks can be used Simultaneously, allowing user to Mask all but 1 bit.**

Block Mask Example

Block Mask Example: 128 Bit Pattern Length
Mask Applied to Bits 65 to 96

Incoming DATA ←
01010011111101101100110010100010 10111010011010101110100011010110
10000100010101110111111000001101 00101111111100011001101001010011

Ref. Pattern ←
01011011111101101100110010100010 10111010011010101110100011010110
10000110010100110110111000101101 00101111111100011011101001010011

MASK ON:
Measured Error Count = 2
Measured Error Rate = 2 / 96 = 2.1E-2

MASK OFF:
Measured Error Count = 6
Measured Error Rate = 6 / 128 = 4.7E-2

Bit Window Example

Bit Mask Example: 128 Bit Pattern Length
Mask Applied to Bits 2, 34, 66, 98

Incoming DATA ←

```
00010011111101101100110010100010 11111010011010101110100011010110
11000110010100110110111000101101 00101111111100011011101001010011
```

Ref. Pattern ←

```
01011011111101101100110010100010 10111010011010101110100011010110
10000110010100110110111000101101 00101111111100011011101001010011
```

MASK ON:
Measured Error Count = 1
Measured Error Rate = 1 / 124 = 8.1E-3

MASK OFF:
Measured Error Count = 4
Measured Error Rate = 4 / 128 = 3.1E-2

Burst Measurements

- **Non-Continuous DATA is called Burst Data**

Continuous DATA....steady stream of 1's and 0's

`0101101111110110110011001010001010111010011010101110100011` ➔ Into Error Detector

Burst DATA....Intervals with no 1's and 0's

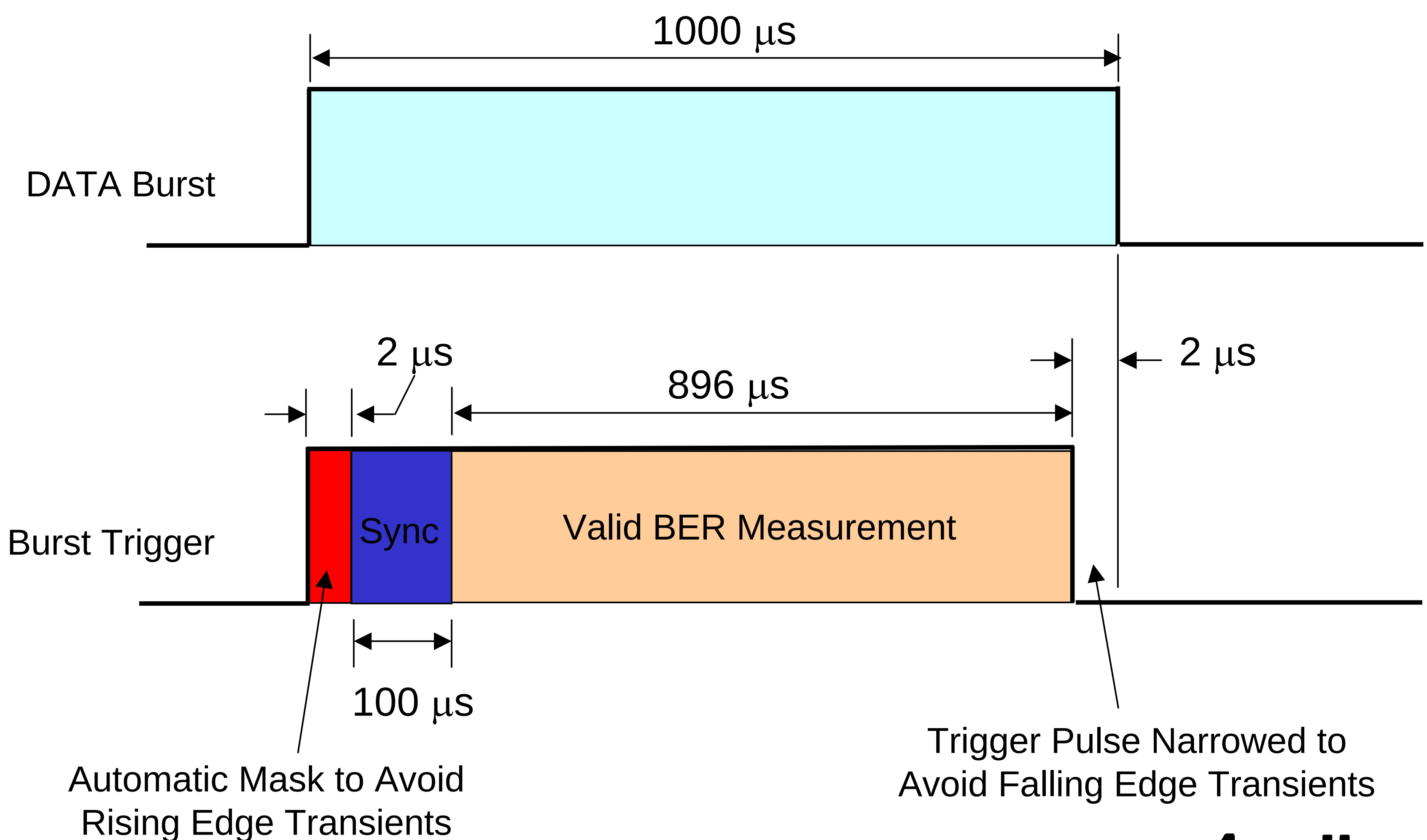
`01101` ——————— `1011101000110` ➔ Into Error Detector

No DATA Present | DATA Present

Burst Measurements

- **The Error Detector Must Be "Told" when DATA is Present. A Burst Input Trigger is Required.**
- **The Burst Trigger stays High During Duration of DATA (minus a few μs to avoid transients)**
- **The Error Detector Must Re-Sync for each Burst Pulse. Valid BER Measurements cannot begin until after Sync. Re-Sync Times must be Fast to Avoid Missing too much DATA.**

Burst Measurements

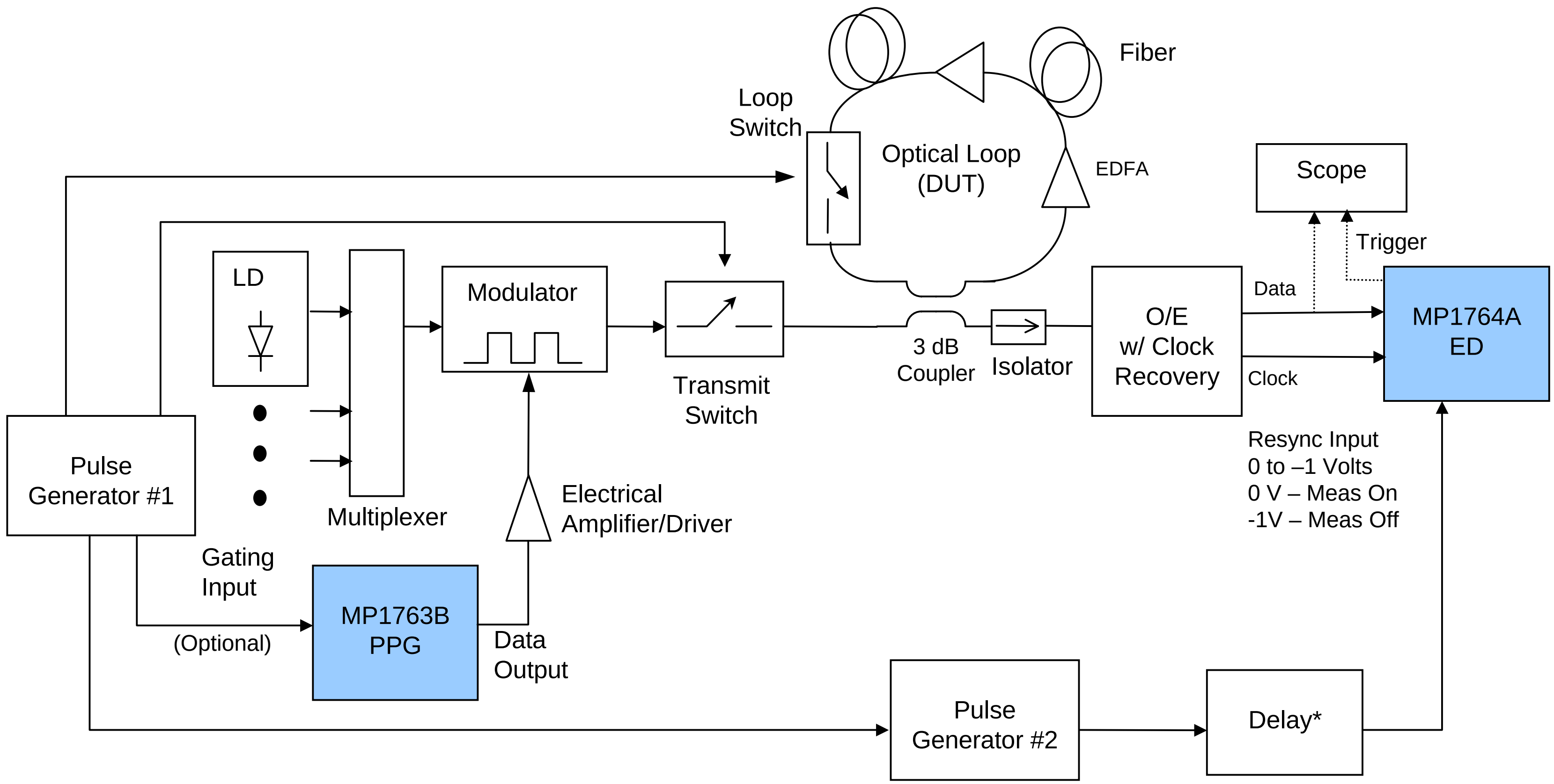


Burst Measurement Applications

- **Circulating Loop Measurement: Simulate Long Haul Optical Transmission Systems with a Subset of the Overall System Hardware.**
  - Burst DATA is Repeatedly sent around Optical Loop to Simulate Long Distance Transmission
  - Popular for Submarine System Simulation, Soliton Research

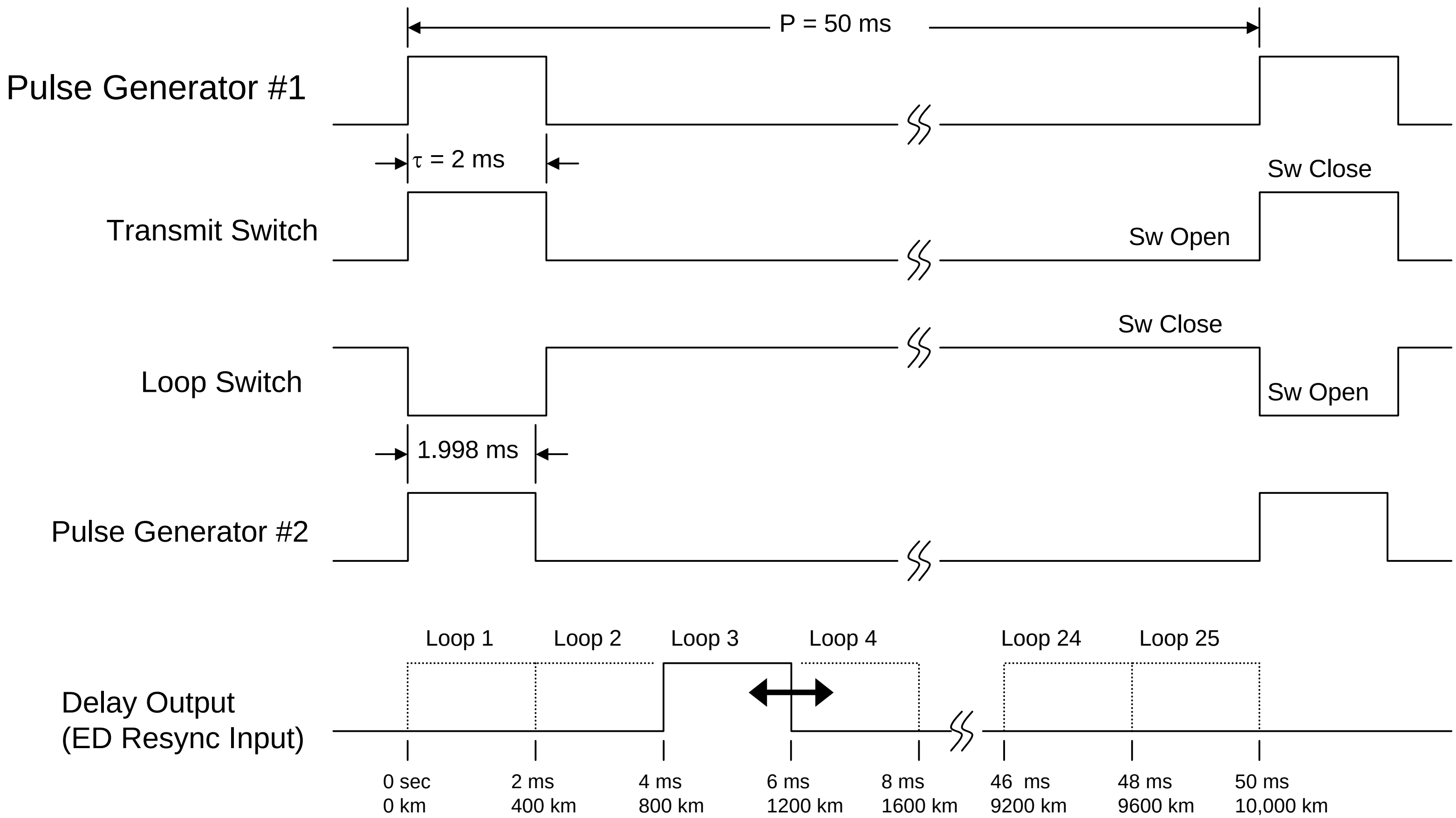
- **PON (Passive Optical Network) Testing**
  - Monitor individual TDMA Channels within a DATA Burst

Circulating Loop Setup



*A separate Delay circuit is not required if Pulse Generator #2 has a “Trigger Delay” feature.

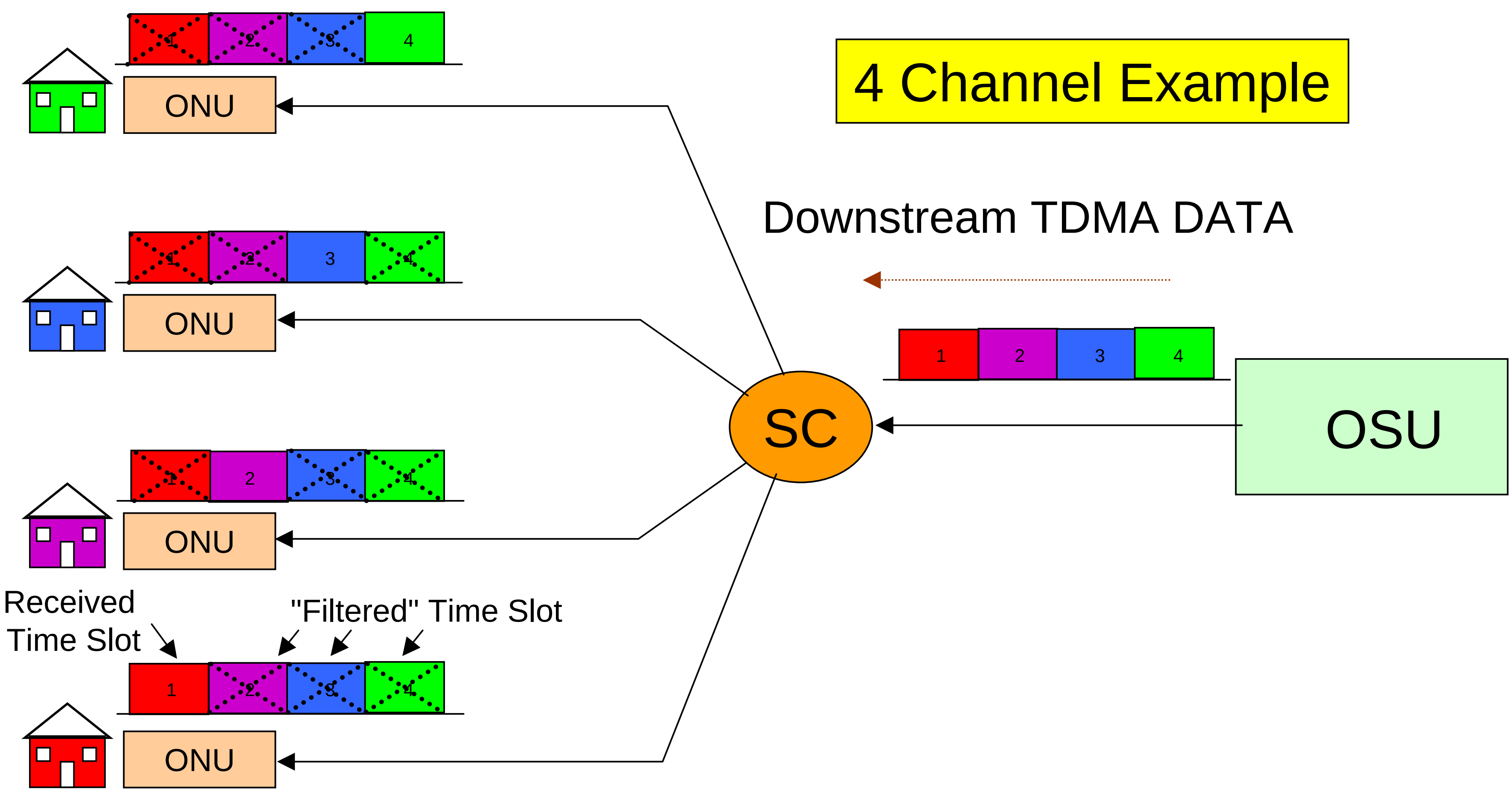
Circulating Loop Timing Diagram



PON Access Networks: Background

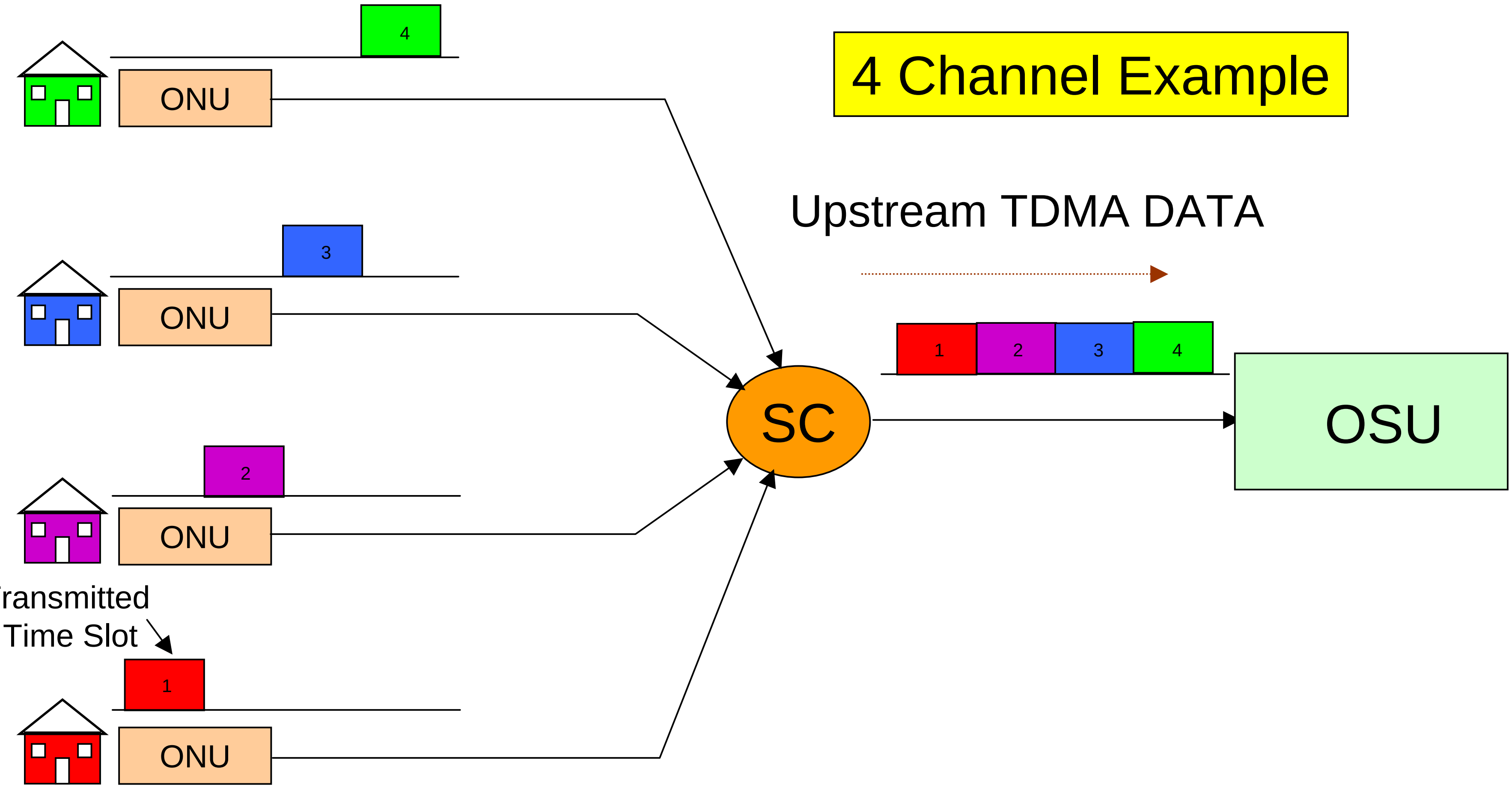
- **PON Systems support Fiber-to-the Home**
- **Two Emerging PON Systems:**
  - High Speed ATM-PDS (Passive Double Star) System
    - Defined in G.983
    - 156M and 622M Rates
    - Up to 32 Channels
    - ATM Cells
    - Upstream/Downstream are WDM: Upstream: 1.31um, Downstream: 1.55um
  - Low Speed Π-PON NTT System used in Japan
    - 49.195M Rate (32 x 1.5M)
    - Up to 32 Channels
    - Upstream/Downstream are TDMA

PON System Block Diagram: Downstream

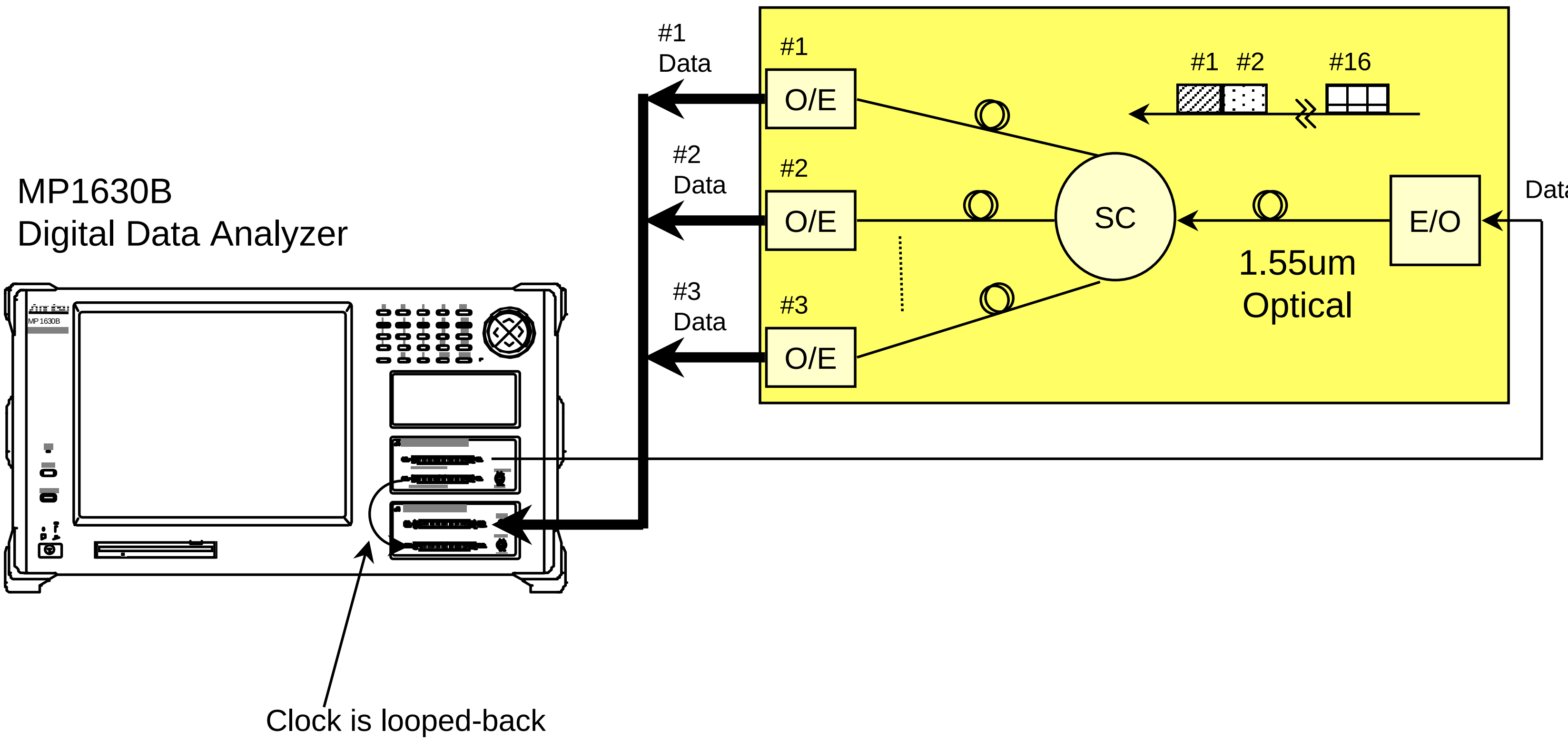


SC: Star Coupler
ONU: Optical Network Unit
OSA: Optical Subscribers Unit

PON System Block Diagram: Upstream

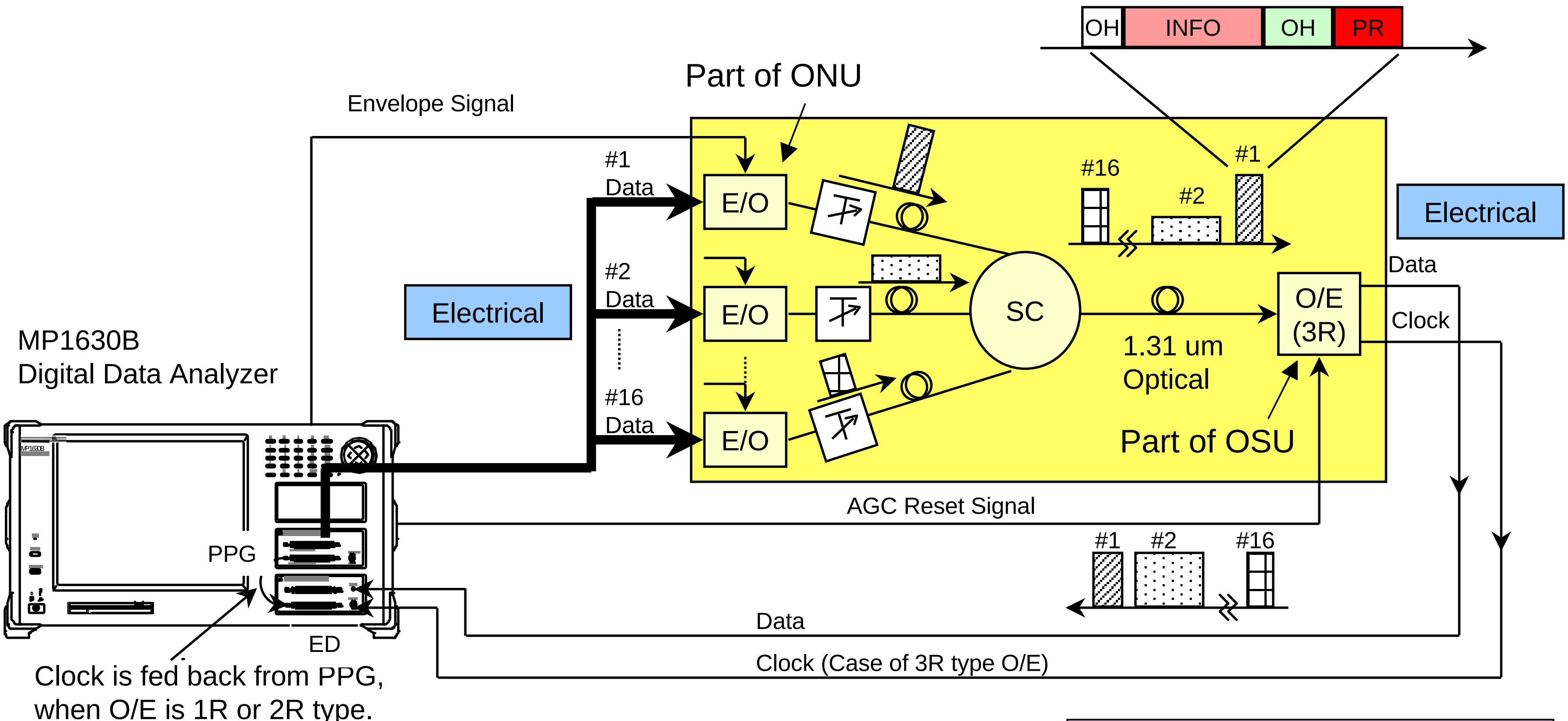


ATM-PDS System Testing (Downstream)



Linking the World

ATM-PDS System Testing (Upstream)



- Clock : 156Mb/s
- Packet Length : 56 Bytes (Standard 53 Byte ATM Cell + 3 Header Bytes)

PR: Preamble (1/0 Alternate)
OH: Overhead (PRGM)
INFO: Information(PRBS or PRGM)
SC: Star Coupler

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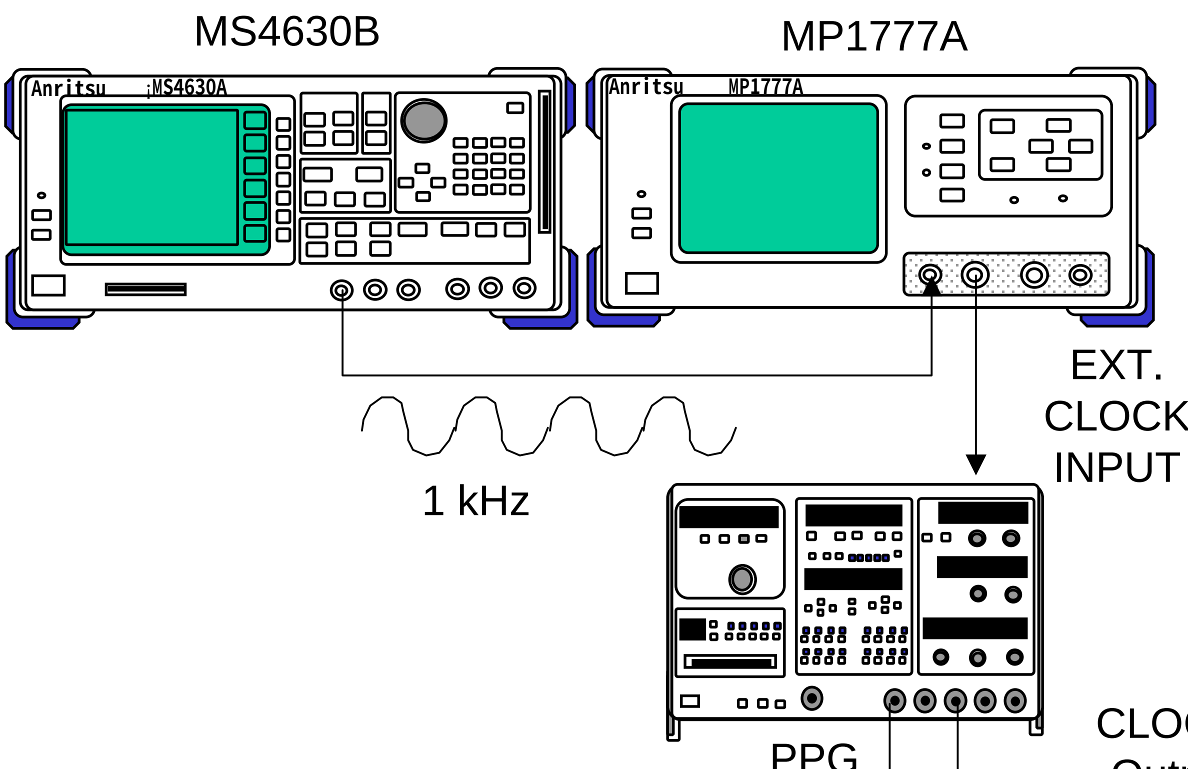
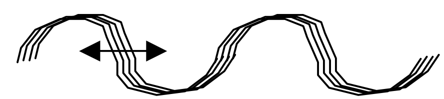
Jitter Measurements

- **The Anritsu MP1763B/MP1764A BERTs are incorporated into the MP1777A 10 G Jitter Measurement System**
  - MP1763B PPG outputs Jittered DATA derived from Jittered External Clock
  - MP1764A ED measure BER in Jitter Tolerance Tests
- **MP1777A supports Jitter Tolerance, Jitter Transfer, and Jitter Generation Measurements at OC-192 and OC-192 FEC rates**
  - Jitter Tolerance Measurement Requires PPG and ED
  - Jitter Transfer Measurement Requires PPG
  - Jitter Generation Measurement Does Not Require PPG or ED

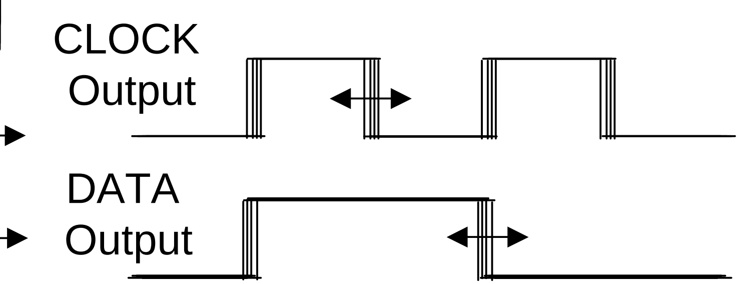
Generating Jittered DATA with the MP1763B PPG



MS4630B Network Analyzer Outputs a Sinusoid at the desired Jitter Rate. MP1777A Creates Phase Modulation on 9.953 Gbit Clock. Amplitude of Jitter is Proportional to MS4630B Signal Amplitude.



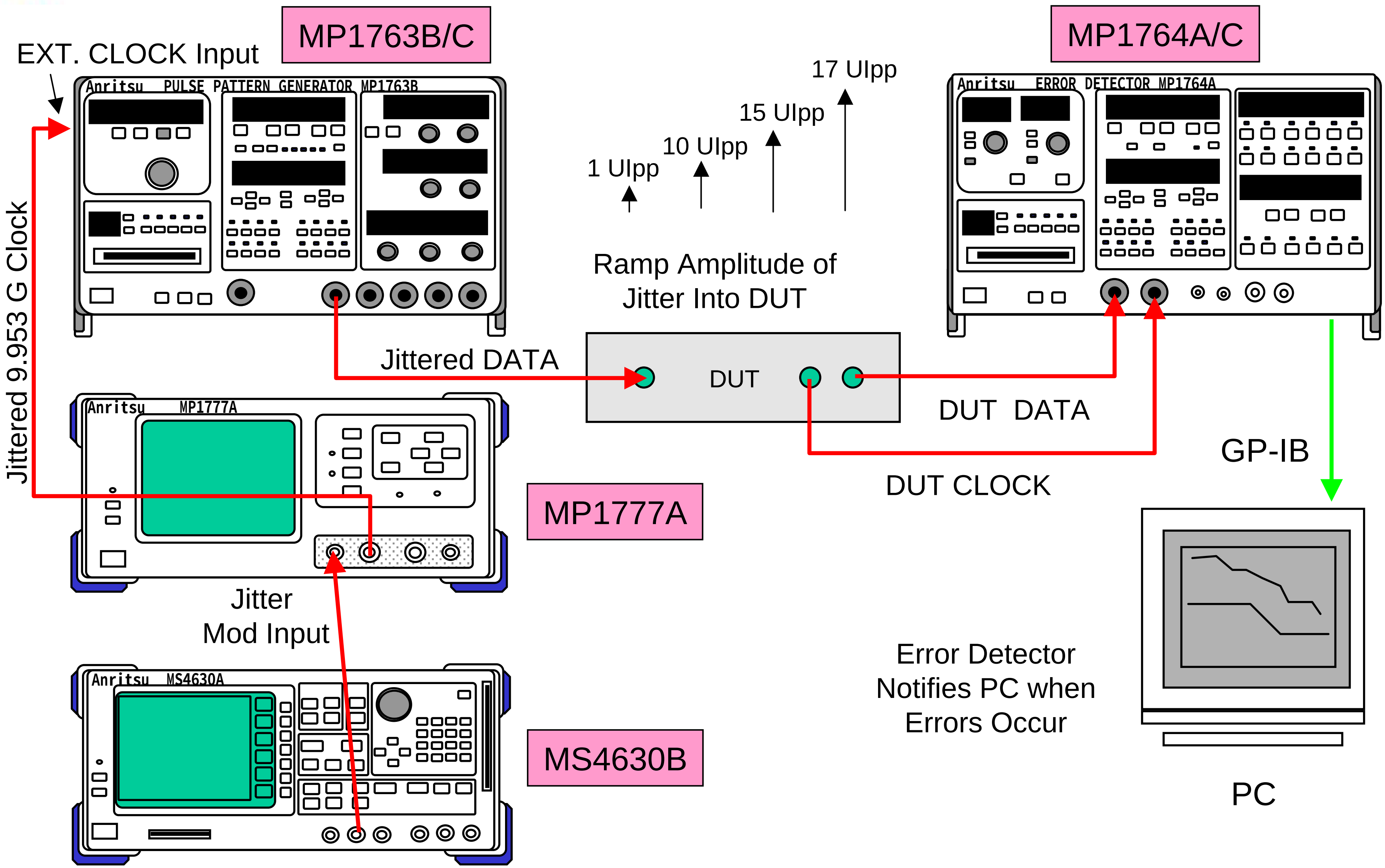
9.953 G with 1kHz Jitter



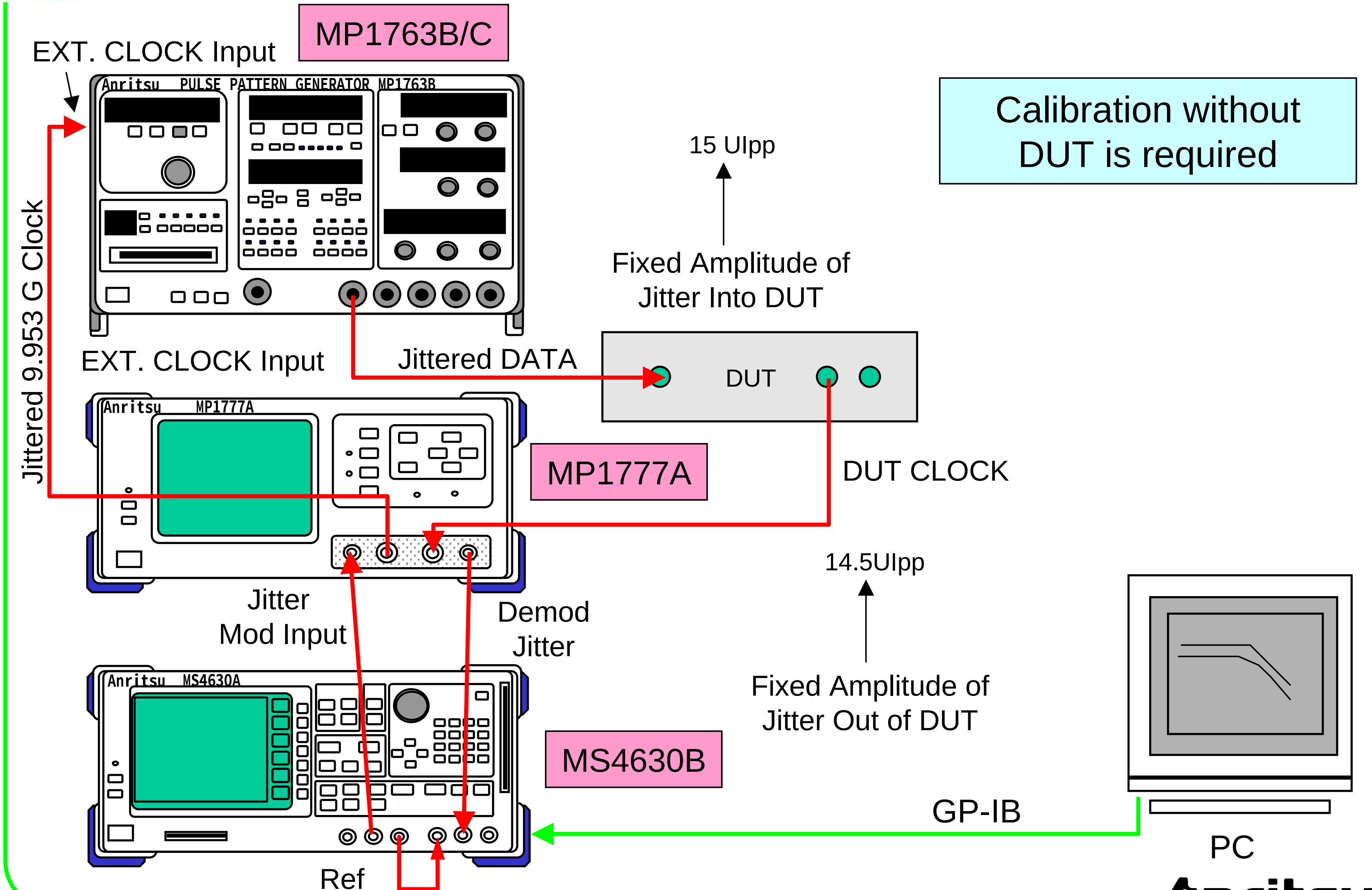
PPG receives Jittered Clock From MP1777A. Outputs DATA and CLOCK with same Jitter

9.953 G with 1kHz Jitter

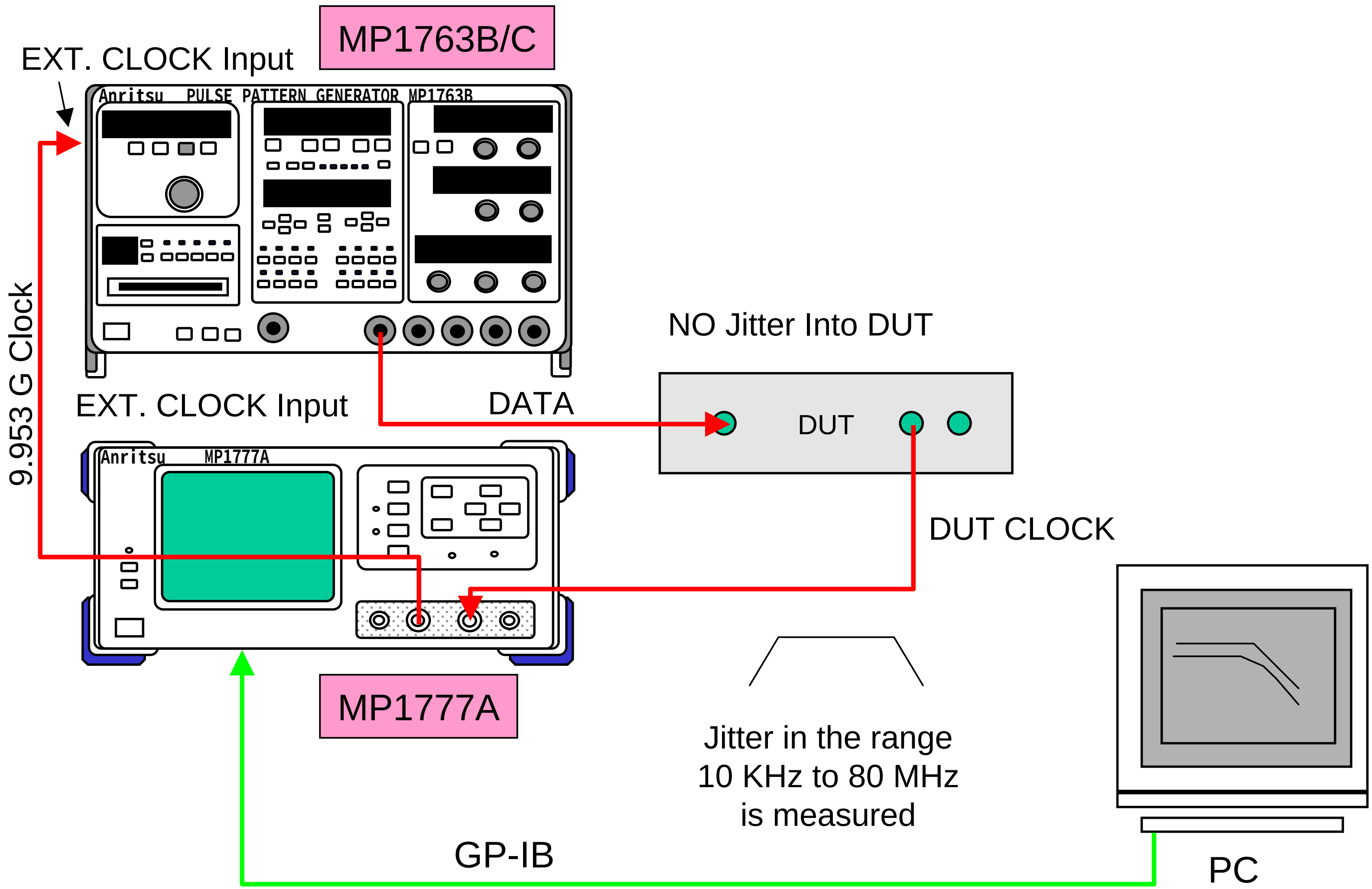
MP1777A Jitter Tolerance Test



MP1777A Jitter Transfer Test



MP1777A Jitter Generation Test

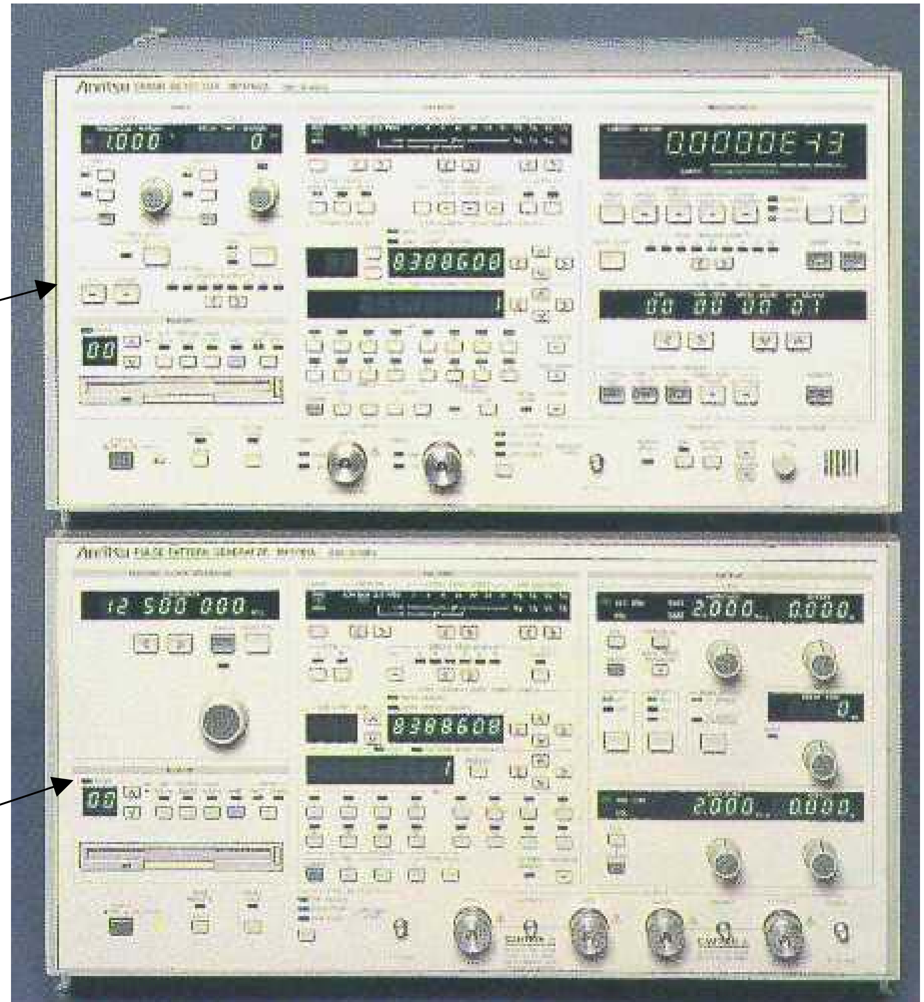


Linking the World

MP1763/64 12.5 G BERT

MP1764A/C

ED



MP1763B/C

PPG

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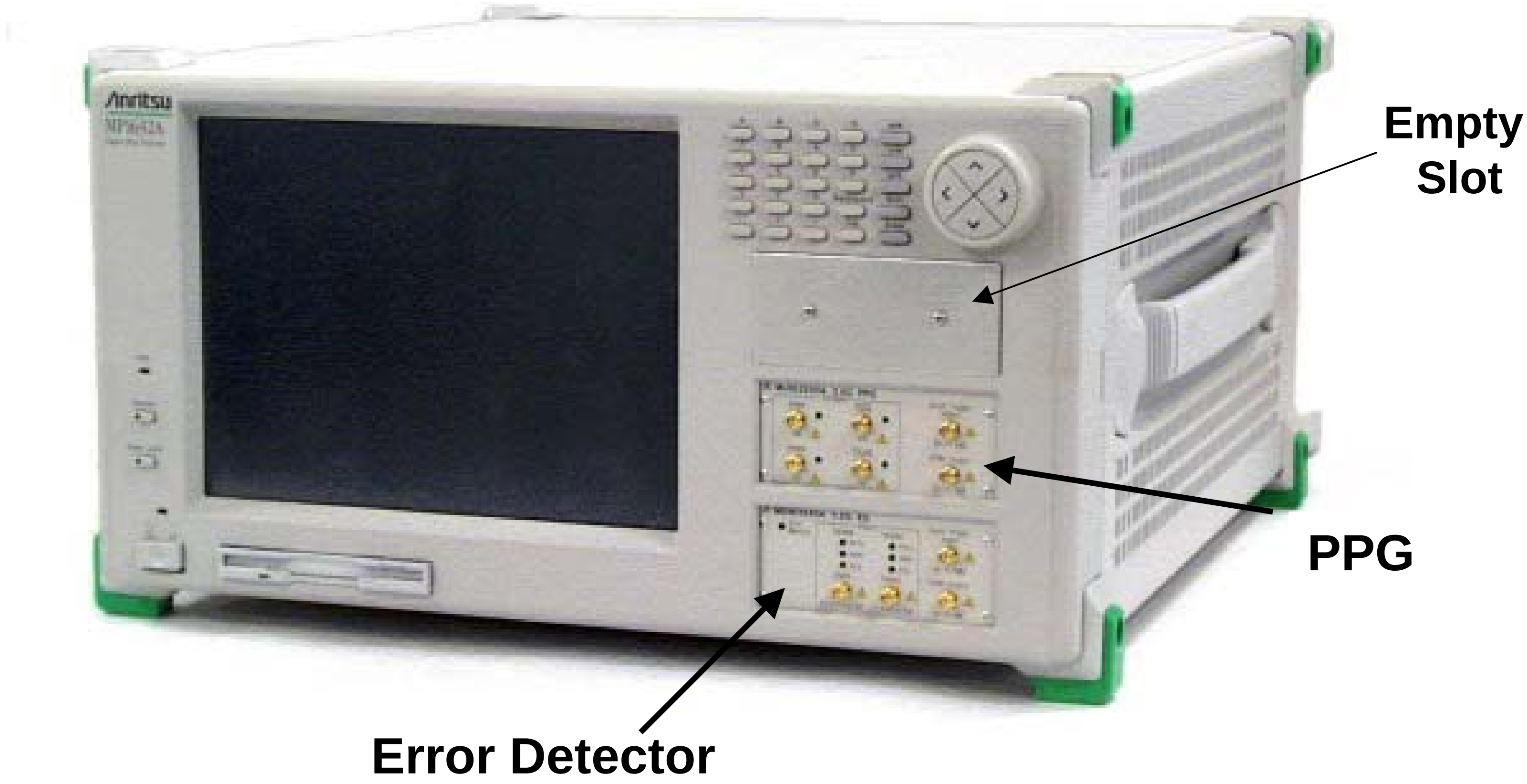
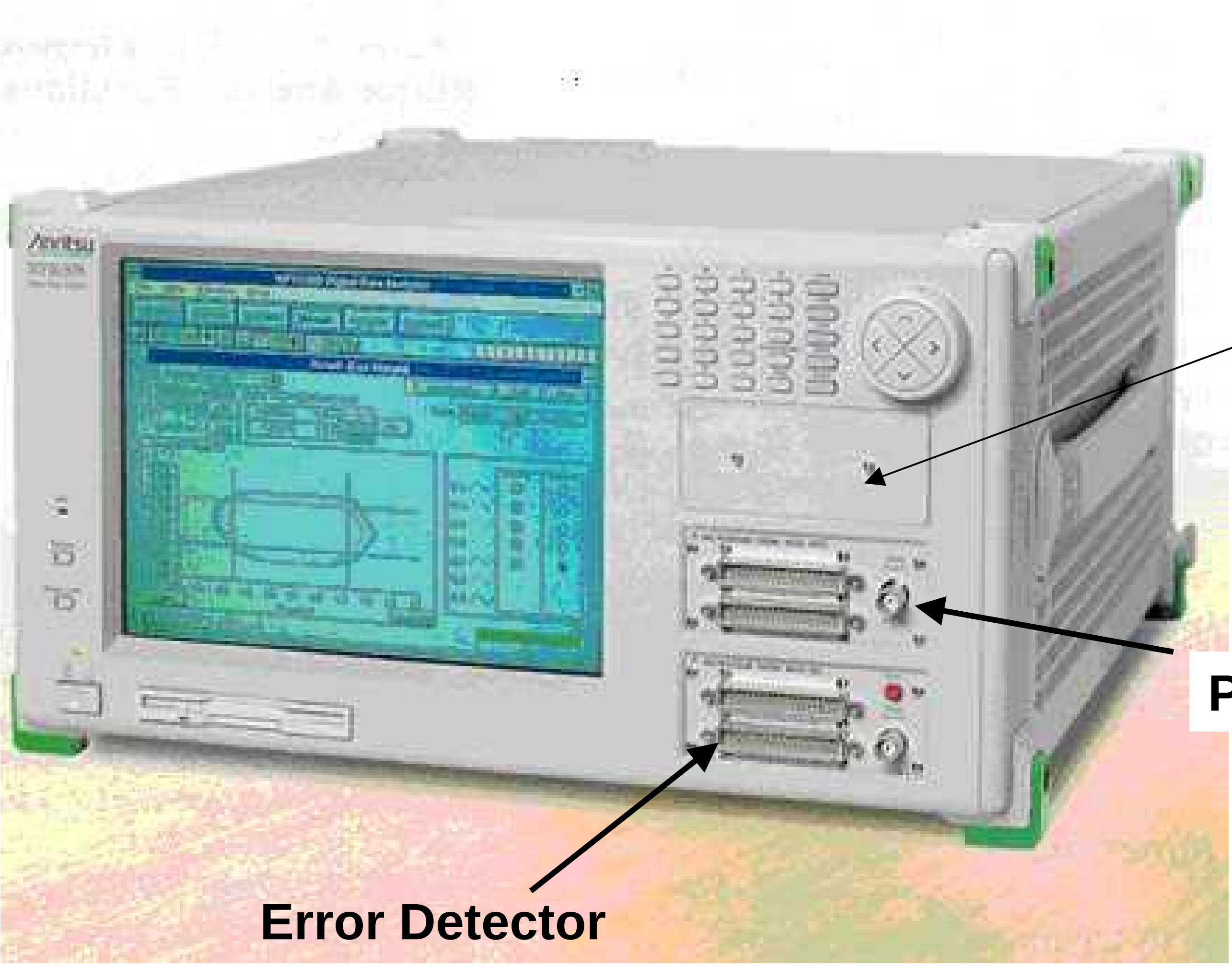
MP1632A/C 3.2 G BERT



Pattern Generator and Error Detector In Same Chassis

MP1630B 200M x16 Channel BERT



Pattern Generator and Error Detector In Same Chassis

MP1777A Jitter Analyzer System

PC

MP1777A

MS4630B

ME7750A 43.5Gbit/s BERT System

Press conference material

September 25th, 2001

ANRITSU Corporation

Measurement Solutions

Contents

43.5Gbit/s BERT System

25 to 43.5Gbit/s

Measurement solution of 40 Gbit/s Transmission System and Optical Modules

Target DUT (Device under test)

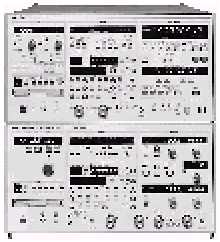
- 40 Gbit/s driver amplifier
- Multiplexer modules
- Demultiplexer modules
- E/O modules
- O/E modules
- 40 to 43 Gbit/s SONET/WDM transmission equipments

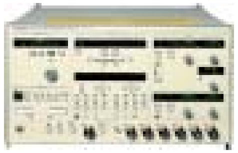
History of Anritsu BERTS

43.5G BERTS System
in September 2001

High waveform quality 43.5 Gbit/s BERT System

12.5Gbit/s 4ch BERTS
in 1994

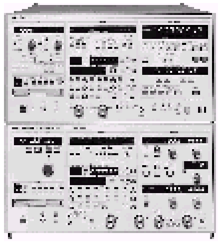




12.5Gbit/s 4ch PPG
in 1994

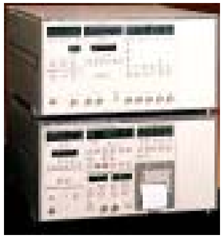
Best seller products that sold over 1000 sets.

3Gbit/s BERTS
in 1990



3.2Gbit/s BERTS in 1998

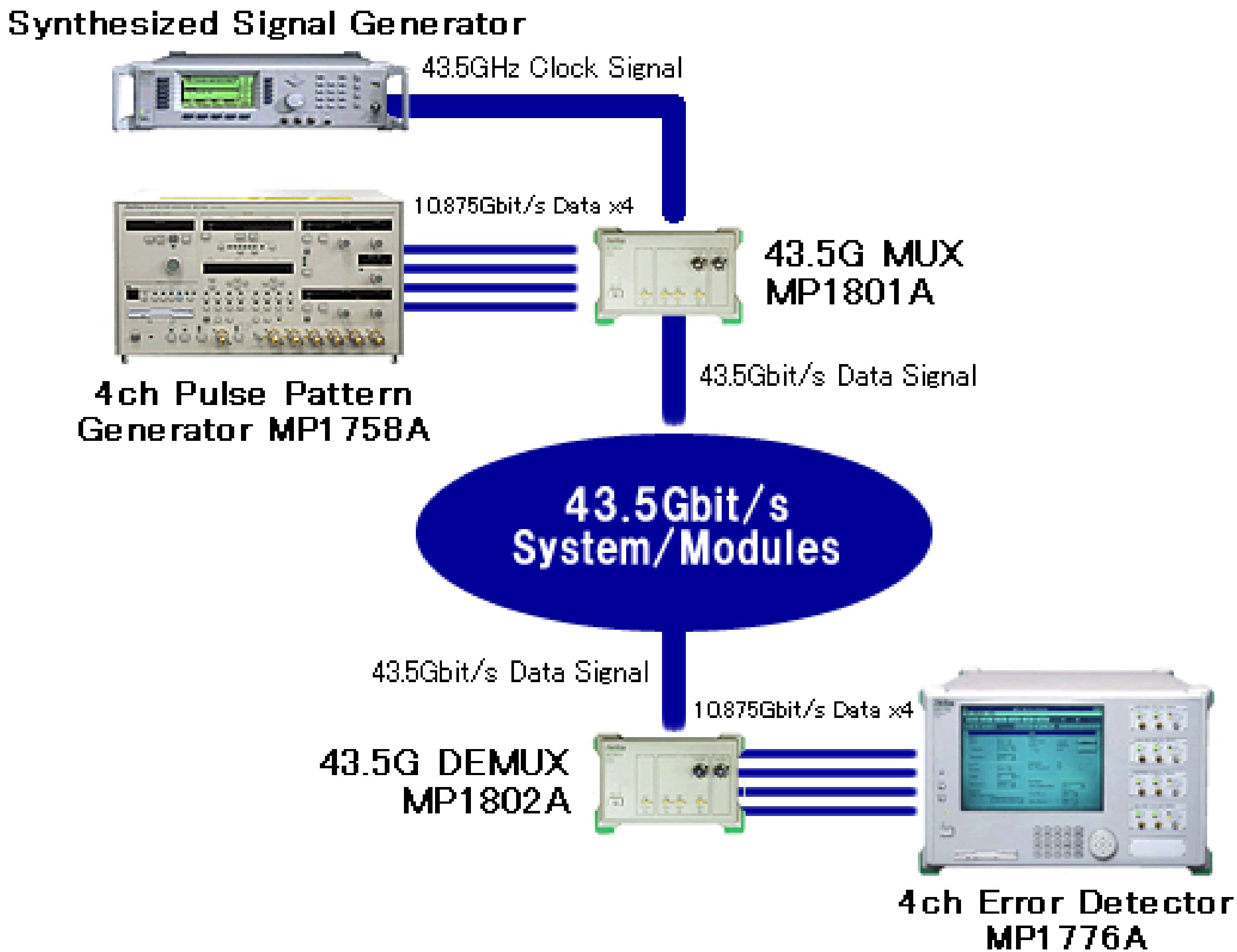
Long seller products that sold 1600 sets on the manufacturing market



1.4Gbit/s BERTS
in 1961

Release of the Bit Error Rate measuring instrument for Giga band Rate

Configuration of 43.5Gbit/s BERT System



Component Instruments of ME7750A 43.5Gbit/s BERT System (1)

69397B Synthesized Signal Generator

The 69397B can generate clock signal up to 65 Gbit/s.
It is used as a clock signal generator for the 43.5 GHz measurement.

MP1758A Pulse Pattern Generator

The MP1758A can generate 4 data signals up to 12.5 Gbit/s. It can generate PRBS and PRGM signals up to 43.5 Gbit/s by combining with the MP1801A.

MP1776A Error Detector

The MP1776A can measure 4 pattern signals up to 12.5 Gbit/s independently. It can measure errors of PRBS and PRGM signals up to 43.5Gbit/s by combining with the MP1802A.

Component Instruments of ME7750A 43.5Gbit/s BERT System (2)

MP1801A 43.5G MUX

The MP1801A multiplexes four signals up to 10.875 Gbit/s generated from the MP1758A, and then it outputs the 43.5Gbit/s data and clock signals.
It can also output a 1/4 clock of 43.5 GHz

MP1802A 43.5G DEMUX

The MP1802A separates a data signal of 43.5 Gbit/s into 4 channels, then it can output them to the MP1776A.

Features of ME7750A 43.5 Gbit/s BERT System

- **Wide operating bitrates**
- **Evaluation using PRBS signal conforming to ITU-T recommendation**
- **Measurement using burst signal**
- **High quality multiplexer output waveform**
- **High sensitive demultiplexer input**
- **Margin measurement of 43.5 Gbit/s signal**

PRBS: Pseudo Random Binary Sequence
Used in the evaluations as real transmission signals.

Total Solutions for R&D of 40 Gbit/s Transmission System (1)

• Support up to 43.5 Gbit/s operating bitrates

Fully support FEC bitrates.
The MP1758A (4ch pulse pattern generator) and the MP1776A (4ch error detector) operate from 100 Mbit/s to 12.5 Gbit/s.
The 43.5G MUX and 43.5G DEMUX support from 25 Gbit/s to 43.5 Gbit/s.

• Evaluation using PRBS signal conforming to ITU-T

It is possible to measure the errors at up to 43.5 Gbit/s using PRBS signal.
Selectable PRBS pattern length; 2^N-1 N=7, 9, 11, 15, 20, 23, 31.

• Generation of burst signal required for the optical circulating loop testing, etc.

It is possible to measure burst signal at 43.5 Gbit/s by using burst measurement function of the MP1776A.

FEC : Forward Error Correction

Total Solutions for R&D of 40 Gbit/s Transmission System (2)

- **High quality multiplexer output waveform**

Low jitter, low waveform distortion and high output amplitude (2 Vp-p) are achieved by using ultra-high speed D-type flip-flop as a re-timing function.

- **High sensitive demultiplexer input**

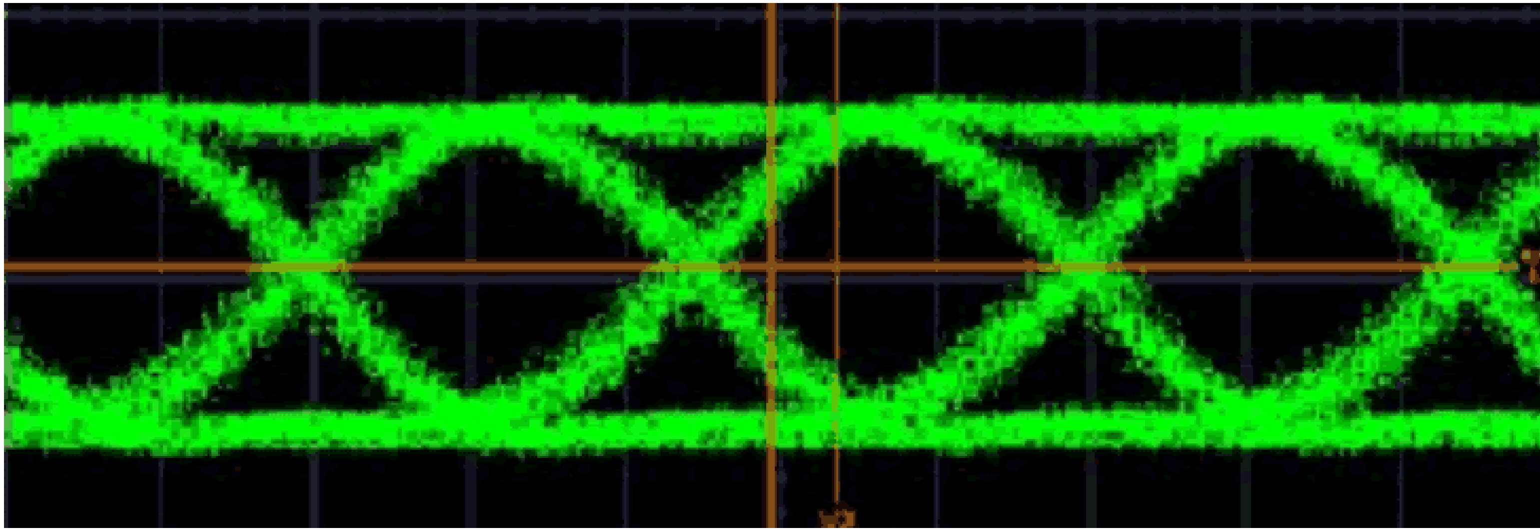
The minimum input amplitude of data signal is 100 mVp-p (at 43.5 Gbit/s).

- **Eye Margin measurement of 43.5Gbit/s signal**

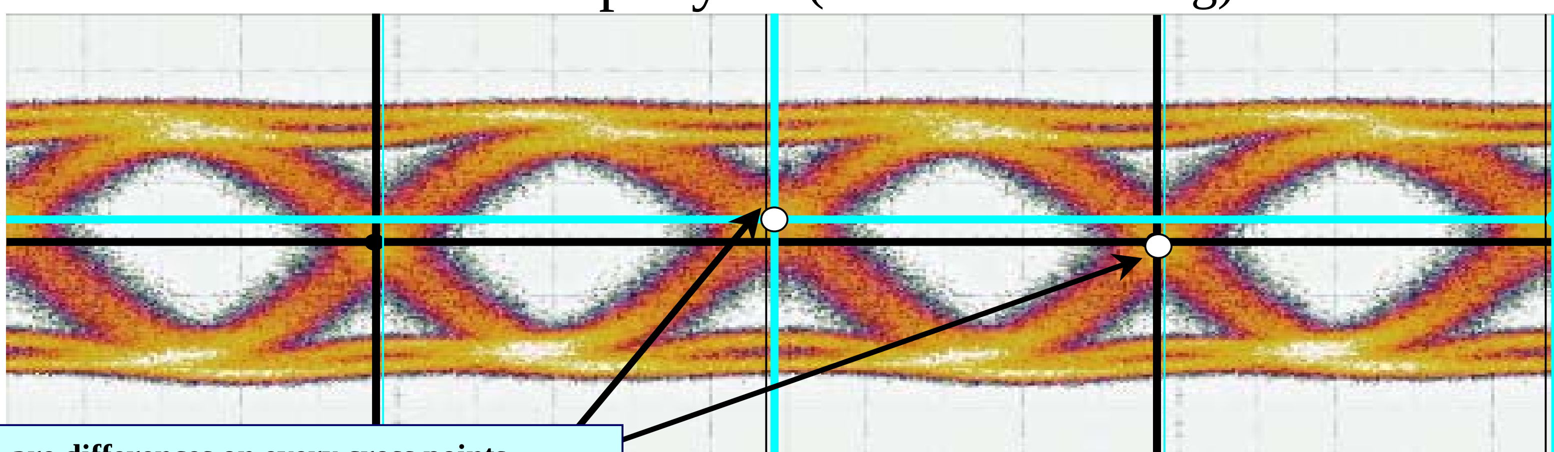
The demultiplexer unit has the adjustment function of the voltage and the clock delay. Those functions make it possible to measure the eye-margin with counting the bit error rates.

Performance Comparison

Anritsu’s Waveform (with D-type flip-flop re-timing circuit)



Waveform of the Company-A (From their catalog)



There are differences on every cross points

Future Development Plan

80/160Gbit/s

40Gbit/s Jitter Analyzer

40Gbit/s Next Generation SDH/SONET Analyzer

Optical Interface

SDH/SONET Frame

43.5Gbit/s BERT System

A Future Subjects
- Functional improvement
- Higher bit-rate operation
- Down sizing

Anritsu

Thank you for listening to our presentation.

ANRITSU Corporation

Measurement Solutions

Digital. Com Div