# Project #1 for Electronic Circuit II

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- Deadline : 6:00 pm on Apr. 7, 2007. No late hand-in will be allowed.

- Team

Students are expected to form a team of two members to do the project and hand in one project report. Equal grades will be given to the members of the same team. Each team must do its own simulation and analysis.

- MOS PSpice parameters

Use Level 7 PSpice parameters for 0.25㎛ CMOS process. The course homepage (강의노트) has PSpice 9.1 student version, level 7 PSpice parameters as well as PSpice basic manual.

- Design rules

1. VDD = 2.5V
2. 0.25㎛ ≤ length of gate ≤ 2㎛
3. 0.25㎛ ≤ width of gate ≤ 200㎛
4. 0.1 ㎊ ≤ all capacitors ≤ 20 ㎌
5. 0 Ω < all resistors ≤ 800㏀
6. Body of pMOS must connect to VDD
7. Body of nMOS must connect to GND

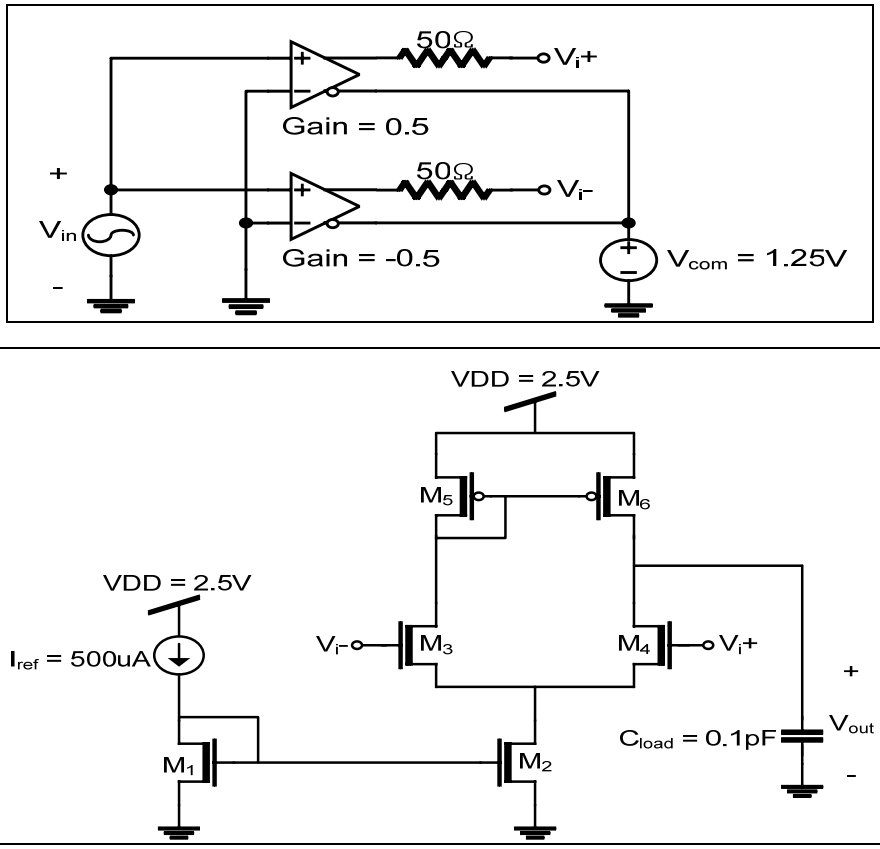
- Goal

You are expected to design 2-stage OTA (shown next page) satisfying given specifications. Your design will be evaluated based on following criteria:

1. How well you satisfy the specifications.
2. How good your amplifier is in terms of its gain-bandwidth product.
3. How good your design report is.

## I. 1-Stage differential amplifier Design [20]

Design 1-Stage differential amplifier that satisfies the following design goals. Differential input source circuit is also given for your simulation condition.




<Fig. 1> 1-Stage differential amplifier schematic

- Design Goals -

| Parameter | Value |
|---|---|
| $A_v$ | > 28 dB |
| Bandwidth | > 120 MHz |
| Input Common Mode Range (ICMR) | Range > 1.35 V |
| Power Consumption | < 1.25 mW |

You should include the following items in the report.

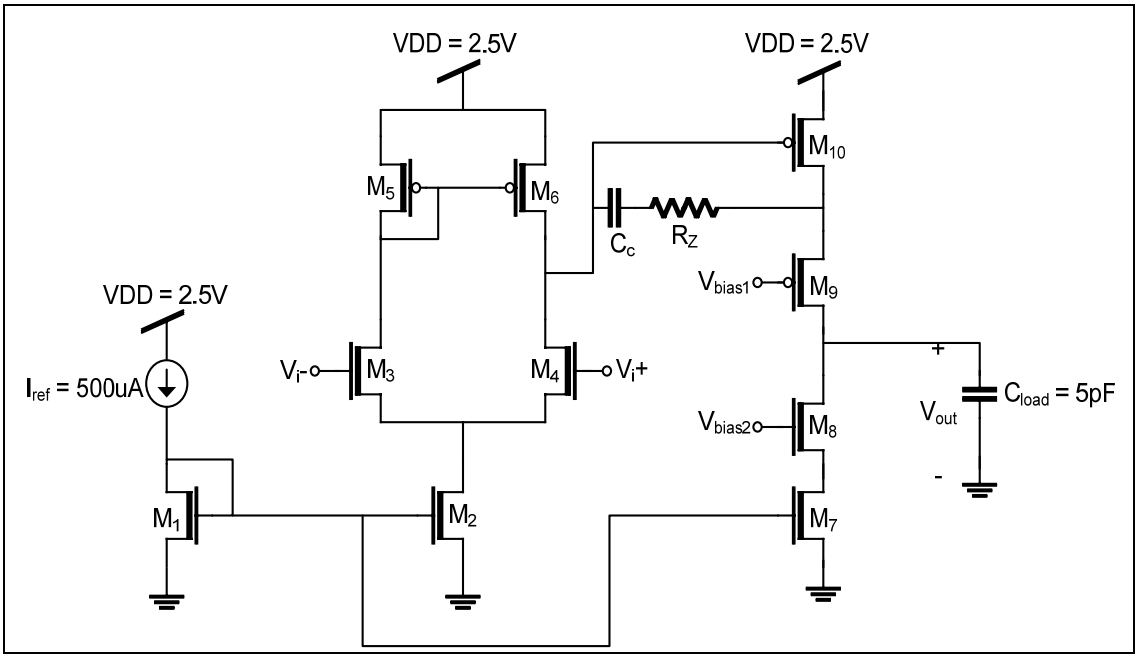
(1) PSpice simulation process to measure each design parameter.

(2) Design processes (How you come up with your design values)

(3) Final results (plots and discussions)

## II. 2-Stage OTA Design [60]

Design the 2-stage OTA that satisfies the following design goals. You may use the design results obtain in Part I.




<Fig. 2> 2-Stage OTA Schematic

- Design Goals -

| Parameter | Value |
|---|---|
| $A_v$ | > 76 dB |
| Bandwidth | > 20 KHz |
| Phase Margin | > 65 ° |
| Slew Rate | > 30 V/us |
| $V_{op\text{-}p}$ (saturation region) | > 800 mV |
| Common Mode Rejection Ratio (CMRR) | > 62 dB |
| Input Common Mode Range (ICMR) | Range > 1.35 V |
| Power Consumption | < 2.5 mW |

## III. 2-Stage OTA Design with temperature variation [10]

Show that your circuit is functional for the temperature between 0°C and 100°C.

## IV. Design Report [10]

You should write a design report in which you clearly explain how you come up with your transistor W/L values and what values you have achieved for design specifications. All your design results should be summarized in Design Summary Sheet. Place the Design Summary Sheet right after the cover page of your report. Three extra points will be given if your report is written in English.

## V. Design Presentation in English [15, extra point]

Eight teams can make presentation of their design process and results for 15 minutes on 4/11. Eight teams will be selected based on their gain-bandwidth product results among those who want to participate in the presentation.

# Design Summary Sheet

Name 1: Student ID No.:
Name 2: Student ID No.:

< 1-Stage differential amplifier >

| | |
|---|---|
| $(W/L)_1$ | |
| $(W/L)_2$ | |
| $(W/L)_3$ | |
| $(W/L)_4$ | |
| $(W/L)_5$ | |
| $(W/L)_6$ | |
| $A_V$ | |
| Bandwidth | |
| GB | |
| ICMR | |
| Power consumption | |

< 2-stage OTA >

| | | | |
|---|---|---|---|
| $(W/L)_1$ | | Av | |
| $(W/L)_2$ | | Bandwidth | |
| $(W/L)_3$ | | Gain Bandwidth product | |
| $(W/L)_4$ | | Phase margin | |
| $(W/L)_5$ | | Slew rate | |
| $(W/L)_6$ | | Vop-p | |
| $(W/L)_7$ | | CMRR | |
| $(W/L)_8$ | | ICMR | |
| $(W/L)_9$ | | Power consumption | |
| $(W/L)_{10}$ | | | |
| Cc | | | |
| Rz | | | |
| $V_{bias1}$ | | | |
| $V_{bias2}$ | | | |

Participation in English presentation(check one): Yes No