Project #3 for Electronic Circuit II

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- Deadline : 6:00 pm on June 9th, 2007. No late hand-in will be allowed.

- Team

Students are expected to form a team of two members to do the project and hand in one project report. Equal grades will be given to the members of the same team. Each team must do its own simulation and analysis.

- MOS PSpice parameters

Use Level 7 PSpice parameters for 0.25㎛ CMOS process. The course homepage (강의노트) has PSpice 9.1 student version, level 7 PSpice parameters as well as PSpice basic manual.

- Design rules

1. VDD = 2.5V
2. 0.25㎛ ≤ length of gate ≤ 2㎛
3. 0.25㎛ ≤ width of gate ≤ 200㎛
4. 0.1 ㎊ ≤ all capacitors ≤ 20 ㎌
5. 0 Ω < all resistors ≤ 800㏀
6. Body of pMOS must connect to VDD
7. Body of nMOS must connect to GND

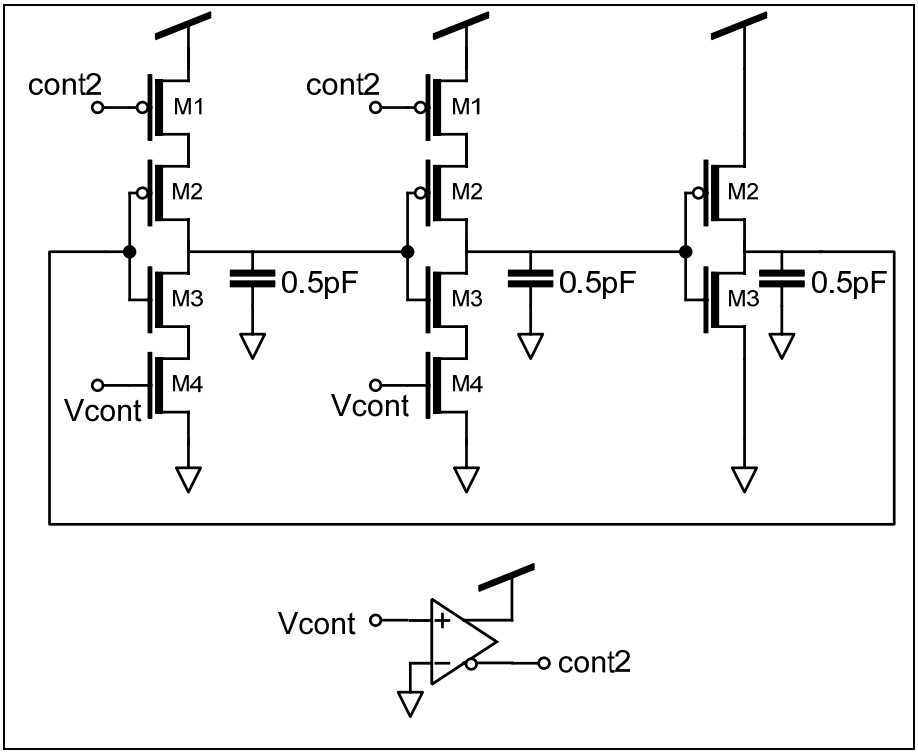
- Goal

You are expected to design a Phase-Locked Loop satisfying given specifications. Your design will be evaluated based on following criteria:

1. How well you satisfy the specifications.
2. How good your settling time of PLL is.
3. How good your design report is.

I. Ring-type Voltage Controlled Oscillator Design [20]

Design a ring-type VCO that satisfies the given design goals. The circuit configuration is given below.



<Fig. 1> Ring-type Voltage Controlled Oscillator schematic

- Design Goals -

Parameter	Value
Frequency Controllability	Min. < 50MHz, Max. > 200MHz
Max. VCO gain (parametric sweep step <= 0.05V)	< 150MHz/V

You should include the following items in the report.

(1) Principle of ring-type VCO operation.

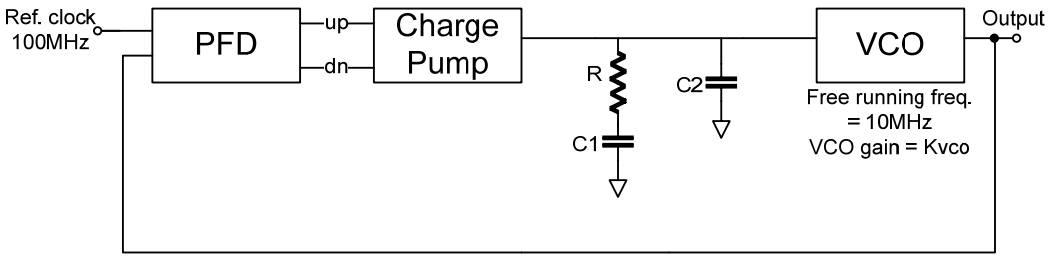
(2) Simulation results:

- Clock signal plot in time domain at control voltage of 1.5V.
- Frequency vs. Vcont plot and discussions.

(3) VCO gain (Kvco) at control voltage of 1.5V.

II. PLL Design [70]

Design the Phase-Locked Loop that satisfies the given design goals. You must use your design results (Kvco at Vcont=1.5V) obtain in Part I.



<Fig. 2> PLL block diagram

- Design Goals -

Parameter	Value
Settling time	As low as possible
Phase margin	> 50 deg
Max. peaking	< 2.75 dB
Damping	<= 0.01 V
20 kHz output jitter gain	= 1
2 MHz output jitter gain	< 0.5
Icp	10uA <= Icp <= 500uA

You should include the following items in the report.

(1) Theory of PLL dynamics.

(2) Relationship between phase-margin and settling-time.

(3) How do you decrease the damping ratio?

(4) How do you decrease the max. peaking in jitter transfer function?

(5) Simulation results:

- Vcont plot in time domain.
- Eye-diagram of output clock without jitter input.
- Eye-diagram of output clock with 20kHz jitter input.
- Eye-diagram of output clock with 2MHz jitter input.

III. Design Report [10]

You should write a design report in which you clearly explain how you come up with your transistor W/L values and what values you have achieved for design specifications. All your design results should be summarized in Design Summary Sheet. Place the Design Summary Sheet right after the cover page of your report. Three extra points will be given if your report is written in English.

Design Summary Sheet

Name 1: Student ID No.:
Name 2: Student ID No.:

< Ring-type VCO Design >

$(W/L)_1$	
$(W/L)_2$	
$(W/L)_3$	
$(W/L)_4$	
Min. frequency	
Max. frequency	
Kvco at Vcont=1.5V	
Power consumption	

< PLL Design >

R	
C1	
C2	
Damping factor	
Natural freq.	
Settling time	
Phase margin	
Max. peaking	
Damping	
20kHz jitter	
1.16MHz jitter	