Quiz #3

June 1, 2009
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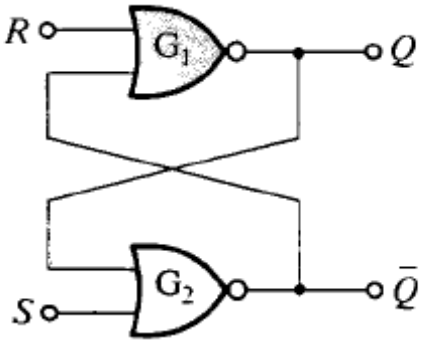
Electronic Circuits II

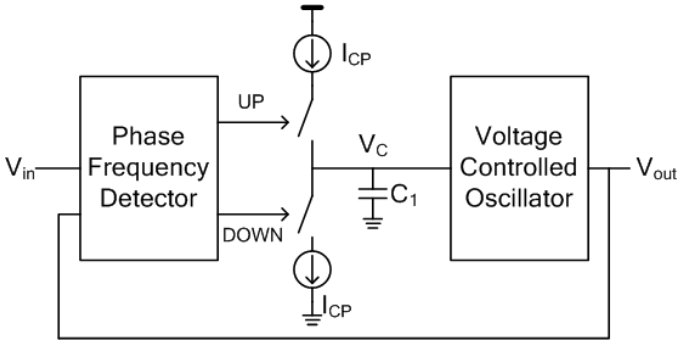
Prob. 1(2)

SR (Set-Reset) flip flop can be realized by cross coupling two NOR gates as shown below. Draw the circuit schematic for CMOS implementation of SR flip flop. Make sure you clearly indicate S, R, Q, Q terminals in your circuit.



Prob. 2(4)

Consider the charge pump PLL shown below



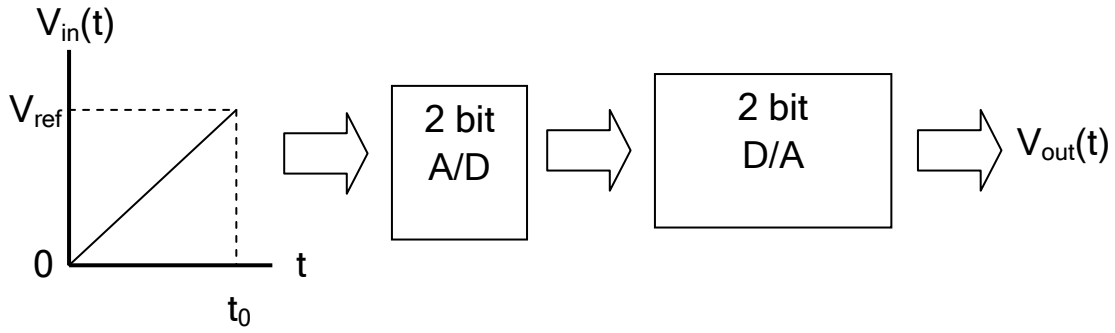
(a)(1) Determine the closed loop gain transfer function, $H(s)=\phi_{out}/\phi_{in}$, where ϕ_{in}, ϕ_{out} are the phase of V_{in}, V_{out}, respectively.

(b)(2) PFD can be realized by two D flip flops and one AND gate. Show the logic gate implementation of PFD.

(c)(1) Explain the main advantage of the PFD realized in (b) over a PD realized with XOR gate.

Prob. 3(4)

We want convert $V_{in}(t)$ into binary codes and then back into an analog signal as shown below. Assume the operation voltage ranges for A/D and D/A converters are from 0 to V_{ref}.



(a)(1) Show the block diagram of 2-bit flash A/D converter.

(b)(1) Show the output binary code of the A/D converter as function of time.

(c)(1) Show the block diagram of 2-bit D/A converter based on binary weighted resistors. Clearly indicate how the A/D output (b_1, b_2 with b_1 MSB) is connected to the D/A converter.

(d)(1) Plot the output of the D/A converter as function of time