Semiconductor Memory II
Future Memory Trend

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VLSI SYSTEM LAB, YONSEI University
School of Electrical & Electronic Engineering

Contents

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Future Memory Trend

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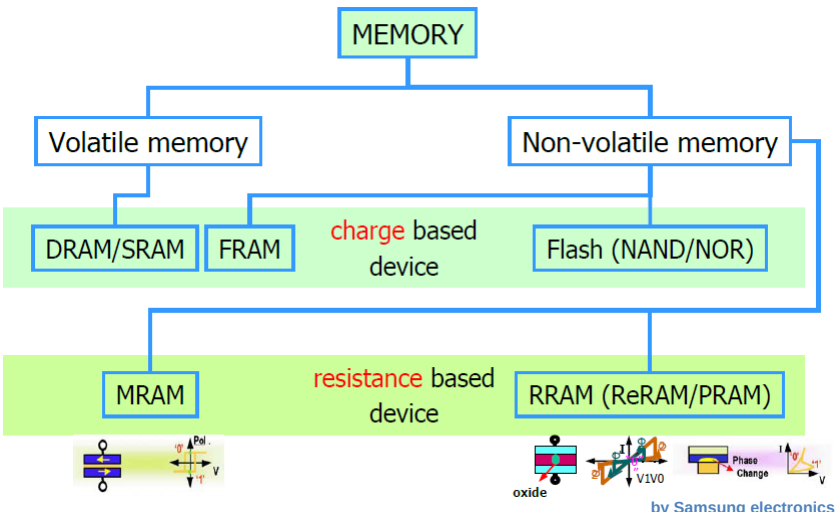
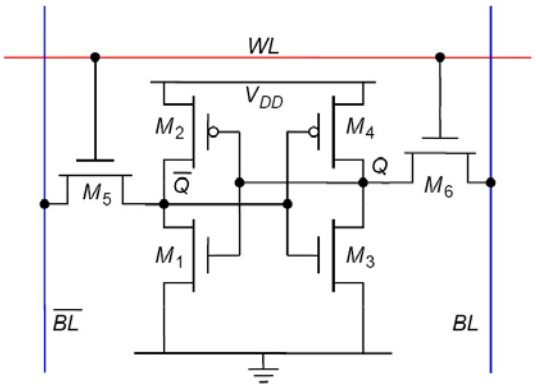
Memory Hierarchy

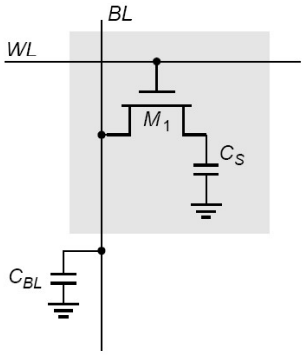


by Samsung electronics

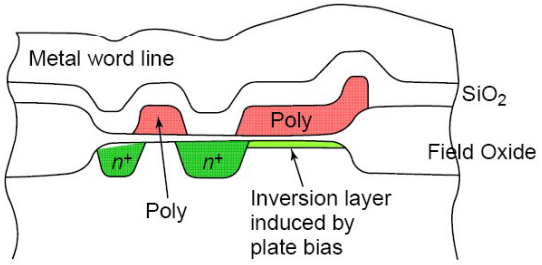
SRAM Cell



DRAM Cell

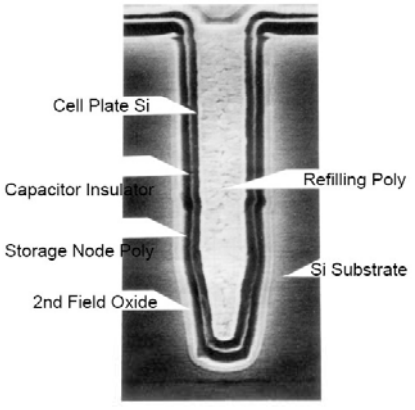


DRAM Cell

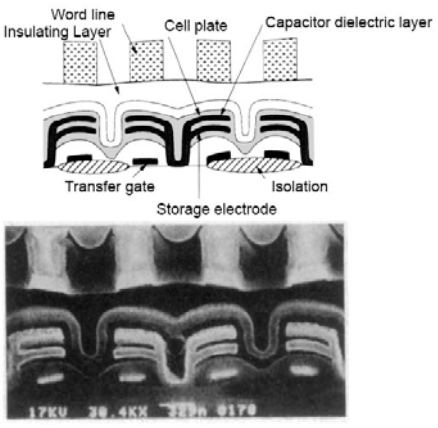


Cross-section

DRAM Cell

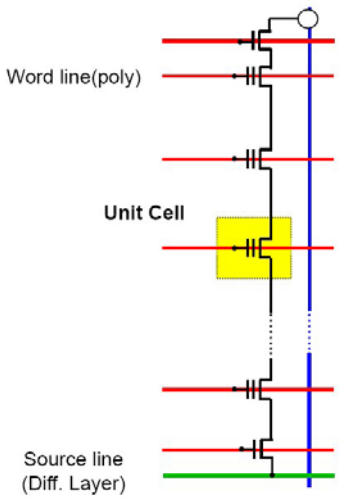


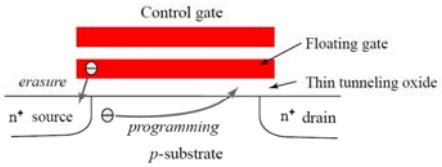
Trench Cell



Stacked-capacitor Cell

Flash Memory Cell





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Current Memories Comparison

	DRAM	FLASH	SRAM
Speed	fast	very slow	very fast
Density	high	very high	low
Endurability	better	poor	better
Power	high	very low	low
Refresh	yes	no	no
Retention	volatile	non-volatile	volatile
Scalability	bad	good	good
Data Storage Mechanism	capacitor	FN tunneling, HCI to floating gate	Bi-stable flip-flop

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DRAM and SRAM Trend

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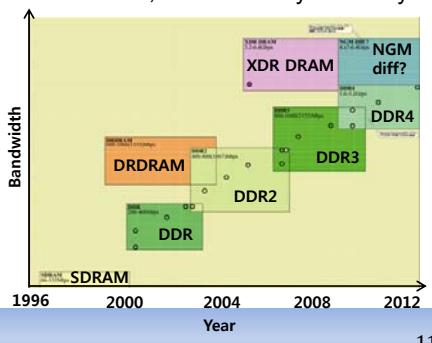
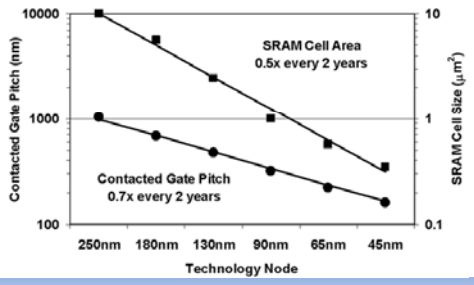
- Improve **performance** and capacity of DRAM and SRAM
  - Technology scaling
  - Design technique
- Function and role of DRAM and SRAM are not changed.
  - SRAM ; cache memory in processor
  - DRAM ; main memory unit in system





by Intel Technology Journal

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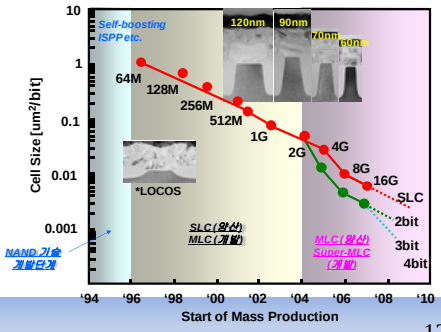
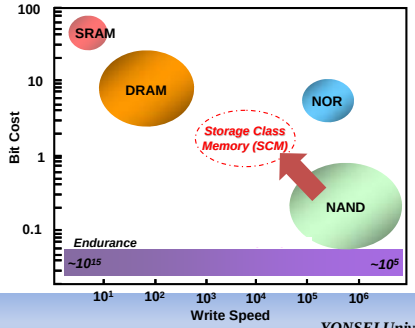
NAND Flash Trend

VLSI SYSTEM LAB.

- Improve **capacity** and performance of NAND flash memory
  - Technology scaling
  - Design technique
- Positioning of NAND flash have been changed.
  - Past ; digital camera, MP3, USB memory..
  - Recent ; solid state drive (SSD) for replacing HDD





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Universal Memory

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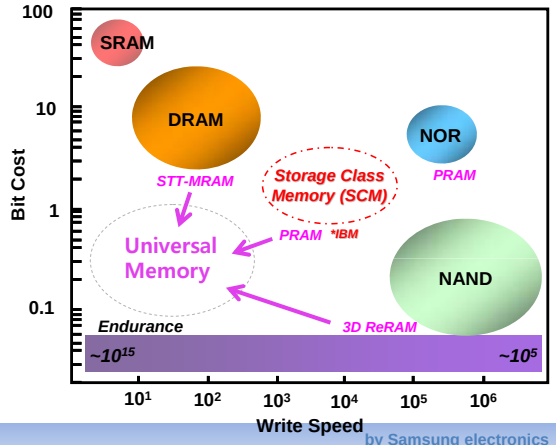
◆ Universal memory is desired for next-generation memory.
- Nonvolatile memory
- High speed
- High density
- High endurability
- Low power

◆ Some candidates
- PRAM
- STT-MRAM
- FeRAM
- ReRAM
- …….



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Future of NAND Flash

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Invention of NAND Flash

ABSTRACT

A NAND structure cell is most promising as an ultra high density EEPROM to replace magnetic memories. This paper describes a new device technology to realize a high performance 4Mb EEPROM with NAND structure cell. The main features of the technology are a new NAND structure cell to realize wide threshold window and high reliability, and a high voltage CMOS process to realize program and erase operations,which require high voltage pulses,such as 22V.

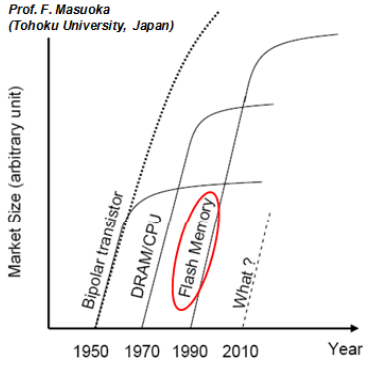
By using 1.0um design rules, the unit cell area per bit is 12.9um^2, which is small enough to realize a 4Mb EEPROM.

INTRODUCTION

In order to replace magnetic memories by solid state devices, a high density EEPROM has been required. Conventional 5V-only EEPROMs, utilizing Fowler-Nordheim tunneling, occupy a very large

by Toshiba, IEDM, 1988

Inventor:
Prof. F. Masuoka
(Tohoku University, Japan)



by Toshiba, Flash handbook, 1992

Application I / Flash Cards

◆ Flash card is used for mobile devices with memory slot

Digital camera

Portable Video game

PC

Cellular phone

Car navigation

Application II / Embedded Application

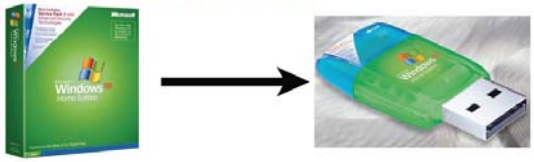
MP3 player

E-Book

Application III / Contents Preloaded Media

Sun

Software Distribution



- Distribute Software as a read-only device
  - > No Viruses
- O/S and Bios already support optical drives
  - > 100% emulation of CD/DVD drive
- Less packaging
- Perfect Application for 3/4bit MLC
- <$5 unit cost

Santa Clara, CA USA
August 2009

Application IV / SSD

Samsung 256GB SSD

SATA interface

compatibility

SATA interface

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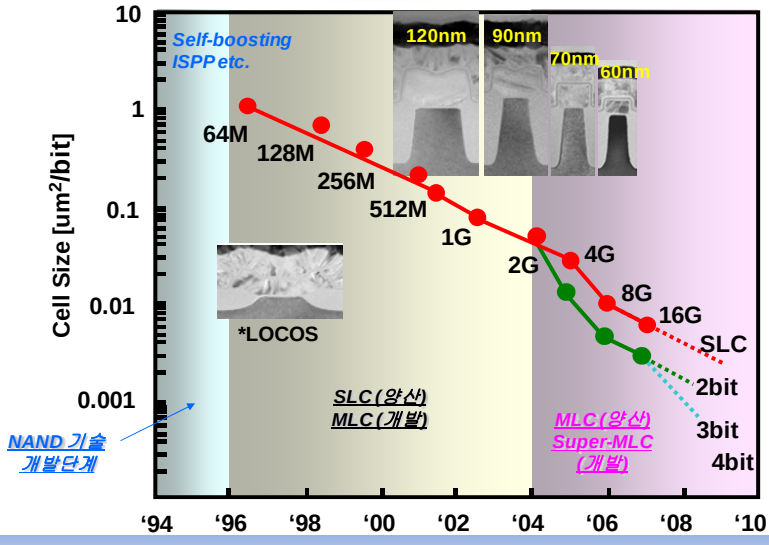
Evolution of NAND Flash Technology



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Limitation of NAND

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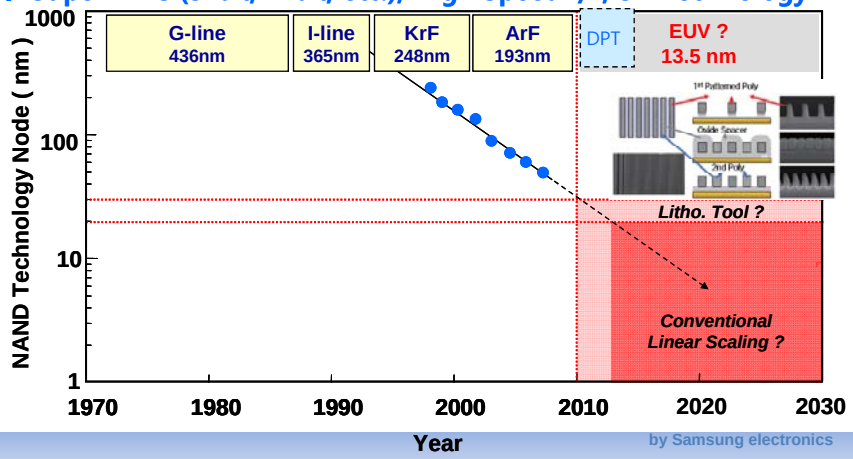
- Beyond 30nm, Uncertainty of EUV Availability → Limit of Patterning
- Beyond 20nm, Uncertainty of Conv. Linear Scaling → Limit of Device

→ **Super-MLC (3-bit, 4-bit, etc.), High Speed I/F, 3D Technology**



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Super-MLC (3-bit, 4-bit, ...)

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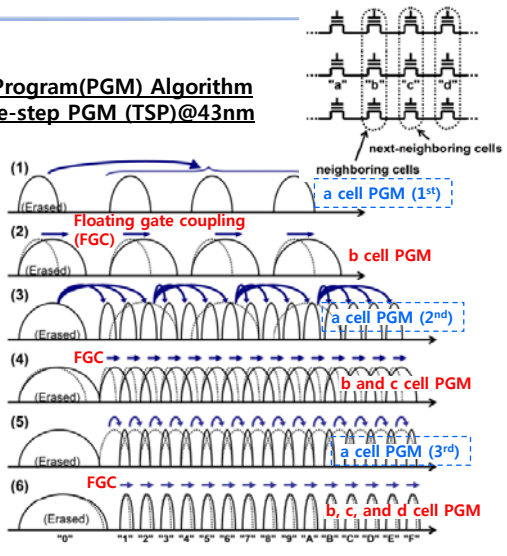
Bits per Cell	4
Density	64Gb
Organization	8KB / Page 4 Pages / WL 64 WL / Block 2k Blocks / Plane 2 Planes
Block Size	2MB (4M Cells)
Architecture	ABL
Program Performance	5.6MB/s
Burst Cycle Time	25ns
Power Supply	2.7 to 3.6V
Technology	3M 43nm CMOS
Die Size	244.45mm²

New Program(PGM) Algorithm
: Three-step PGM (TSP)@43nm



by Toshiba-Sandisk, ISSCC, 2009

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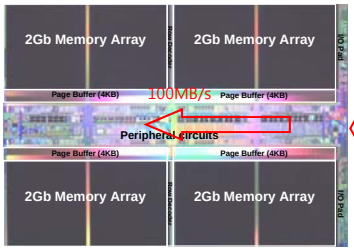
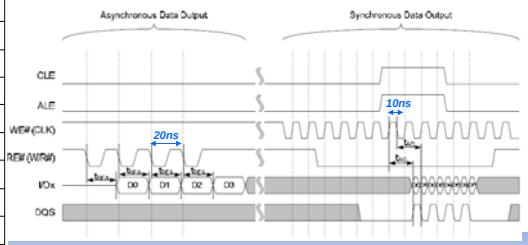
High Speed Interface (DDR) NAND



200MB/s

→ ONFI (Open NAND Flash Interface)
: Intel, Micron, Hynix, etc.
→ Toggle-mode NAND
: Samsung, Toshiba

Technology	30nm p-sub CMOS triple-well 3metal
Cell size	0.011μm² (effective)
Chip size	169.5mm²
Organization	4096 x 128 pages x 512 blocks x 4 planes x 8
Power supply: Vcc	2.7V-3.6V
Power supply: VccQ	1.7V-1.95V or 2.7V-3.6V
Read time	30μs
Program time	160μs (typical)
Erase time	3ms (typical)
Clock cycle time	10ns
I/O width	x8



by Micron-Intel, ISSSC, 2008

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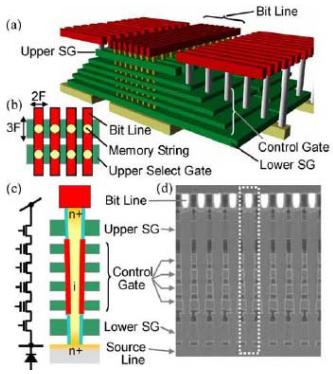
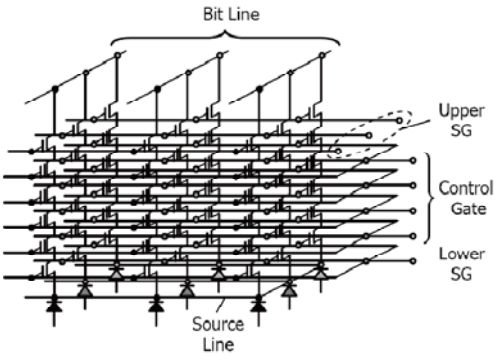
3D NAND for Tera-bit Storage

- 3D Vertical NAND
- High Density Oriented, CTF, MLC



by Toshiba, IEDM, 2007



by Toshiba, VLSI, 2007

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SDD vs. HDD

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	2.5" SATA 3.0Gbps SSD		2.5" SATA 3.0Gbps HDD
	Solid NAND flash based	Mechanism type	Magnetic rotating platters
	64GB	Density	80GB
Low weight	73g	Weight	365g
High performance	Read: 100MB/s, Write :80MB/s	Performance	Read: 59MB/s, Write: 60MB/s
Low power	1W	Active Power consumption	3.86W
Low vibration	20G (10~2000Hz)	Operating Vibration	0.5G (22~350Hz)
	1,500G for 0.5ms	Shock resistance	170G for 0.5ms
	0°C to 70°C	Operating temperature	5°C to 55°C
Low noise	None	Acoustic Noise	0.3 dB
Low endurance	MTBF >2M hours	Endurance	MTBF < 0.7M hours

However, high cost per capacity, now

by Samsung electronics

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Component of SSD

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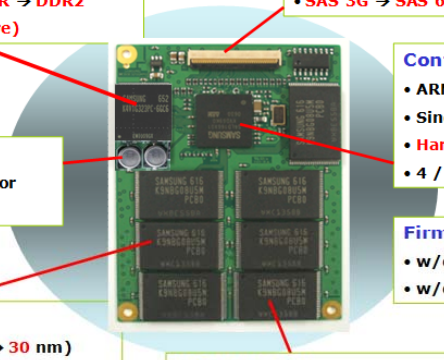
◆ Performance = f(CPU, DRAM, Flash, Host Interface, HW automation)

DRAM
- 32 → 128 → 1024 MB
- Mobile SDRAM → DDR → DDR2
- PRAM / FRAM (Future)

Host Interface
- PATA → SATA 3G → SATA 6G (Note PC)
- SAS 3G → SAS 6G (Server / Storage)



Controller
- ARM CPU (133 → 300 MHz)
- Single / Duo Core CPU
- Hardware Acceleration
- 4 / 8 / 16 ch. (NAND I/F)

Power Supply
- Power-Failure Monitor
- Super Cap

Firmware
- w/o OS → Real Time OS
- w/o Queue → Queued CMD

NAND Flash
- SLC/MLC (50 → 40 → 30 nm)
- SDR I/F (40 MB/s/chip)
- DDR I/F (133 → 266, → ... MB/s)

SSD Capacity
- 32 / 64 / 128 / 256 / 512 GB

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SSD / Solving the I/O Bottleneck

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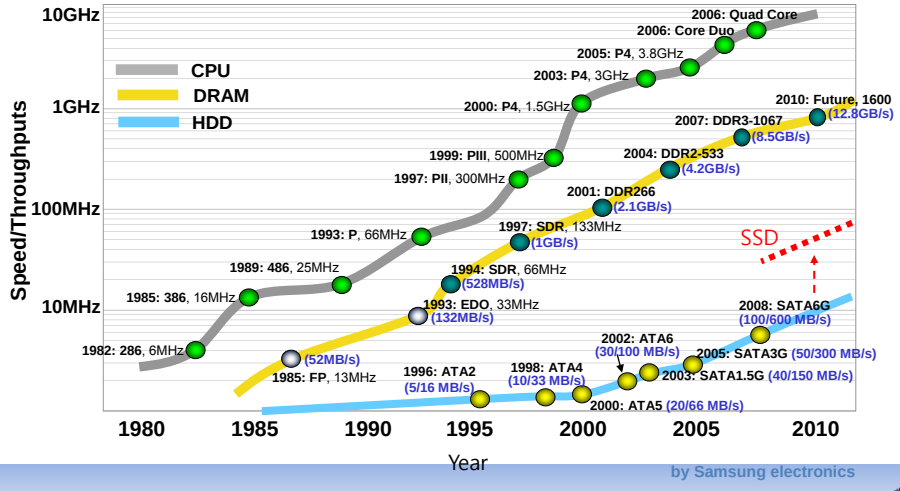
◆ Bridge Performance Gap between CPU and HDD

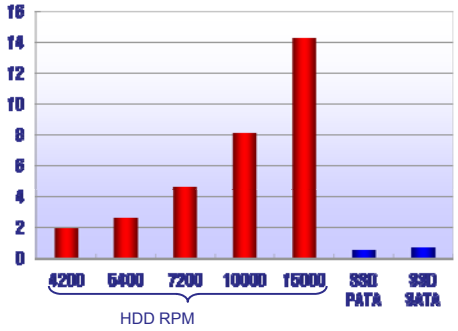


SSD / Solving the Power Bottleneck

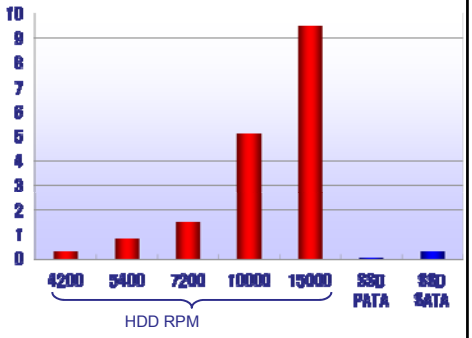
VLSI SYSTEM LAB.

◆ HDD: Higher RPM = Higher Power + Generates more Heat
◆ SSD: Less Power /No Heat saves lifetime Energy Costs…

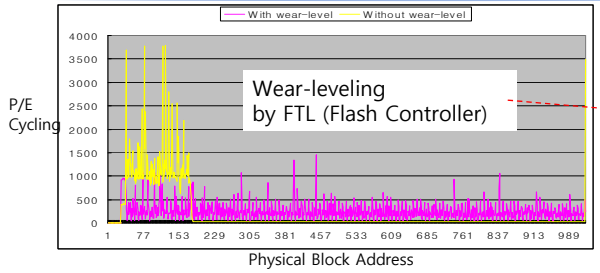
Watts used in Operation Mode

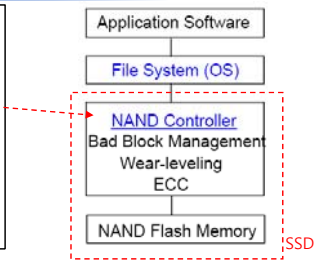


Watts used in Idle Mode

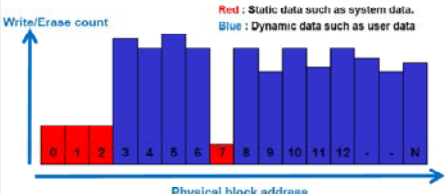


Wear-leveling for Optimization

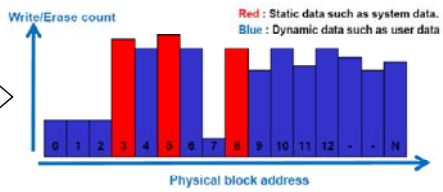




Dynamic Wear-leveling



Static Wear-leveling



MP3, USB, DSC etc.

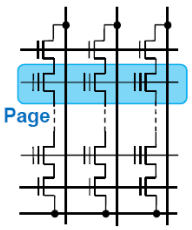
SSD

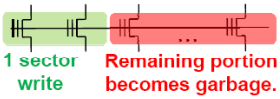
by Samsung electronics

Sector Size for Optimization

◆ Existing OS is for HDD! → OS should be optimized for SSD!!!

- **Sector size optimization**
  - Minimum write/read unit of NAND is a page.
  - Typical page size is 4-8KByte.
  - A page is written only ONCE to avoid the program disturbance.
  - With current OS having 512Byte sector, one sector write wastes >80% of data in a page.





  - LBD(Long Block Data) sector standard (Windows Vista) : 4KByte sector size fits better with SSD.
  - As the page size increases as NAND is shrinking, larger sector size such as 64KByte or 128KByte is required.

by K. Takeuchi, ISSCC Forum, 2008

Self-monitoring, Analysis and Reporting Technology

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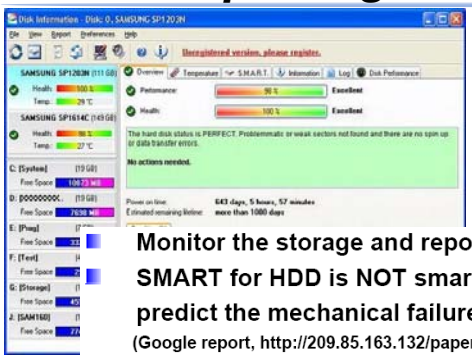

✓ SMART
(Self-Monitoring, Analysis and Reporting Technology)

- Monitor the storage and report/predict the failure.
- SMART for HDD is NOT smart because it is very difficult to predict the mechanical failure.
  (Google report, http://209.85.163.132/papers/disk_failures.pdf)

- SMART for SSD can be really smart.
- Product lifetime can be predicted because the failure rate is highly correlated with the write/erase cycles.
  - Predict the SSD lifetime by monitoring the write/erase cycles and replace SSD before the fatal failure occurs.

Universal Memory

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Power Dissipation of IT Equipments

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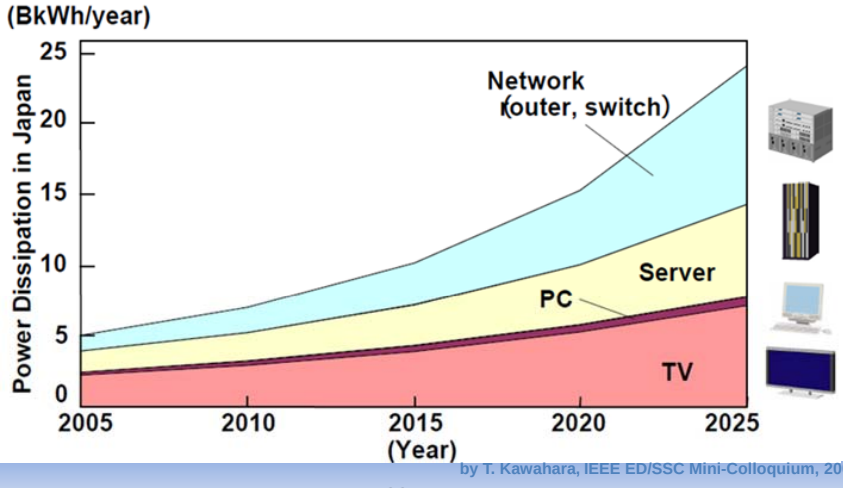
- In 2025, Power dissipation will reach 5 times larger.



by T. Kawahara, IEEE ED/SSC Mini-Colloquium, 2009

Normally OFF, Instant ON

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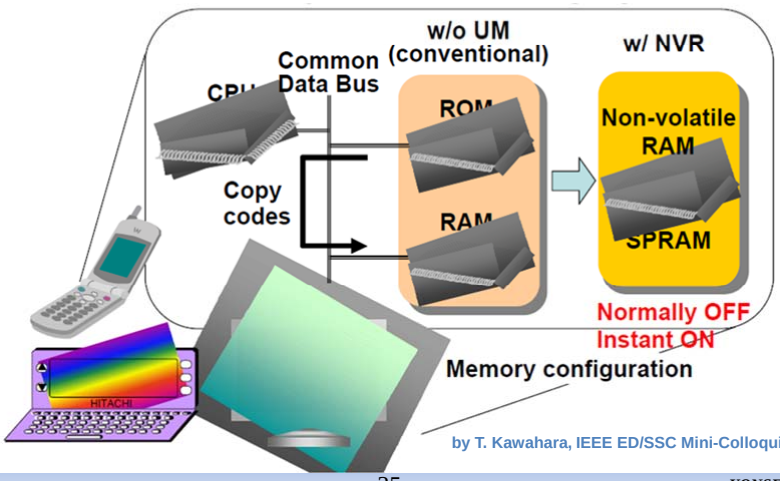
- Read operation ; sensing resistance of GST
- Voltage biased to GST must to limited under V_{th} to prevent disturb.
- Current sensing scheme
  - Appling read voltage to cell converts from resistance to current
  - Load device converts from current to voltage
  - Sense amplifier converts from analog voltage value to digital output

by T. Kawahara, IEEE ED/SSC Mini-Colloquium, 2009

Change Memory Configuration

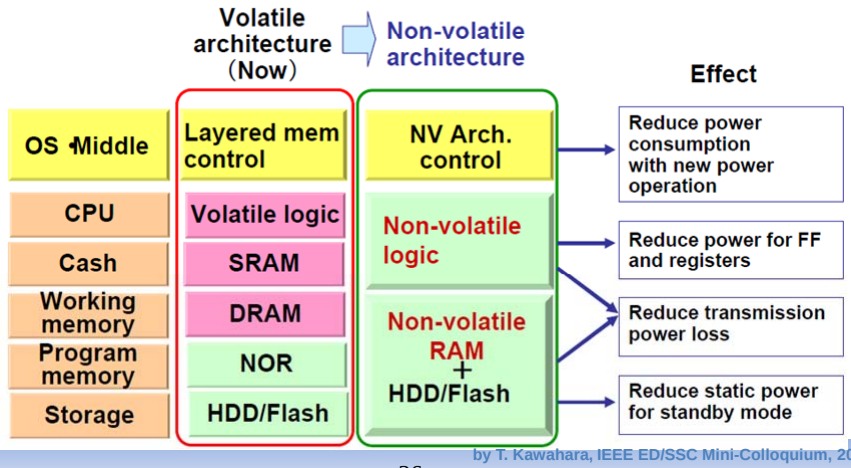
- Nonvolatile RAM enhances user's convenience.
- Instant ON. Quickly software changing.



by T. Kawahara, IEEE ED/SSC Mini-Colloquium, 2009

Nonvolatile (NV) RAM Application

- Innovation for low power system including hardware, software, and architecture



by T. Kawahara, IEEE ED/SSC Mini-Colloquium, 2009

Impact on Performance

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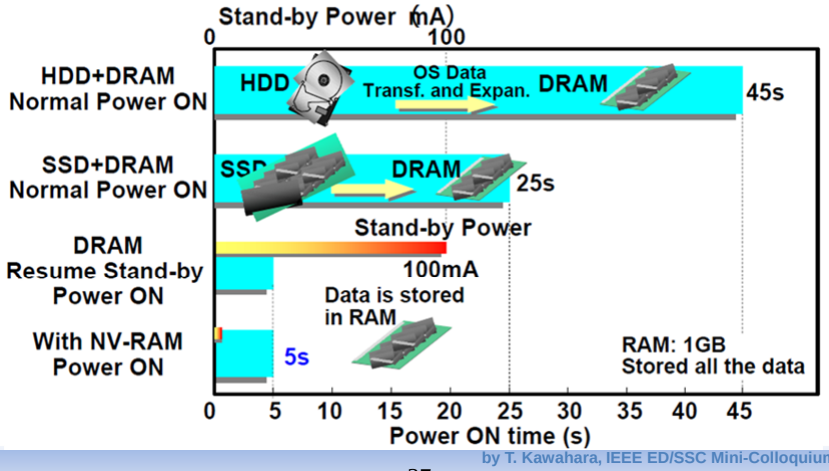
- Power ON time is improved to 1/9.
- Nonvolatility achieves low power also.



Impact on Power

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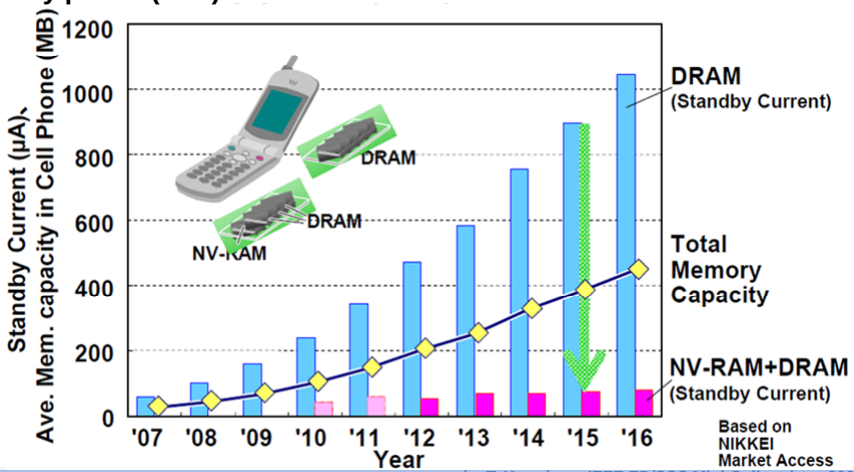
- High-end cellular phone with large memory with low stand-by power (1/10).



Universal Memory I
PRAM

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Structure of PRAM Cell

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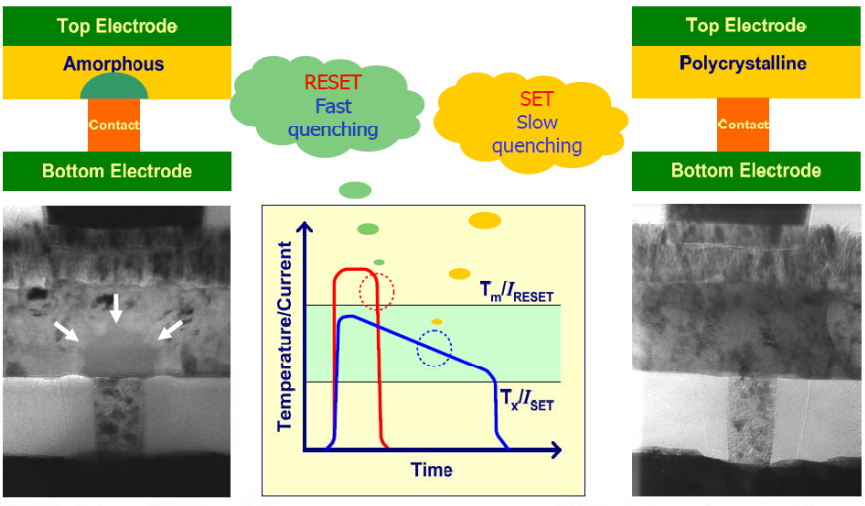

RESET state = High resistance

SET state = Low resistance

by Samsung electronics

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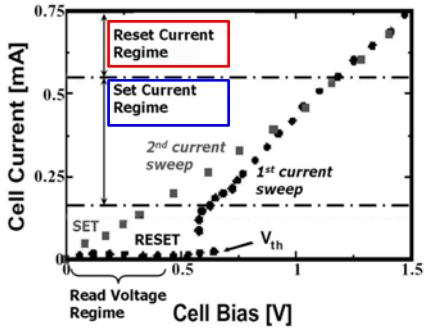
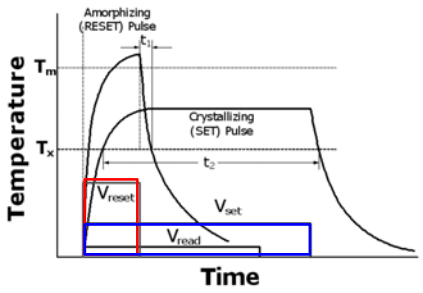
Write Operation of PRAM

VLSI SYSTEM LAB.

- Reset pulse (strong & short) ; Amorphous state (~100kΩ)
- Set pulse (weak & long) ; Crystalline state (kΩ)



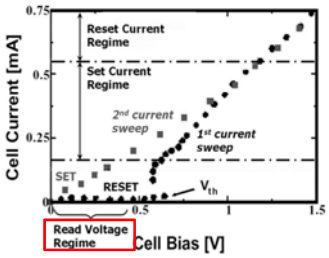


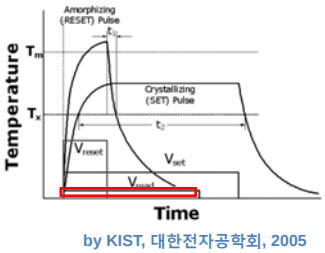
by KIST, 대한전자공학회, 2005

Read Operation of PRAM

VLSI SYSTEM LAB.

- Read operation ; sensing resistance of GST
- Voltage biased to GST must to limited under V_{th} to prevent disturb.
- Current sensing scheme
  - Appling read voltage to cell converts from resistance to current
  - Load device converts from current to voltage
  - Sense amplifier converts from analog voltage value to digital output





by KIST, 대한전자공학회, 2005

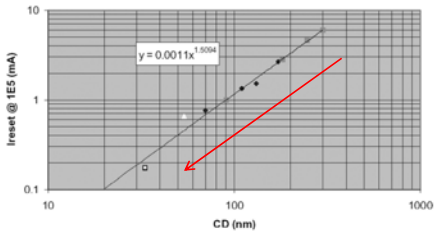
Recent Technical Issues

Reducing Required RESET Current

VLSI SYSTEM LAB.

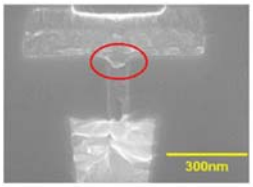
◆ Reducing BEC

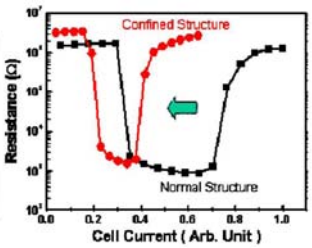
Increasing heat
by increasing
current density
→ reducing I_{RESET}



◆ Confined contact

Increasing heat
by increasing
current density
→ reducing I_{RESET}





by Samsung Electronics, Sym. VLSI Tech., 2007

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Recent Technical Issues

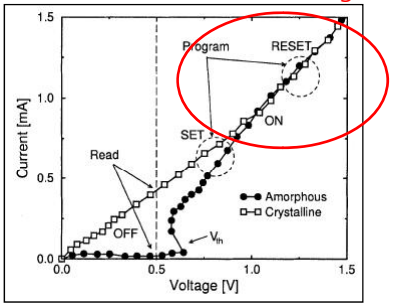
Reducing Required RESET Current

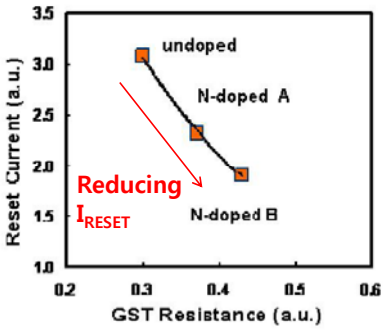
VLSI SYSTEM LAB.

◆ Impurity doping

Increasing GST resistance
→ increasing heat
→ reducing I_{RESET}

Reset Current Regime





by Samsung Electronics, Sym. VLSI Tech., 2007

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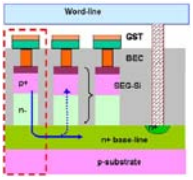
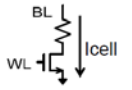
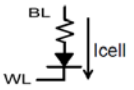
Recent Technical Issues

Obtaining Larger RESET Current

VLSI SYSTEM LAB.

◆ Enhancing current driving capability
- Vertical BJT



	256 Mb PRAM Cell ISSCC2006	512Mb PRAM Cell ISSCC2007
Unit Cell Structure		
Switch Device	(3-terminal) MOS Switch	(2-terminal) Diode Switch
Process Tech.	100nm	90nm
Cell Size	0.166mm² (16.6F²)	0.0467mm² (5.8F²)
Switch Device Capability	6 mA/mm² @ V_{ds}=1.5V, V_{gs}=3.0V	21mA/mm² @ V_{diode}=1.5V
Integration Density (Chip Size)	256 Mb (79.2 mm²)	512Mb (91.5 mm²)

by Samsung Electronics

History of PRAM

VLSI SYSTEM LAB.

- **2000**
  - STMicroelectronics obtained license about CD-ROM from Ovonyx an d started researching with Ovonyx to develop PRAM.
- **2002**
  - Intel and Ovonyx are developed 4Mb PRAM
- **2004**
  - STMicroelectronics developed 8Mb PRAM using 0.18um tech.
  - Samsung developed 64Mb PRAM using 0.18um tech.
- **2005**
  - Samsung developed 256Mb PRAM.

History of PRAM

- **2007**
  - **Samsung** developed 512Mb PRAM using 90nm tech. (using N-doped GST, vertical BJT)
  - **Hynix** obtained license about PRAM from Ovonyx.
  - **Numonyx** developed 128Mb PRAM.
- **2008**
  - **Numonyx** developed 128Mb PRAM with multi level cell(MLC).
- **2010**
  - **Numonyx** developed 1Gb PRAM.

Future of PRAM

◆ When ?? 2010 ?
- **Samsung** and **Numonyx** expect to possess technology to mass-produce 512Mb~1Gb PRAM.
- Absence of alternative market is obstacle of commercialization of PRAM.
- **Samsung** or **Numonyx** may launch PRAM in 2010.

◆ Target !! NOR Flash !!
- Recently, improvement of NOR flash disturbs commercialization of PRAM.
- Main product of NOR flash is 256, 512Mb and uses for embedded system.

◆ Future !!
- SSD drive
- System that don't need booting

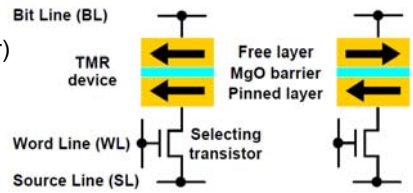
Universal Memory II
STT-MRAM

VLSI
SYSTEM LAB.

MTJ Device Structure

VLSI SYSTEM LAB.

◆ MTJ
- Two magnetic layer(Free and pinned layer)
- Insulating layer(Tunnel barrier)



◆ R_{MTJ} ; depends on the state of free layer

	State	Effective resistance
Parallel	0	Low (R_0)
Anti-Parallel	1	High ($R_1=R_0*(1+MR)$)

(MR ; magnetoresistance)

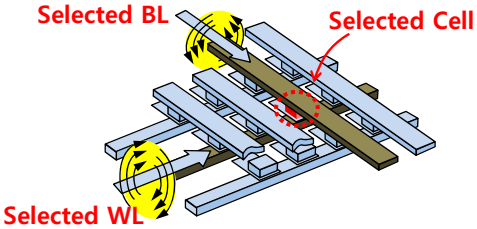
Reading operation ➡ Reading resistance of MTJ

Writing operation ➡ Switching free layer of MTJ

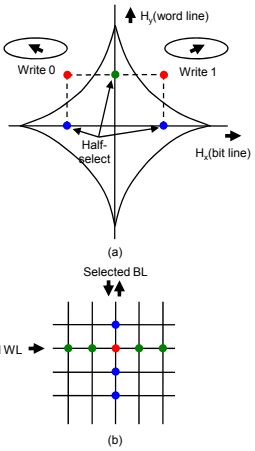
Write Operation of Conventional MRAM

VLSI SYSTEM LAB.

◆ Applied Magnetic Fields

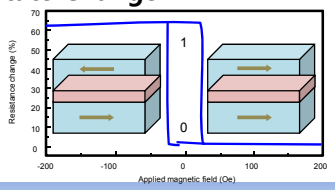


< Applied magnetic field >



< Half selection issue >

◆ State Change



< State change >

T. M. Maffitt, et al., IBM J., 2007

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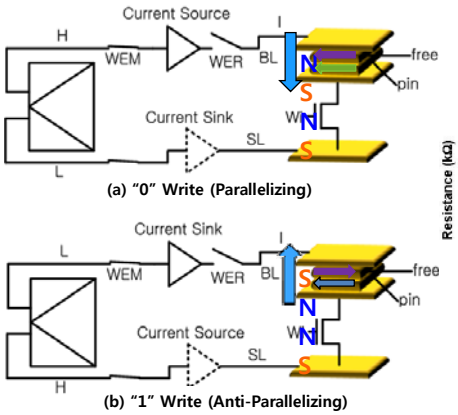
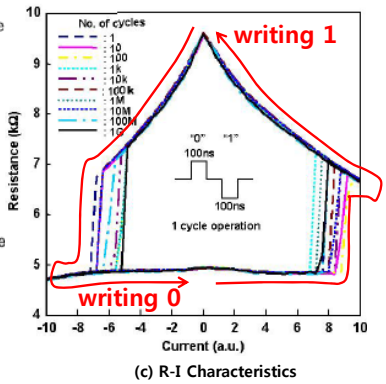
Write Operation of STT-MRAM

VLSI SYSTEM LAB.

◆ Spin-polarized electron





< Parallelizing and Anti-Parallelizing Current>

by T. Kawahara, et al., ISSCC, 2007

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Conventional MRAM vs. STT-MRAM

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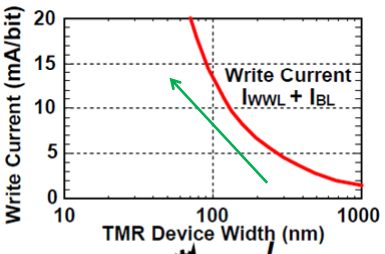
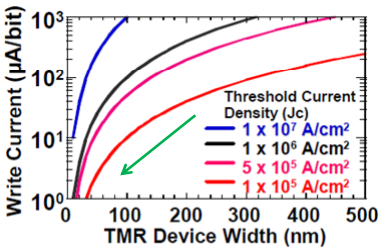
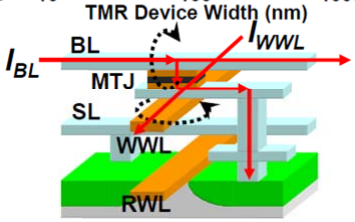
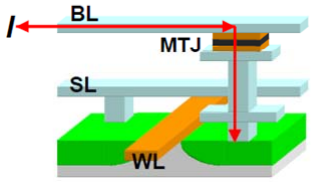
◆STT-MRAM has good potential in scalability due to Write current.







Conventional MRAM



STT-MRAM

by Samsung electronics

Recent Technical Issues

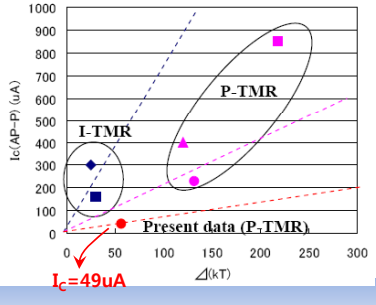
Reducing Required Critical Current

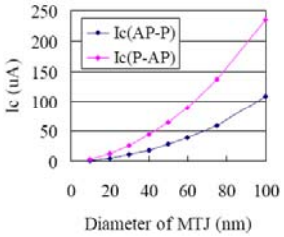
VLSI SYSTEM LAB.

◆Perpendicular MTJ

- TMR element with perpendicular magnetic anisotropy (P-TMR)
- Lower critical current than I-TMR

Research Group	Conference	MTJ size (diameter)	Critical current	Switching time
Toshiba	IEDM2008	55nm	49uA (AP-P) 100uA (P-AP)	4ns





Critical current (I_C) of P-ST is dependent on MTJ size. (opposite result compared with page 2)

by T. Kishi, et al., IEDM, 2008

Recent Technical Issues

Obtaining Larger Write Current

◆2 Transistor – 1 MTJ (2T1MTJ) cell structure

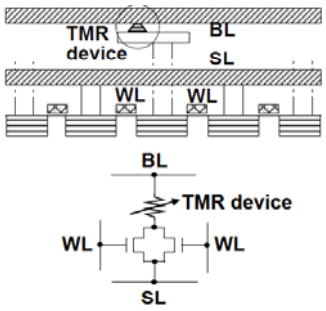


Fig. 1 2T1R Memory Cell

To minimize the cell area, the isolation area between a cell and an adjacent cell is replaced by the adjacent cell's transistor; the "off" state of the channel region of the adjacent cell can insulate electrically among memory cells.

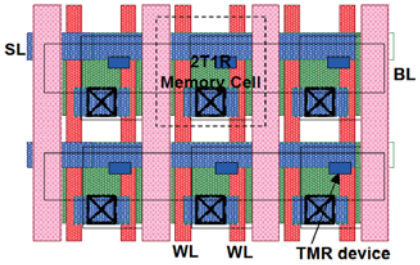


Fig. 2 Cell Layout

Larger write current with same area

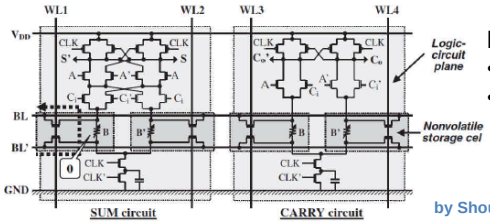
by R. Takemura, et al., Symposium on VLSI circuits, 2009

NEW Application using MTJ

Spintronics Logic

◆ Recently, nonvolatile logic using MTJ had been studied.

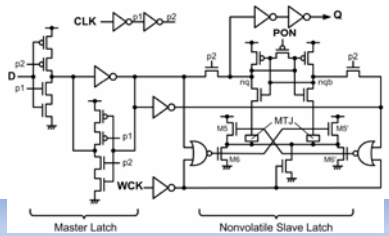
◆ Highly expected for LSI advancement and innovation.



Full adder with nonvolatile input B

- Dynamic logic type
- Dynamic power can reduced to 23%

by Shoun Matsunage, et al., Applied Physics Express, 2008



Nonvolatile Flip-flop

- Cross-coupled inverter latch type
- Standby power can reduced to 0%

by Noboru Sakimura, et al., CICC, 2008

Power Reduction by STT-MRAM and Spintronics Logic

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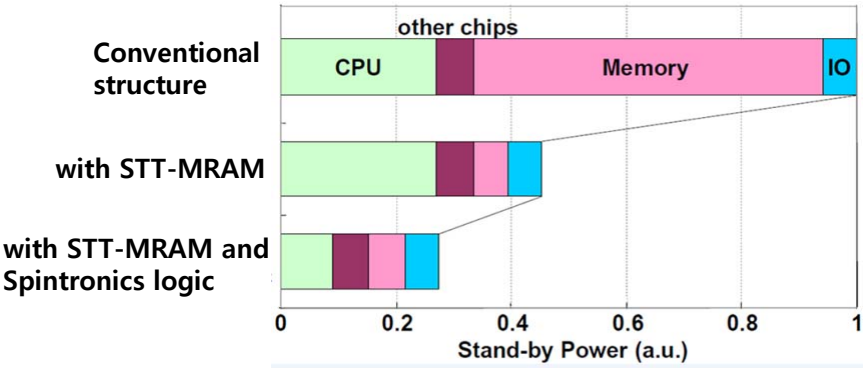
- Keep normally the equipment turned off.
- Power consumption adjusted to one third.



by T. Kawahara, IEEE ED/SSC Mini-Colloquium, 2009

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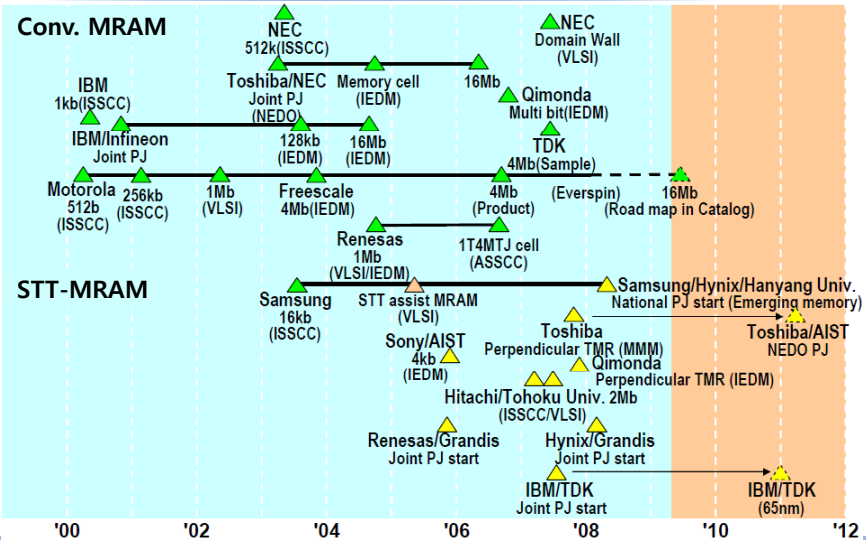
History of STT-MRAM

VLSI SYSTEM LAB.



by T. Kawahara, IEEE ED/SSC Mini-Colloquium, 2009

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Conclusion

VLSI SYSTEM LAB.

- The density and performance of flash memory have been improved by improvement of process and design technology.
- Solid state drive (SSD) is remarkable as alternate storage device. As cost per capacity decreases, SDD will replace HDD, gradually.
- Advantage of SSD
  - Low power
  - High performance
  - No noise & vibration
  - Low heat
- Next generation memory had been studied for overcoming current memory. (PRAM, STT-MRAM, …)
- Requirement for universal memory
  - Nonvolatile
  - Low power
  - High performance
  - High density