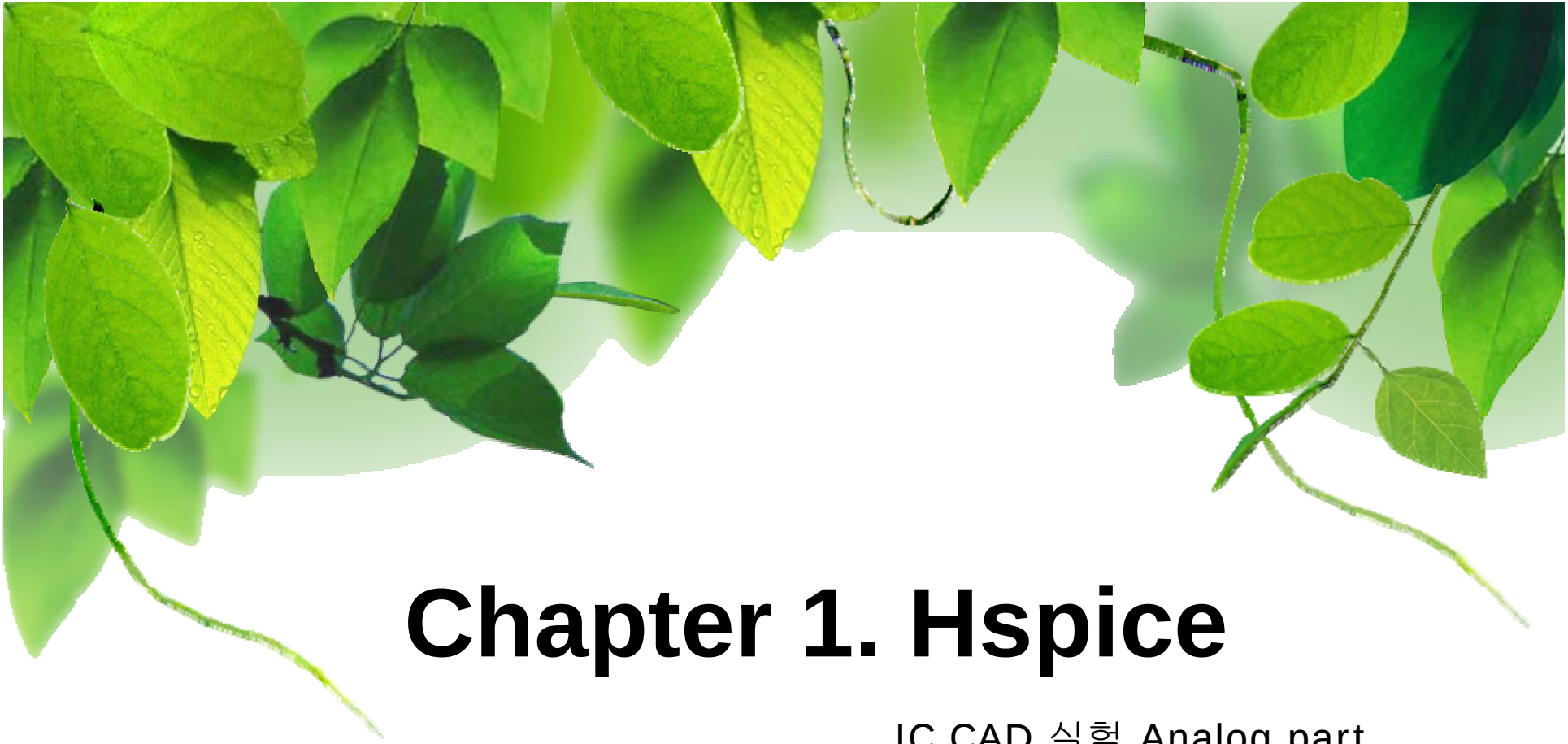

Chapter 1. Hspice

IC CAD 실험 Analog part

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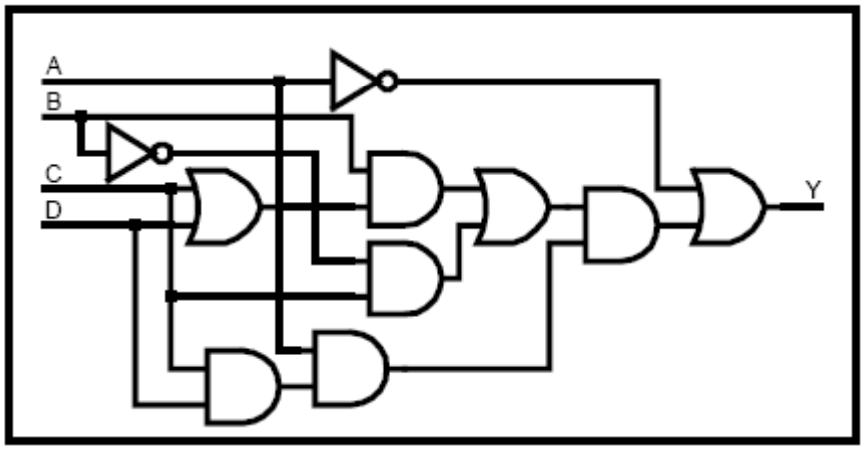
Digital circuit design

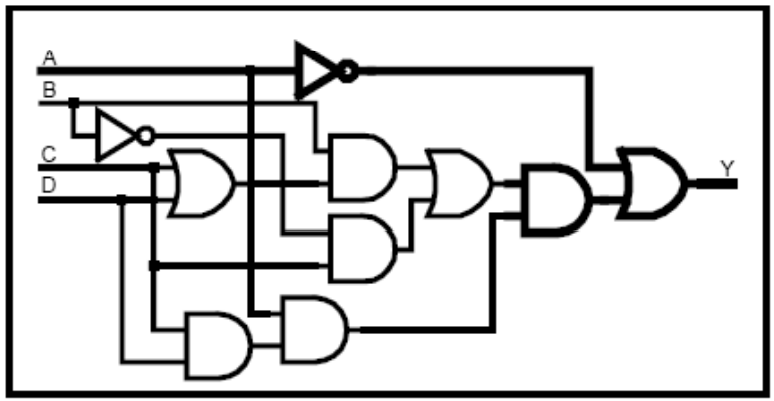
```
if(A == 1)
  Y = C & D;
else if(B==1)
  Y = C | D;
else
  Y = C;
```

RTL description

Synthesis

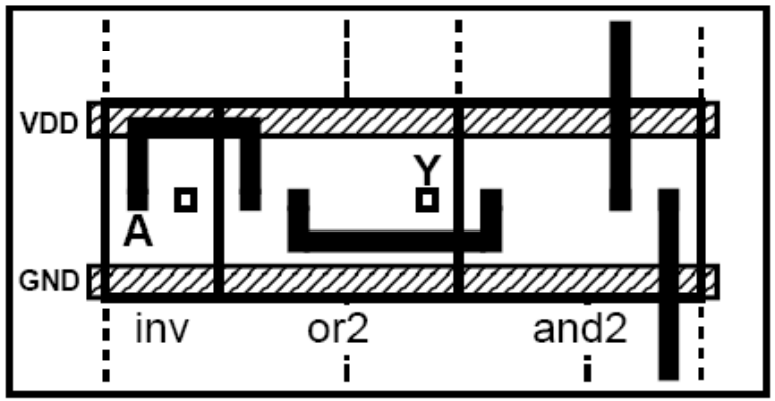


Gate-level netlist



Gate-level netlist

P&R



Layout

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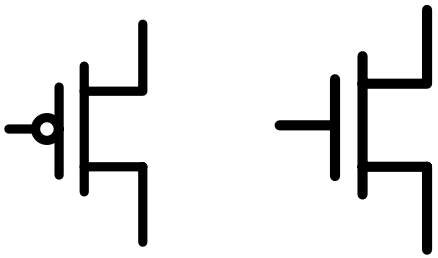
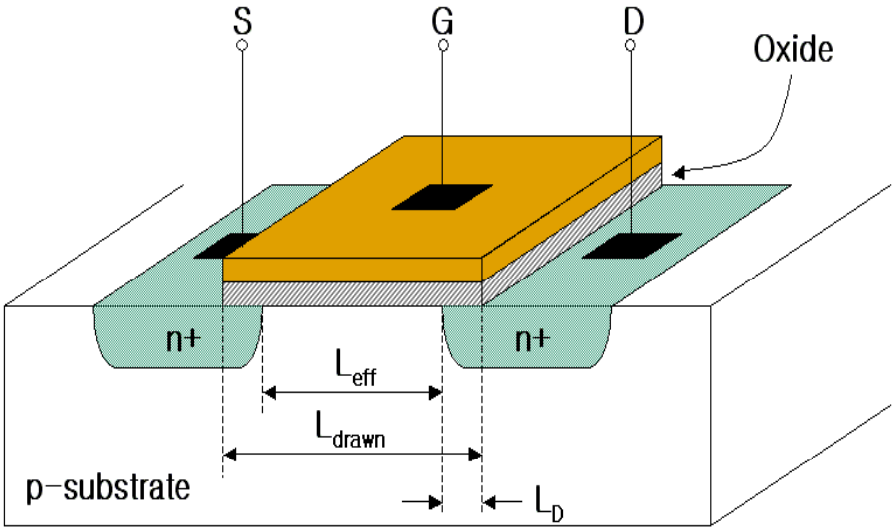
Layout?

MOSFET!

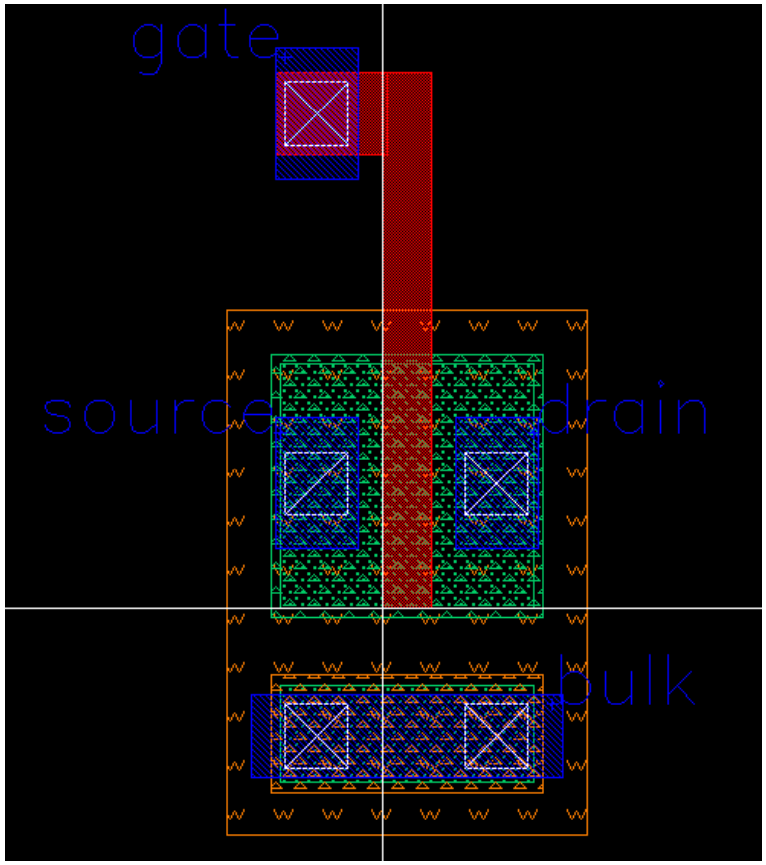
Symbol



Physical structure



Layout



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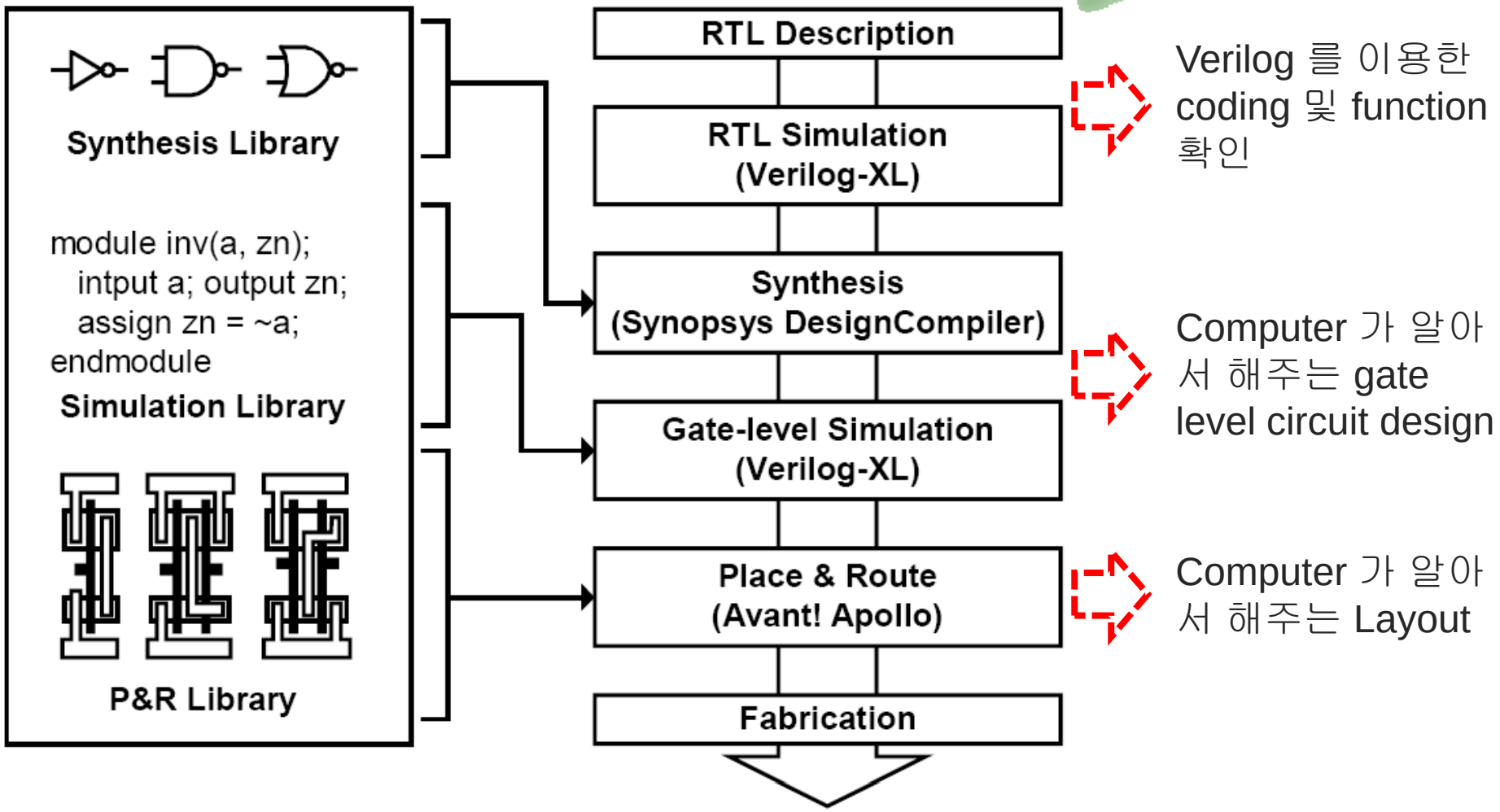
Digital circuit design



Analog circuit design

TR level circuit design

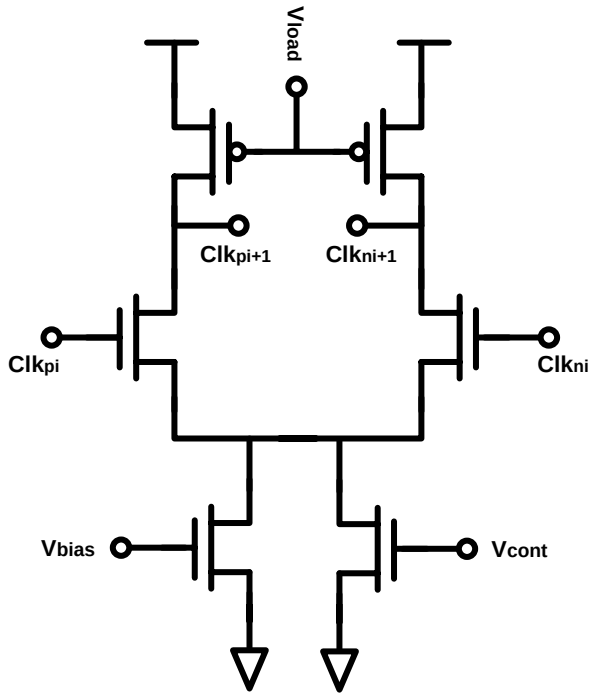
TR level simulation

Layout

Post layout simulation

Fabrication

Hspice, cadence 를 이용한 TR level circuit design & simulation



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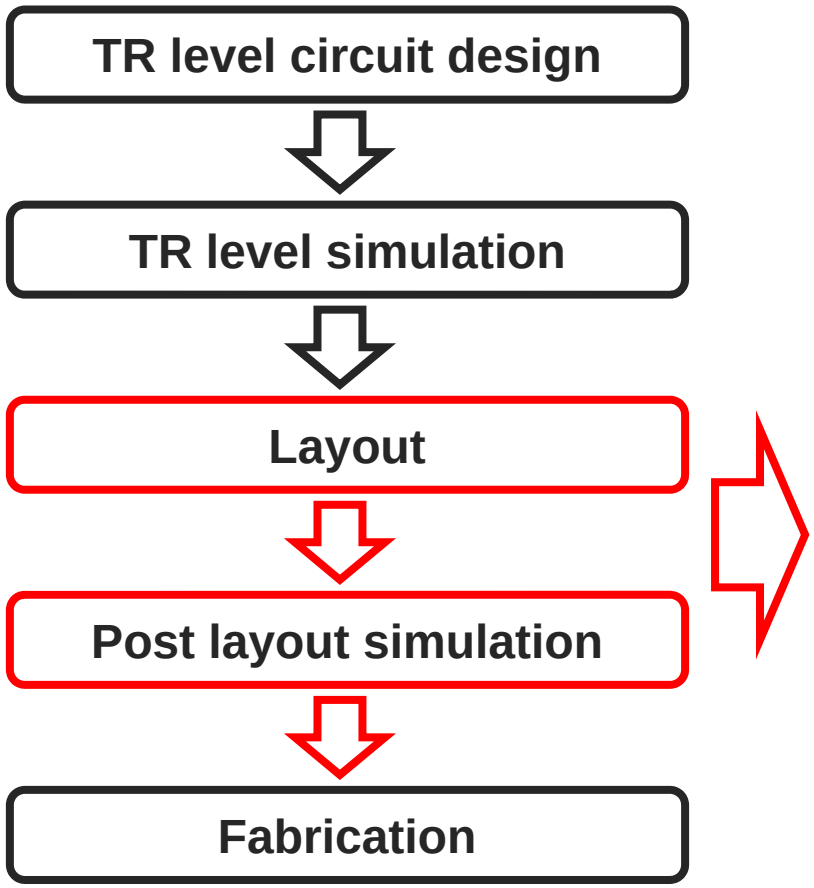
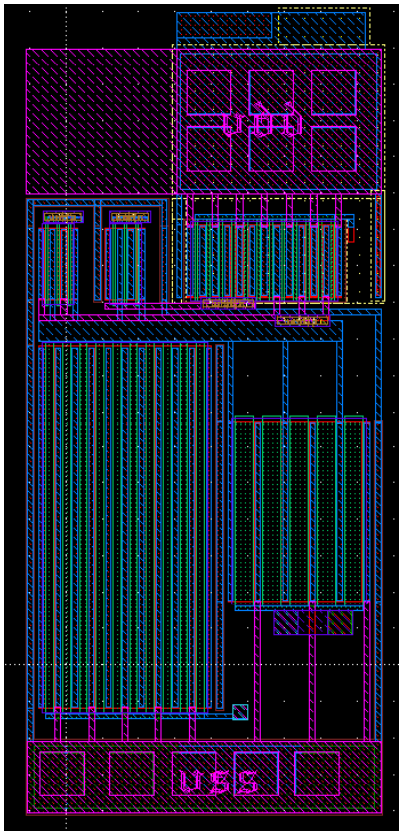
Analog circuit design

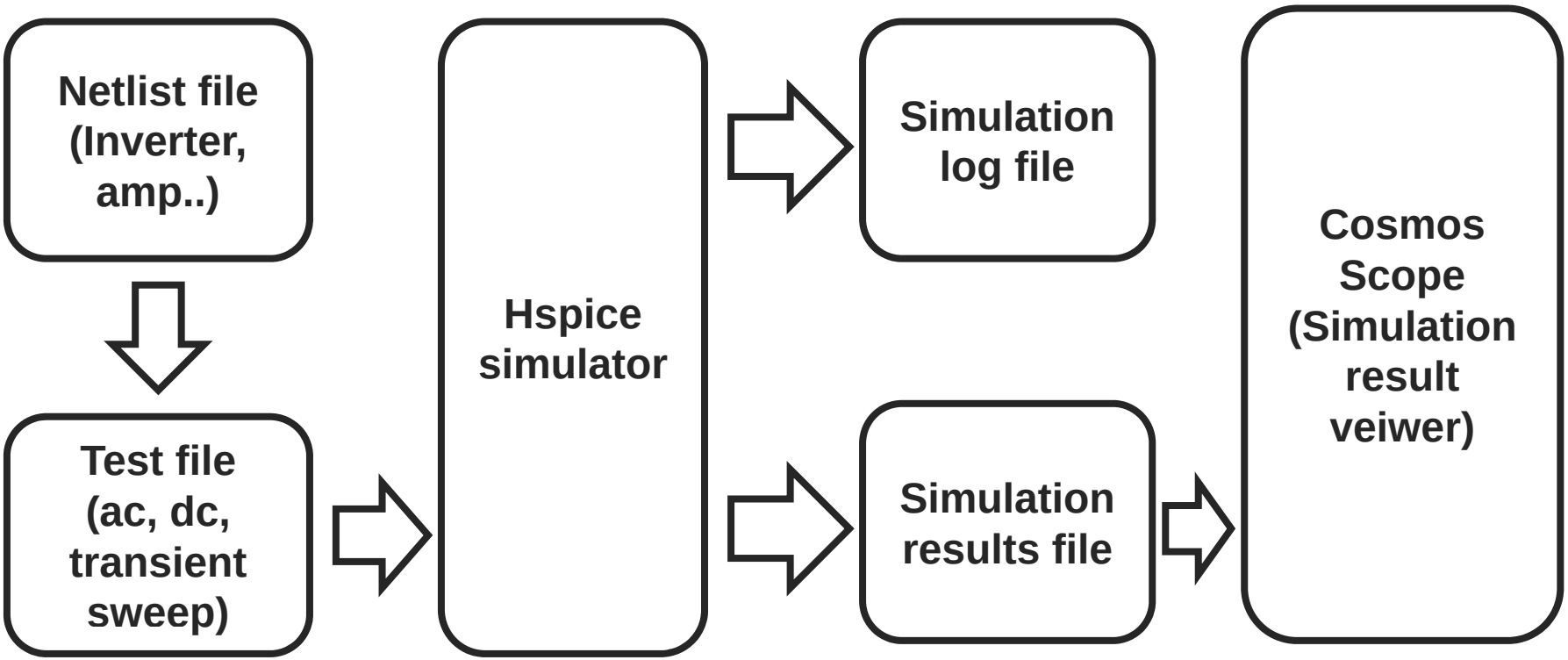


Cadence layout editor 를 이용한 손으로 하는~layout, Hspice, cadence 를 이용한 post layout simulation



Hspice simulation

TR level circuit simulator! – text 기반



Hspice simulation

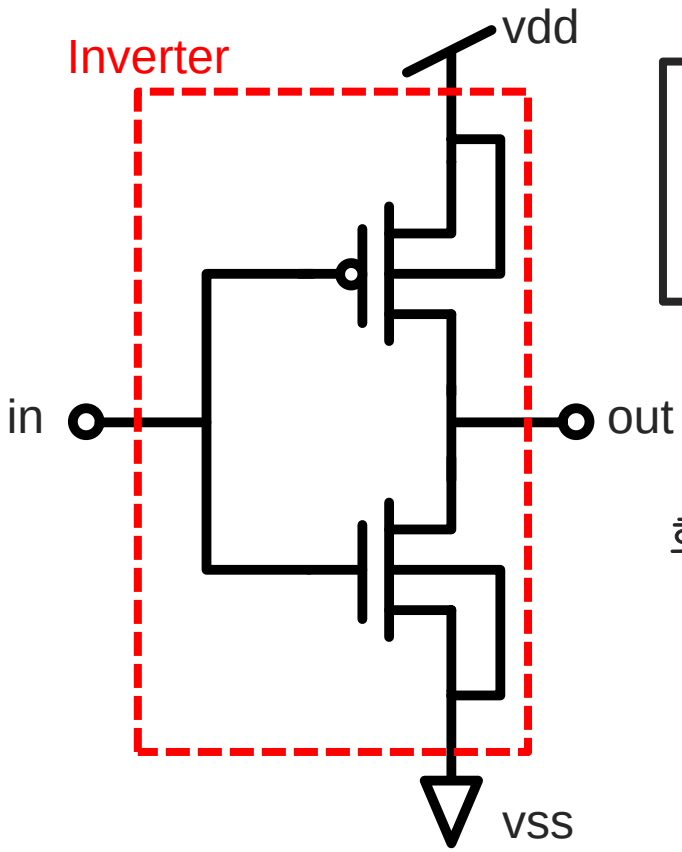
Example> Inverter 설계 및 simulation

[ICCAD@train##]/user1/train##/ > mkdir hspice
[ICCAD@train##]/user1/train##/ > cd hspice
[ICCAD@train##]/user1/train##/ hspice>
cp /user1/master/hspice/netlist.sp .
cp /user1/master/hspice/PMOS_VTL.inc .
cp /user1/master/hspice/NMOS_VTL.inc .
ls

[ICCAD@train##]/user1/train##/ hspice> vi netlist.sp

Hspice simulation

Example> Inverter 설계 및 simulation



Netlist

```
.subckt Inverter out in vdd vss
M_p out in vdd vdd PMOS_VTL w=10u l=0.05u
M_n out in vss vss NMOS_VTL w=5u l=0.05u
.ends
```

.subckt **Inverter** **out** **in** **vdd** **vss**

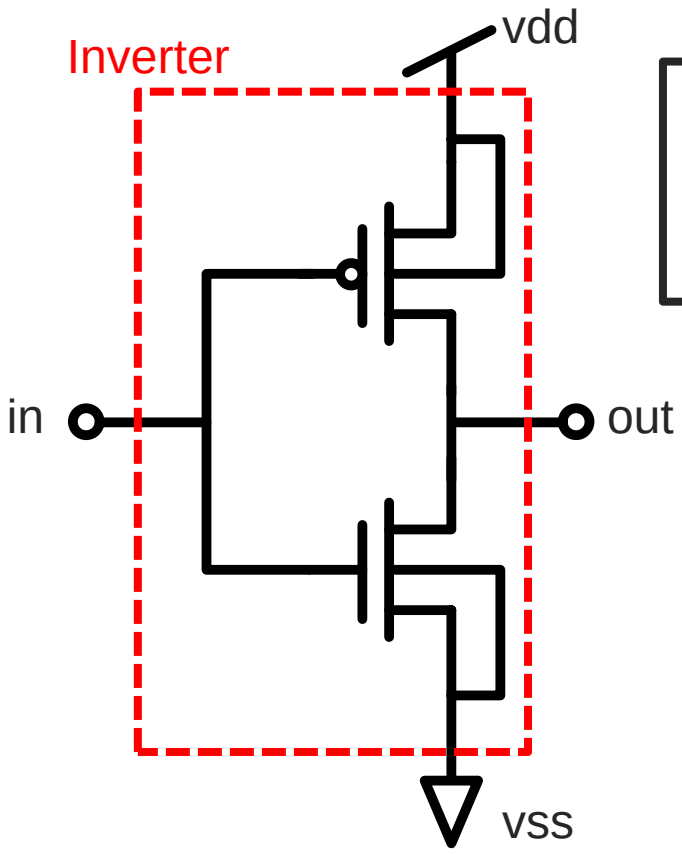
회로 만들기

회로 이름

회로 바깥에서 보이는 **port** 들

Hspice simulation

Example> Inverter 설계 및 simulation



Netlist

```
.subckt Inverter out in vdd vss
M_p out in vdd vdd PMOS_VTL w=10u l=0.05u
M_n out in vss vss NMOS_VTL w=5u l=0.05u
.ends
```

Mosfet 의 이름 | **Drain 의 node 명** | **Gate 의 node 명** | **Source 의 node 명** | **Bulk 의 node 명**

M_p | **out** | **in** | **vdd** | **vdd**

PMOS_VTL | **w=10u** | **l=0.05u**

Mosfet 의 type

Mosfet 의 width 와 length

Inverter 설계 끝!

Hspice simulation

Example> Inverter 설계 및 simulation

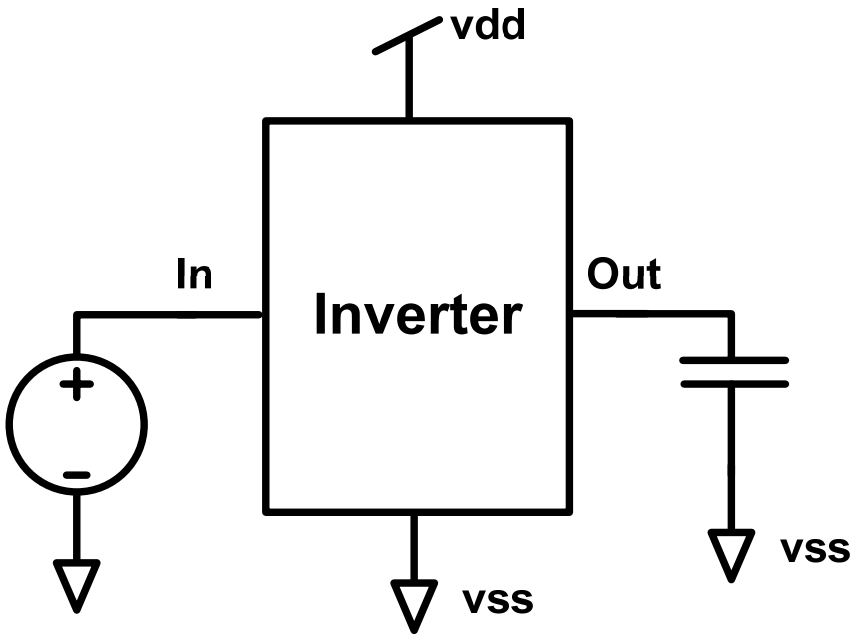
[ICCAD@train##]/user1/train##/ hspice>
cp /user1/master/hspice/inv_sim.sp .

[ICCAD@train##]/user1/train##/ hspice> vi inv_sim.sp

Hspice simulation

Example> Inverter 설계 및 simulation

DC simulation




```
.include 'PMOS_VTL.inc'
.include 'NMOS_VTL.inc'
.include 'netlist.sp'
```

Model 및 만들어 놓은 회로 불러오기

```
.OPTIONS POST NODE LIST

V1 vdd 0 1
V2 vss 0 0
Vin    in     vss    0.5
```

Voltage 정의해 주기

Inverter 라는 회로 불러오기

```
x_inv   out    in     vdd    vss    Inverter
c_out   out    vss    1p
```

Capcitor 정의

```
.dc    Vin    0      1      0.001
.END
```

Vin 이라는 voltage source 를 0.001 단위로 0에서 1까지 변화시키면서 각각의 node 들의 값이 어떻게 되는지 simulation 해라.

Hspice simulation

Example> Inverter 설계 및 simulation

[ICCAD@train##]/user1/train##/ hspice>
hspice inv_sim.sp > a.lis &

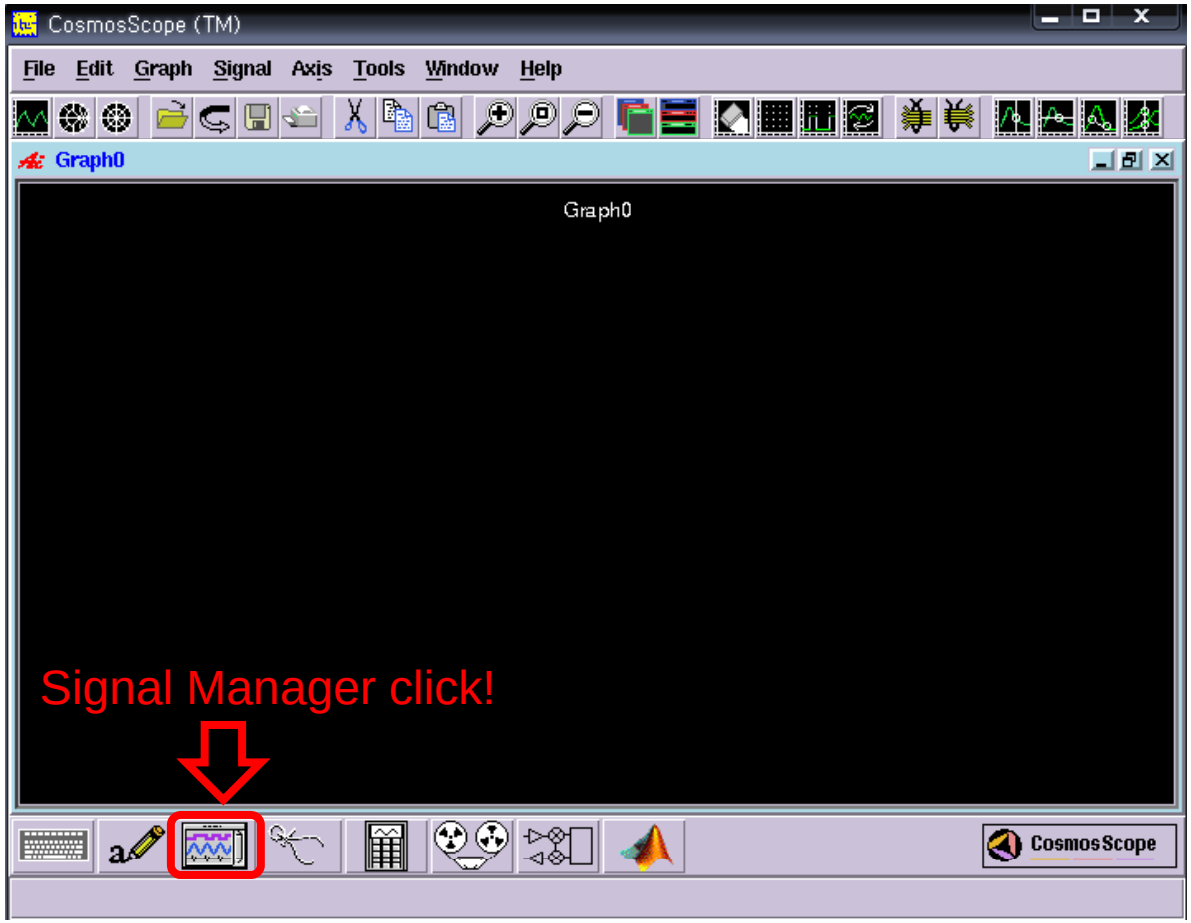
[ICCAD@train##]/user1/train##/ hspice> >info :
**** hspice jab concluded

[ICCAD@train##]/user1/train##/ hspice> cscope &

Hspice simulation

Example> Inverter 설계 및 simulation

파형 확인하기



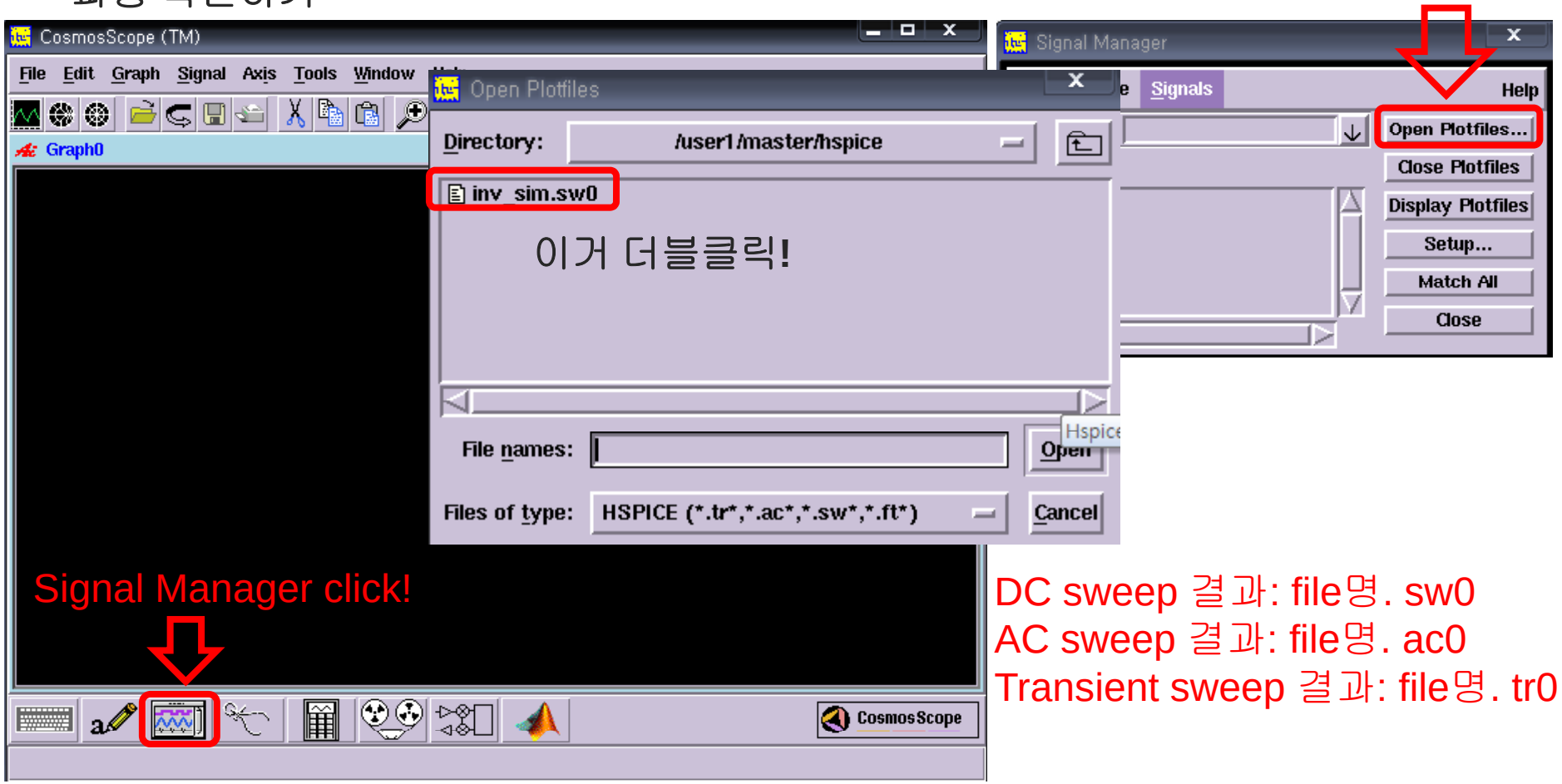
파형 열어보자!

Hspice simulation

Example> Inverter 설계 및 simulation

파형 확인하기

파형 열어보자!



DC sweep 결과: file명. sw0
AC sweep 결과: file명. ac0
Transient sweep 결과: file명. tr0

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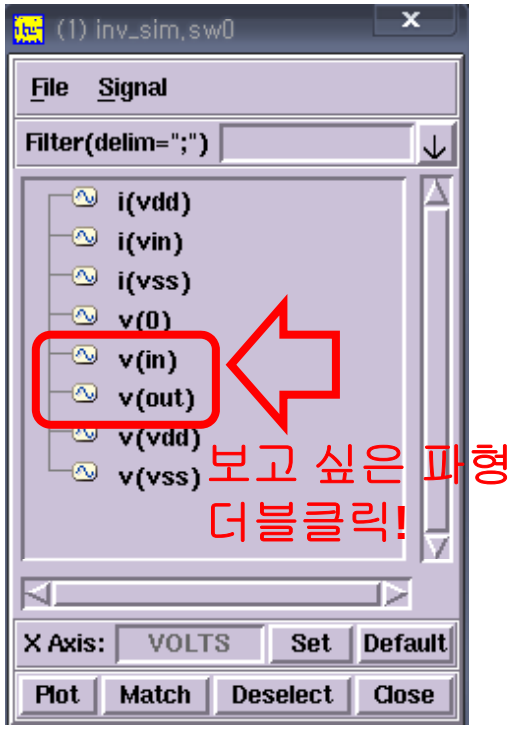
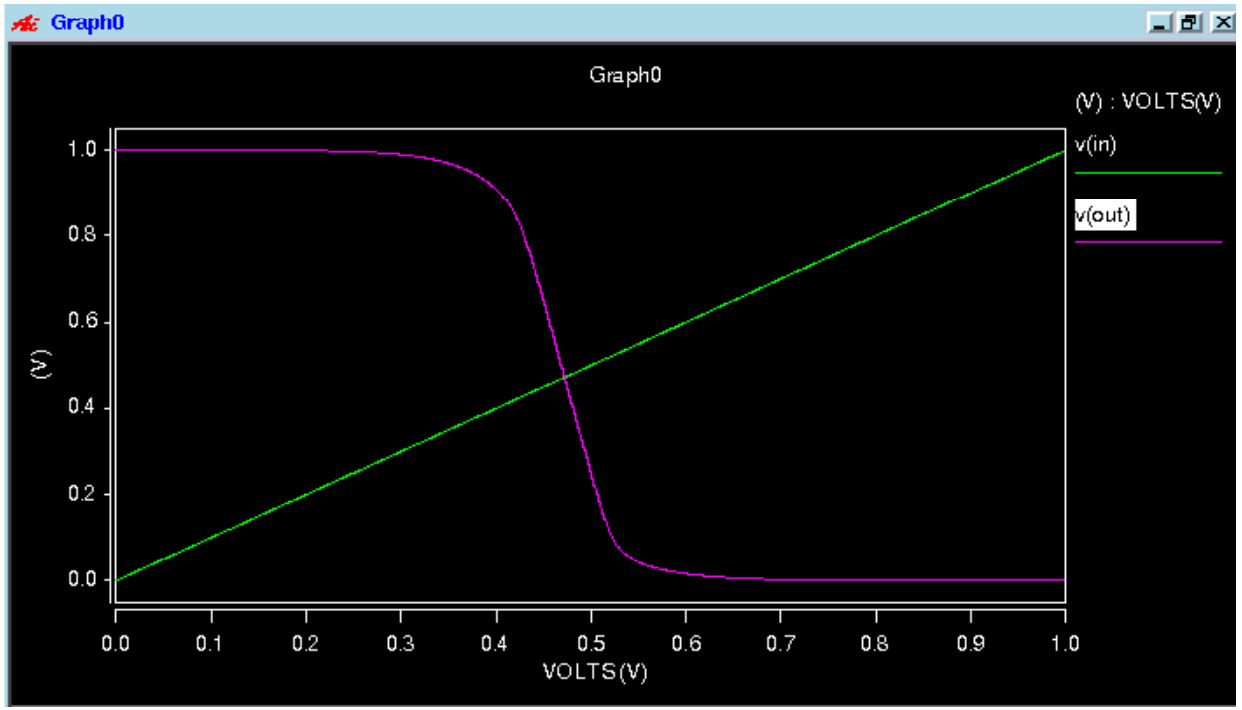
Hspice simulation

Example> Inverter 설계 및 simulation

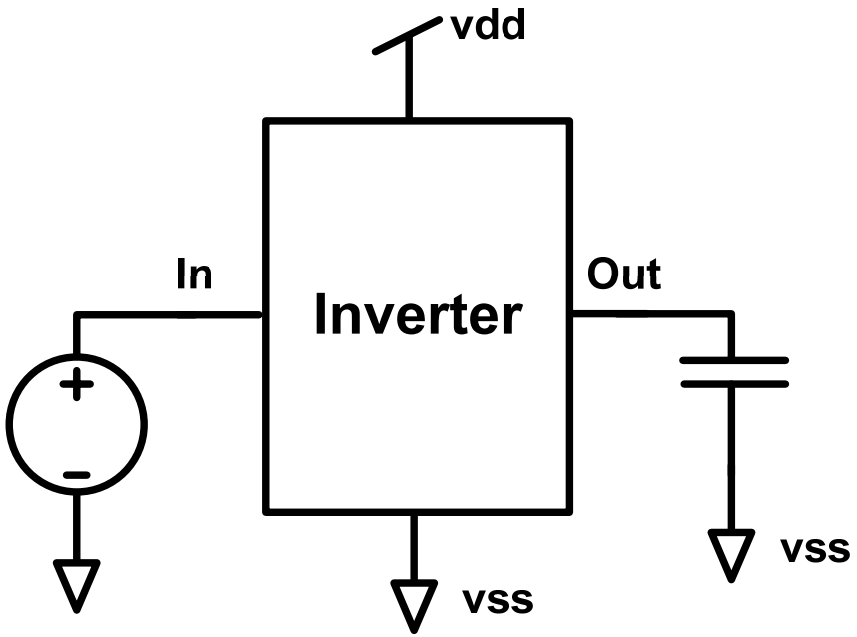




Hspice simulation

Example> Inverter 설계 및 simulation

AC simulation



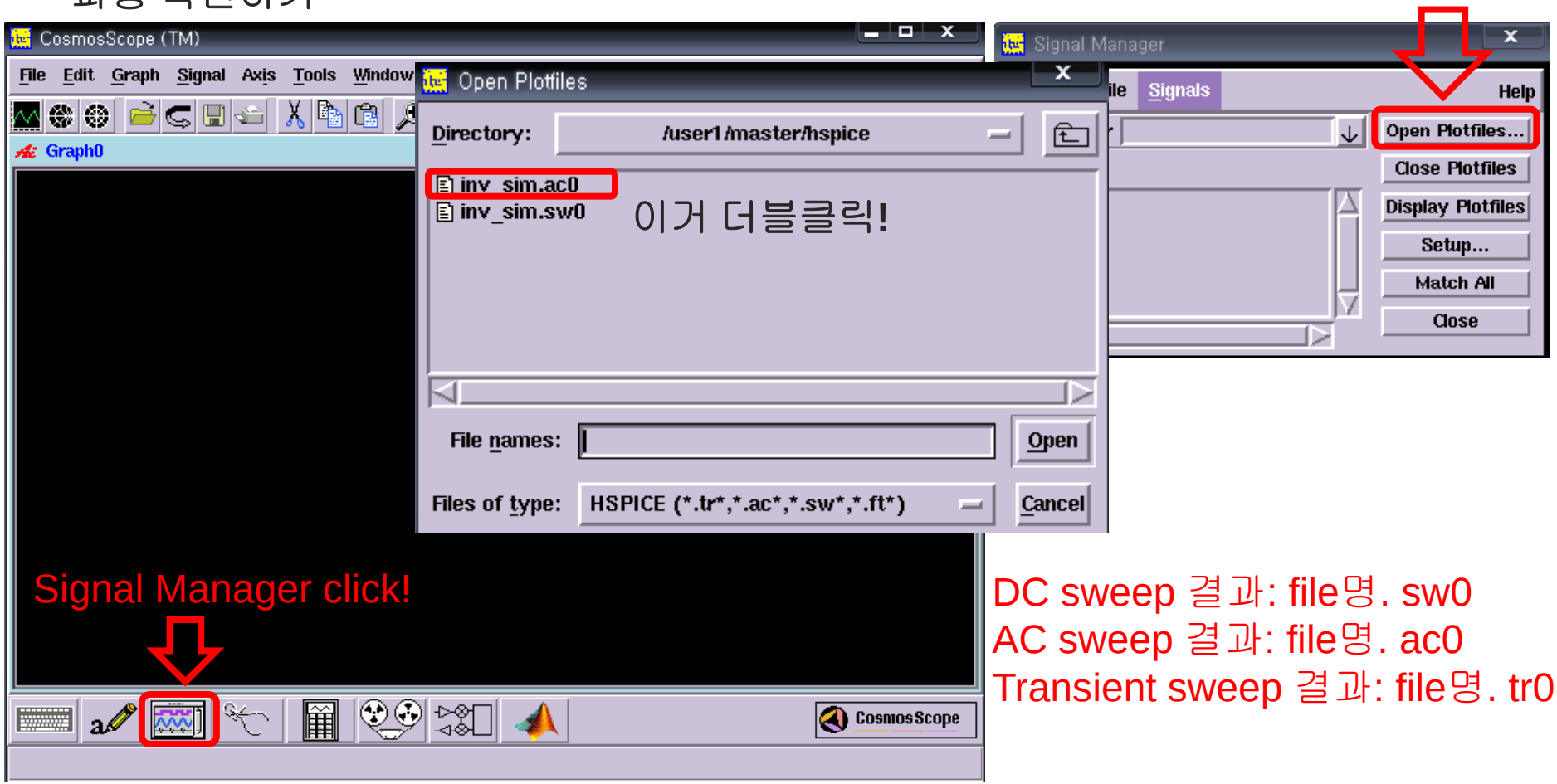

```
.include 'PMOS_VTL.inc'
.include 'NMOS_VTL.inc'
.include 'netlist.sp'

.OPTIONS POST NODE LIST

V1 vdd 0 1
V2 vss 0 0
Vin    in     vss    0.5      ac=1


x_inv  out    in     vdd    vss    Inverter
c_out  out    vss    1p

.ac    dec    1000     100k          10g
.END
```

Ac sweep 을 frequency 축을 decade 단위로 하여, 각 decade 마다 1000개의 data 를 찍고, 100KHZ 에서 부터 10GHz 까지의 주파수 응답을 simulation 해라

Hspice simulation

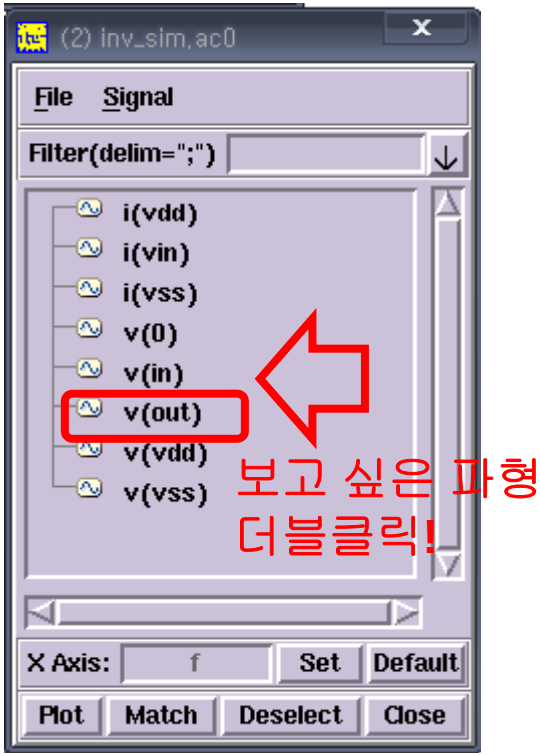
Example> Inverter 설계 및 simulation

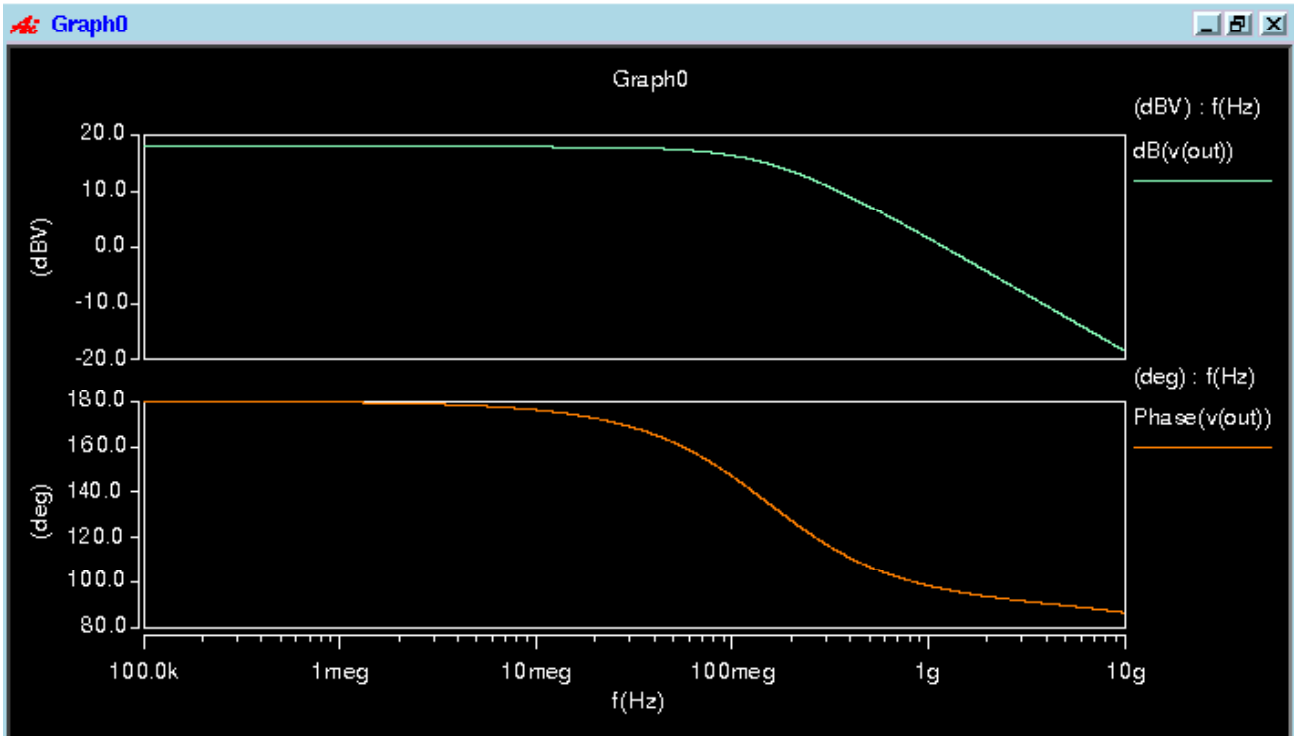
파형 확인하기



Hspice simulation

Example> Inverter 설계 및 simulation

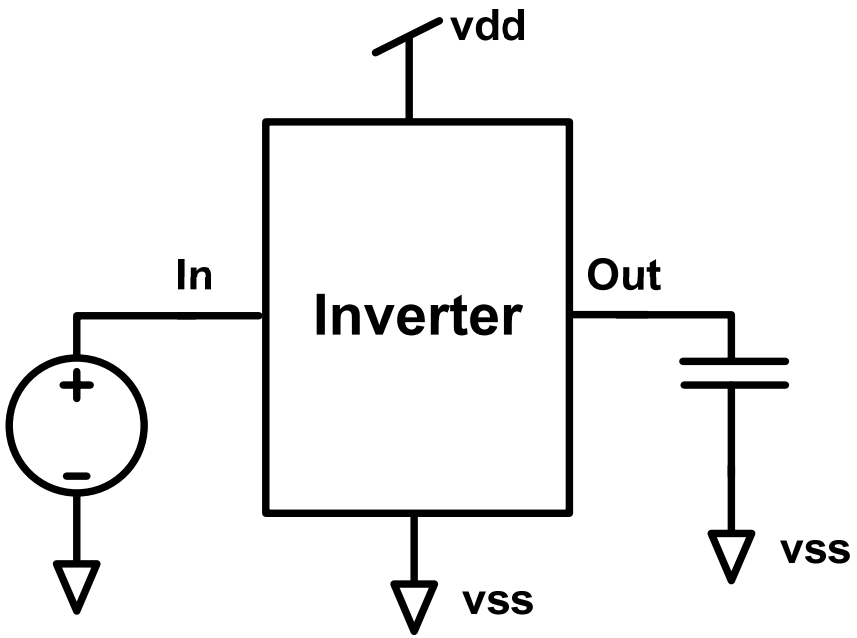




Hspice simulation

Example> Inverter 설계 및 simulation

transient simulation




```
.include ‘PMOS_VTL.inc'
.include 'NMOS_VTL.inc'
.include 'netlist.sp'

.OPTIONS POST NODE LIST

V1 vdd 0 1
V2 vss 0 0
Vin     in      vss     sin(0.5 0.5 100x)
0.5 V ± 0.5V 의 swing 을 가지는
100MHz 의 sin 파 신호 생성
x_inv   out     in      vdd     vss     Inverter
c_out   out     vss     1p

.tran       1p          100n
.END
```

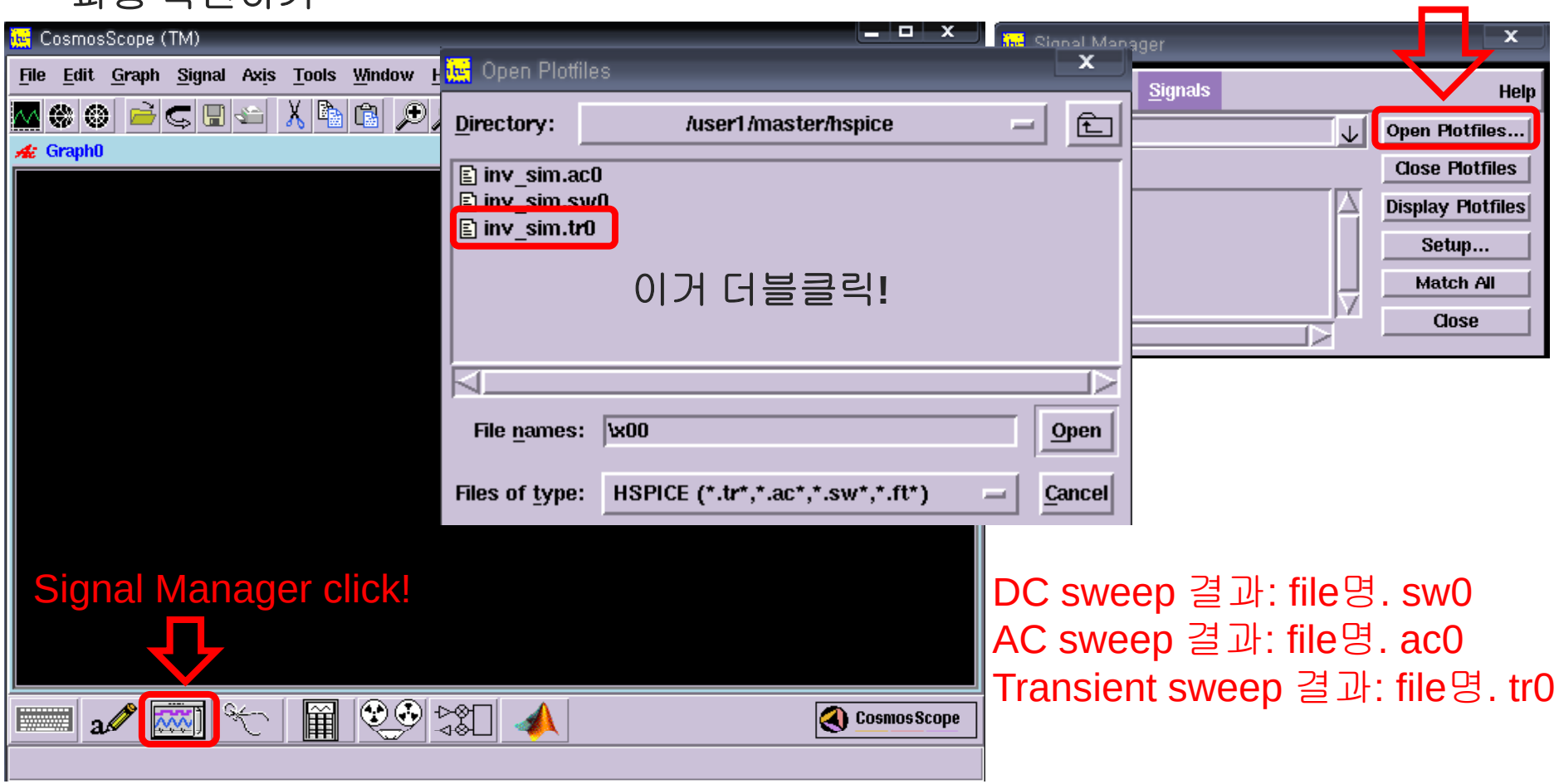
Transient sweep 을 1ps 마다 data 를 찍어서 100ns 까지 simulation 해라

Hspice simulation

Example> Inverter 설계 및 simulation

파형 확인하기

파형 열어보자!



DC sweep 결과: file명. sw0
AC sweep 결과: file명. ac0
Transient sweep 결과: file명. tr0

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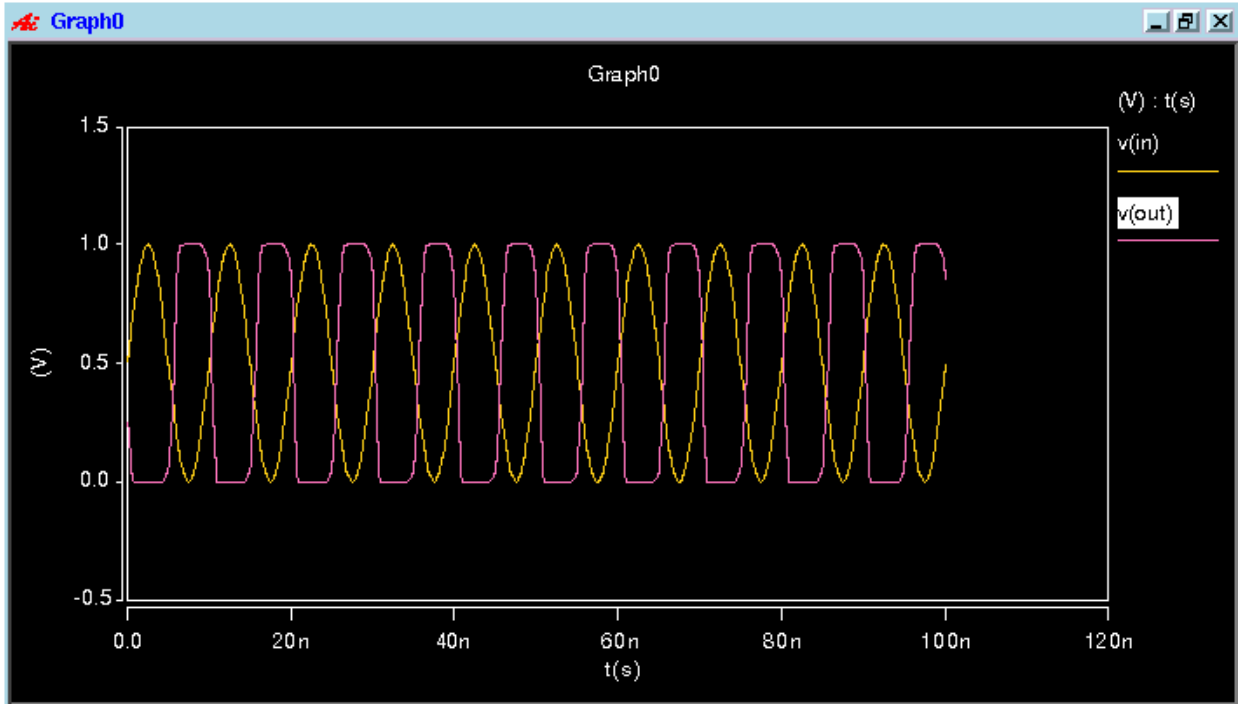
Hspice simulation

Example> Inverter 설계 및 simulation



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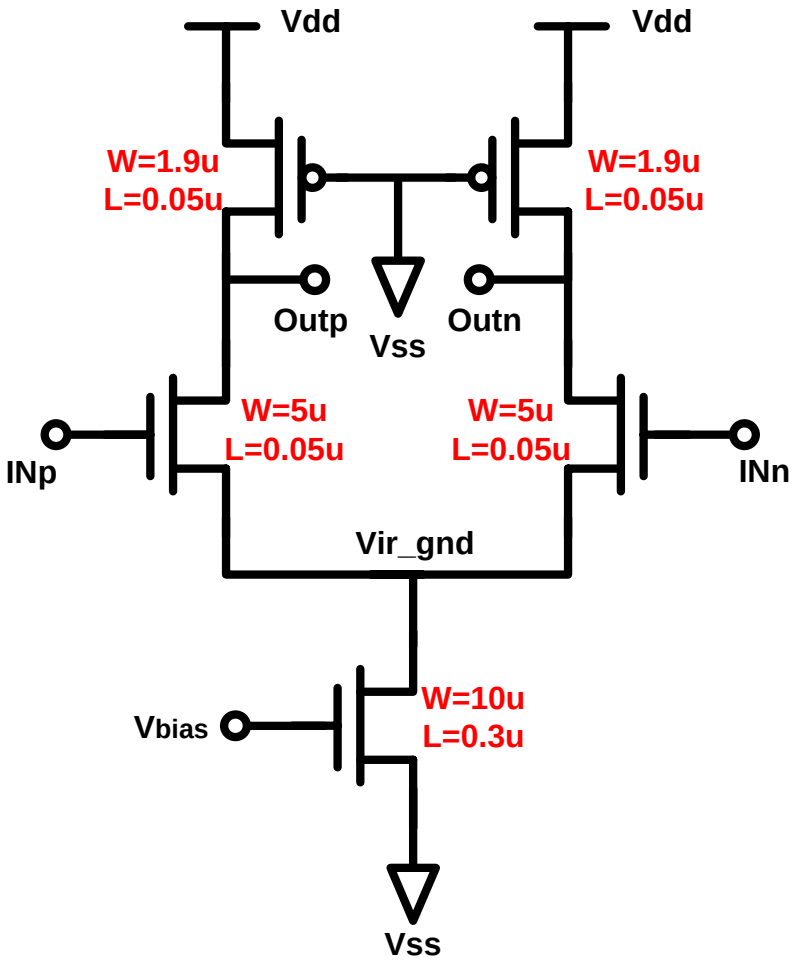
실습

차동 증폭기 (differential amplifier) 의 설계 및 시뮬레이션



DC, AC, Transient sweep 후 파형 확인

Differential input signal generator

```
vin in vss ac=1
Voff off vss 0.75
Einp inp off in vss 0.5
Einn inn off in vss -0.5

Vvbias   vbias    vss      0.7

.dc vin -0.5 0.5 0.001
.ac dec 1000 100k 10g
.tran 1p 100n
```

모든 NMOS 의 bulk 는 vss 로
모든 PMOS 의 bulk 는 vdd 로 연결!

Appendix

• **Parameter 설정 및 parameter sweep**

Hspice netlist 에서 parameter 설정은 다음과 같이 한다. 예를 들어 어떤 dc voltage 값을 cont 라는 parameter (변수) 값으로 지정하고 싶다면,

```
Vcont    cont    vss    'cont'
```

와 같이 ' ' 안에 변수 값을 써 주면 된다. 그리고

```
.param   cont=0.6
```

과 같이 선언해주면 cont 에는 0.6 이란 값이 들어가게 된다.

Cont 값을 바꿔가며 parameteric sweep 을 하려면,

```
.dc      vx      0      1      0.001    sweep   cont    0       1       0.1
```

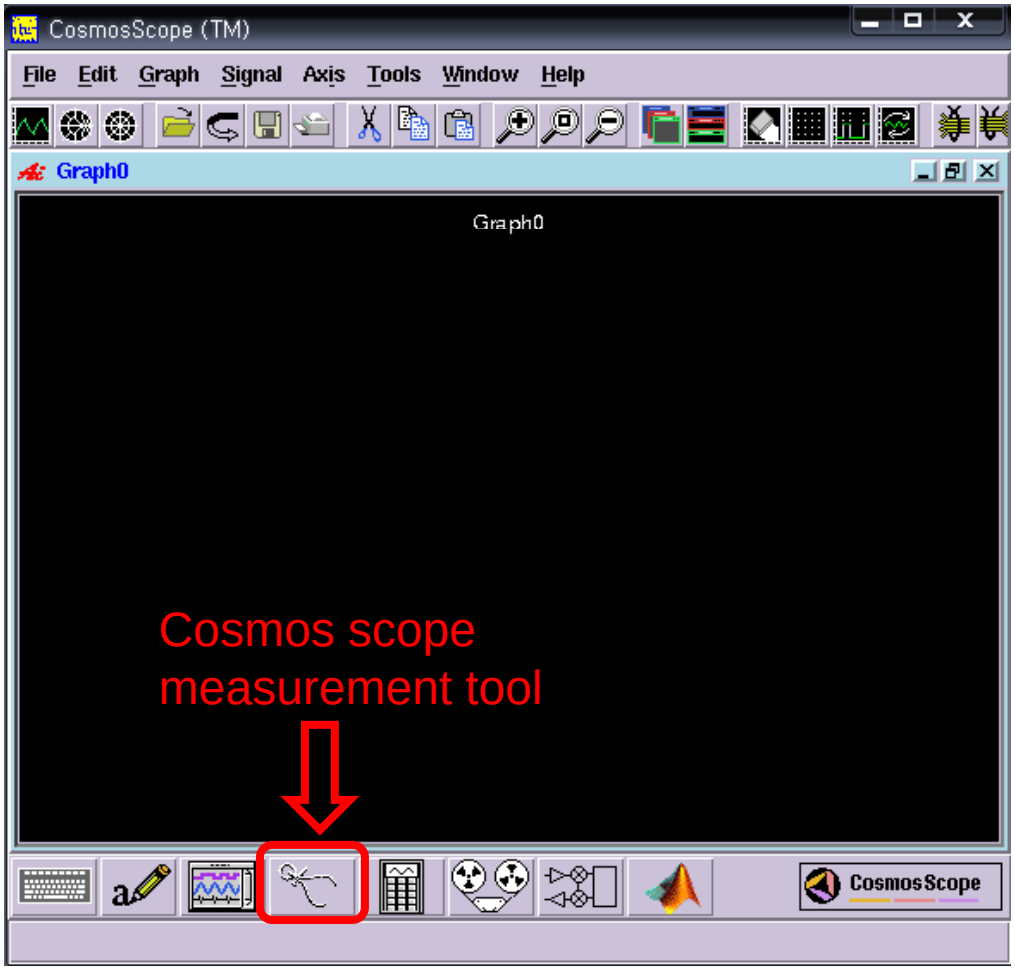
과 같이 설정해준다. 이렇게 해 주면, cont 값을 0 에서 1 까지 0.1 씩 변화시키며 10번 반복하여 dc sweep 을 하게 된다.

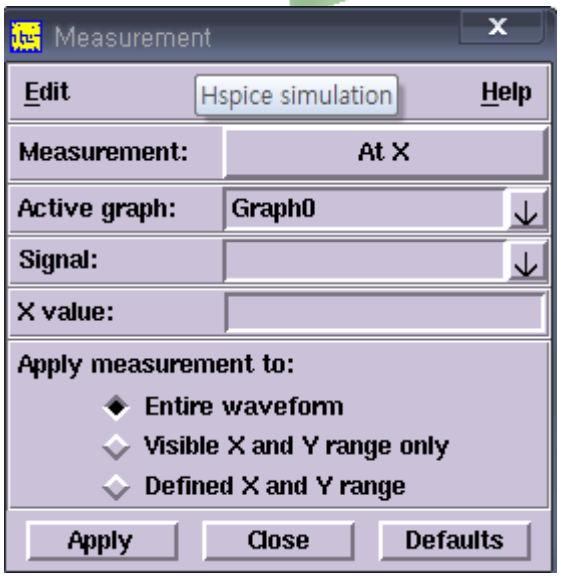
이는 ac sweep, transient sweep 에서도 마찬가지로 적용할 수 있다.

```
.ac      dec     1000   100k    10g      sweep   cont    0       1       0.1
.tran    1p      100n   sweep   cont     0       1       0.1
```

Appendix

- **Cosmos scope measurement tool**





Measurement tool 을 잘 사용하면 파형에 대한 거의 모든 정보를 얻을 수 있다. 예를 들어 파형의 주파수 혹은 swing 폭, rising time, falling time 등을 알고 싶을 땐, 직접 재려고 하지말고 measurement tool 을 이용하라