High Frequency Devices and Circuits

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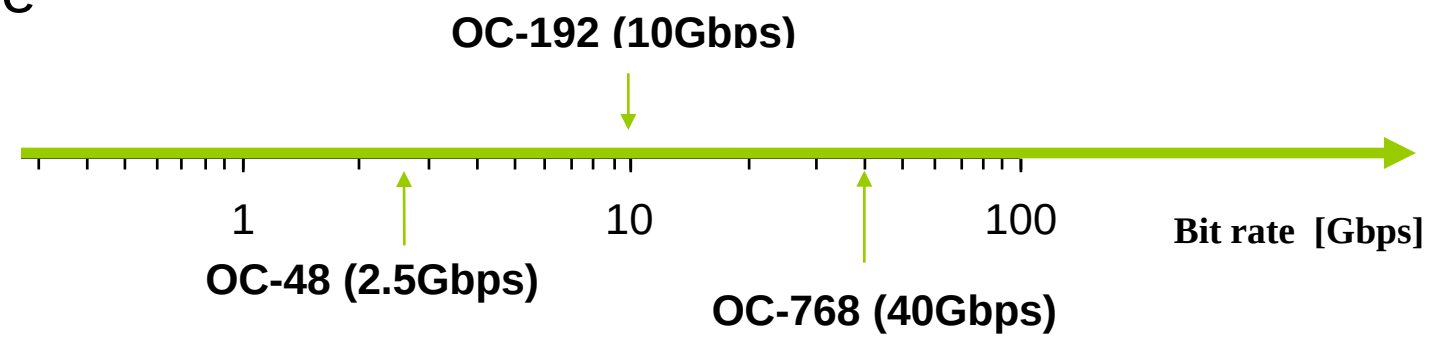
Outline

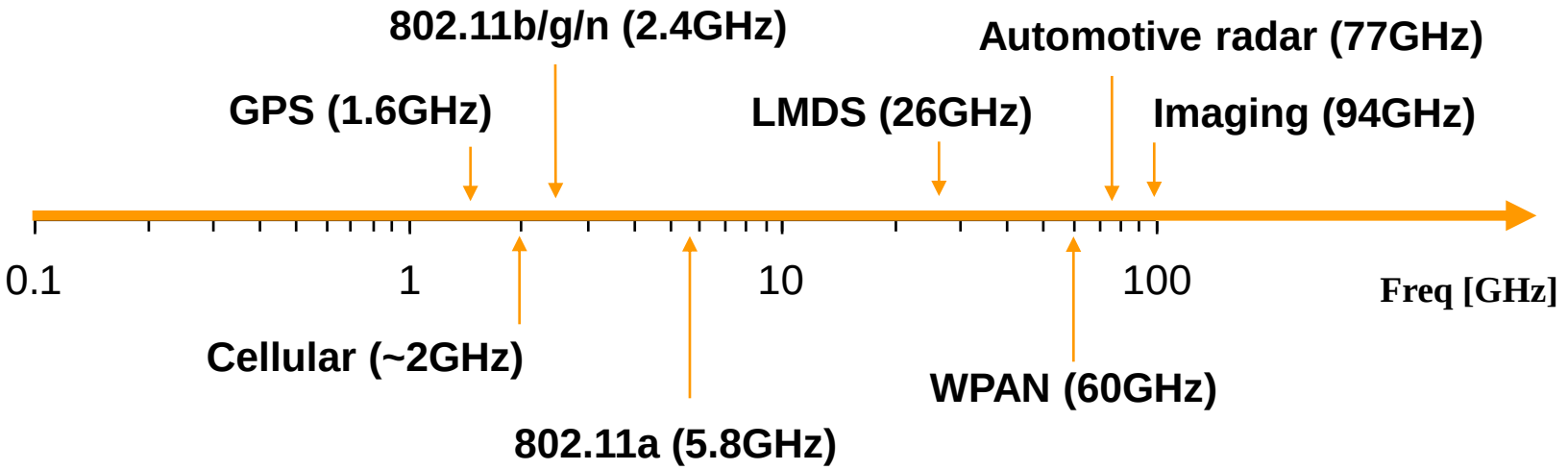
- High Frequency Applications
- High Frequency Semiconductor Devices
- High Frequency Semiconductor Circuits

Various Application of RF and mm-wave

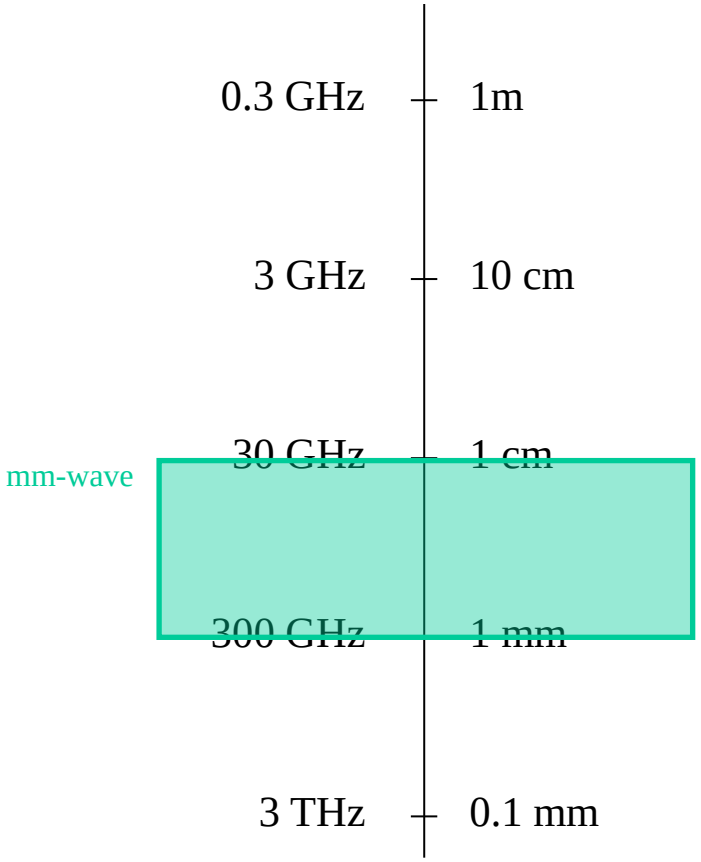
Wireline



Wireless



Definition of mm-wave



L band	**1 – 2 GHz**
S band	**2 – 4 GHz**
C band	**4 – 8 GHz**
X band	**8 – 12 GHz**
Ku band	**12 – 18 GHz**
K band	**18 – 26 GHz**
Ka band	**26 – 40 GHz**
Q band	**30 – 50 GHz**
U band	**40 – 60 GHz**
V band	**50 – 75 GHz**
E band	**60 – 90 GHz**
W band	**75 – 110 GHz**
F band	**90 – 140 GHz**
D band	**110 – 170 GHz**
G band	**140 – 220 GHz**
H band	**220 – 325 GHz**

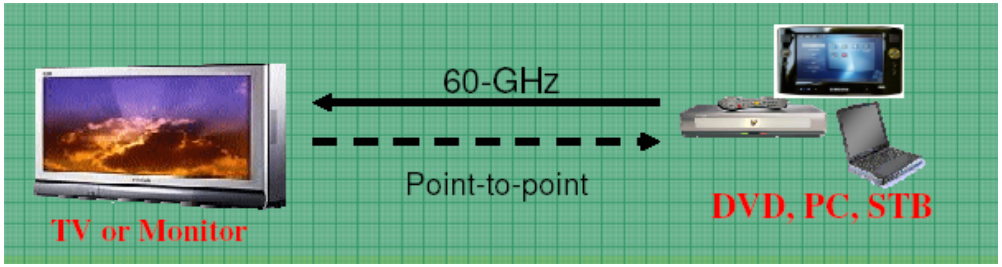
mm-wave

$1\ \text{mm} \leq \lambda < 1\ \text{cm}$

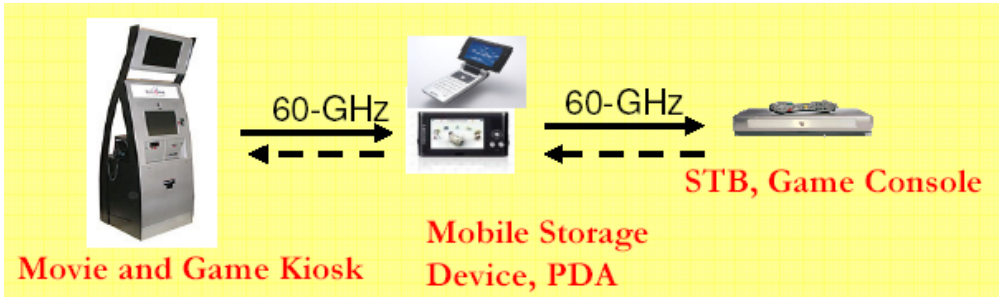
$30\ \text{GHz} < f \leq 300\ \text{GHz}$

60 GHz Applications

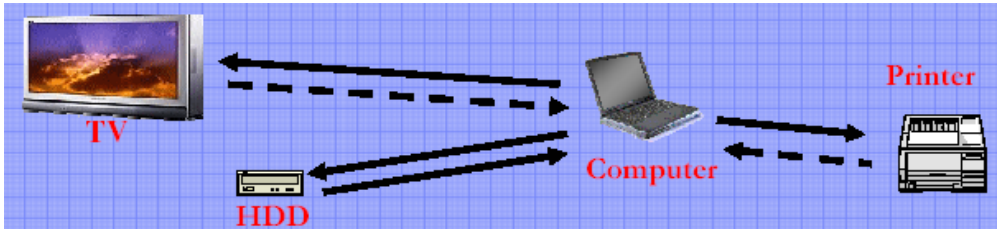
- WPAN (Wireless Personal Area Network)
  - Gigabit rate wireless communication



Streaming HD Video
(Uncompressed)
1080i > 1.5 Gb/s
1080p > 3 Gb/s



"Point-and-shoot" file transfer
1-3 Gb/s burst data
1-3 m range

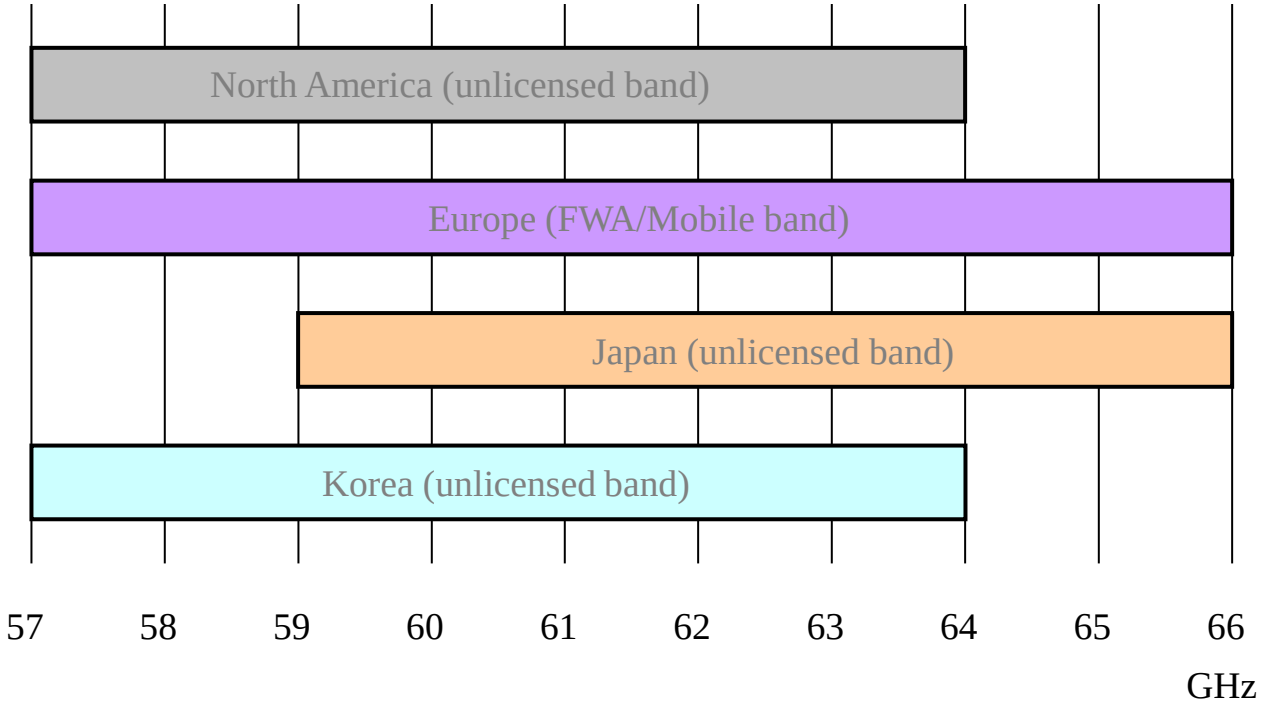


Personal Area Network
Streaming video + file transfer

B. Floyd IMS-WS 2007

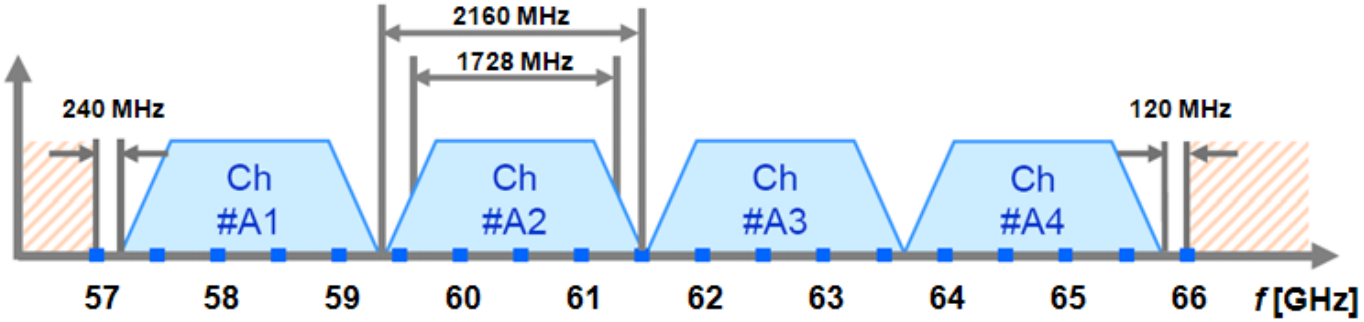
Available Frequency Bands

- Available frequency band for WPAN in various regions

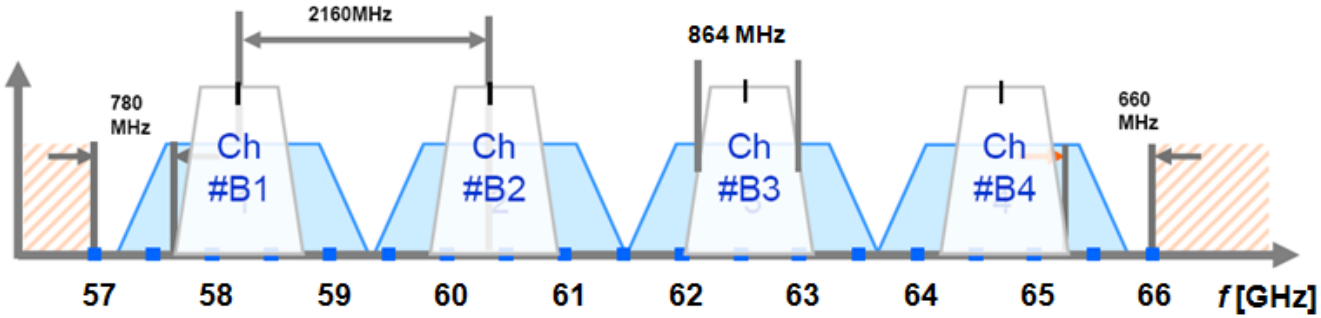


Channel Plan

- IEEE 802.15.3c standard channel plan
  - Full rate (2 GHz)

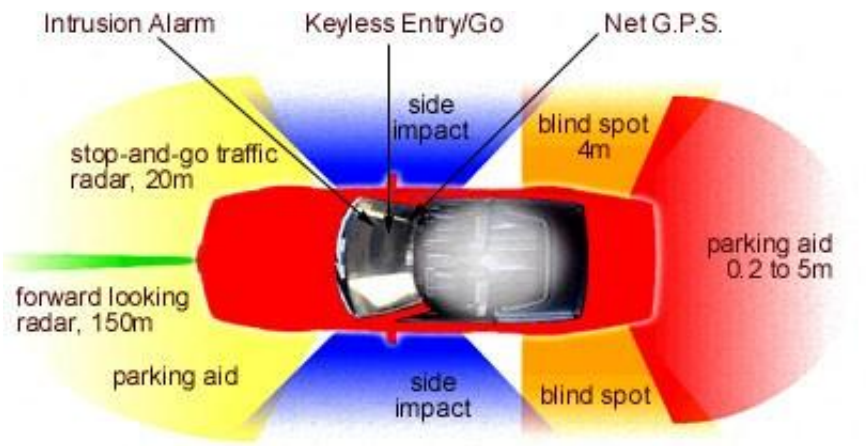


  - Half rate (1 GHz)



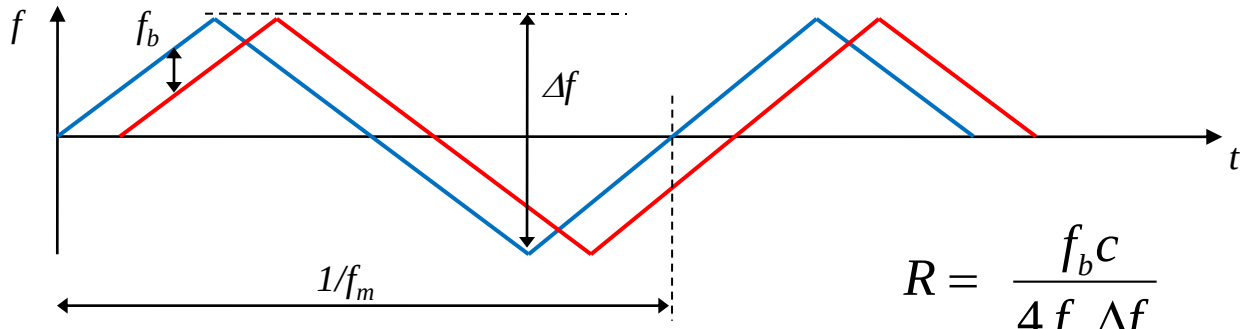
77 GHz Applications

- Automotive radar
  - Long range radar (LRR)
    - For ACC (Adaptive Cruise Control)
    - Operating at 77 GHz
  - Short range radar (SRR)
    - For collision warning, stop-and-go function, parking aid, blind spot monitoring, lane change assistance, rear crash collision warning
    - Currently dominated by 24 GHz operation
    - Planned to shift to 79 GHz (mandatory from July 2013 in EU)
  - A typical radar system is composed of 1 LRR and several SRR's



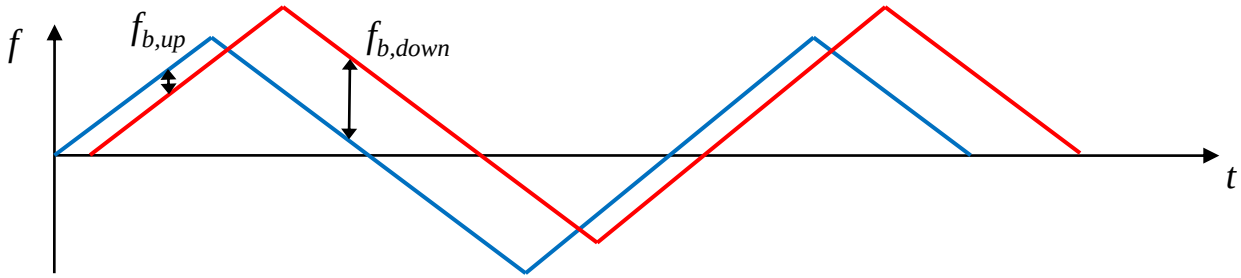
Principles of FMCW

When the object is stationary (relative speed zero)



$$R = \frac{f_b c}{4 f_m \Delta f}$$

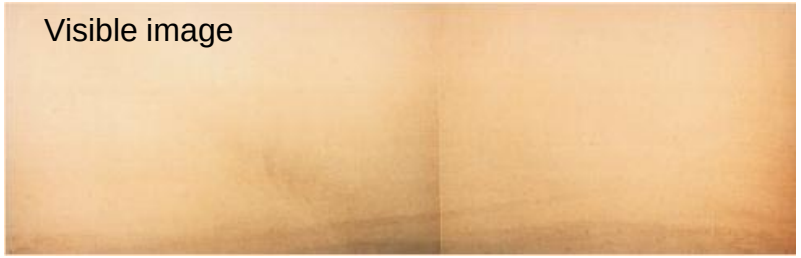
When the object is moving (relative speed non-zero)

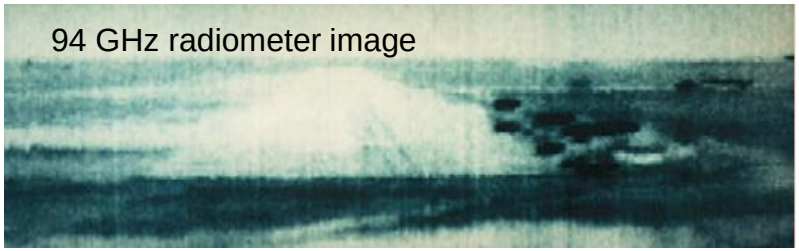


$$R = \frac{\left(f_{b,down} + f_{b,up} \right)}{2} \cdot \frac{c}{4 f_m \Delta f}, \qquad v = \frac{\left(f_{b,down} - f_{b,up} \right)}{\left(f_{b,down} + f_{b,up} \right)} \cdot c$$

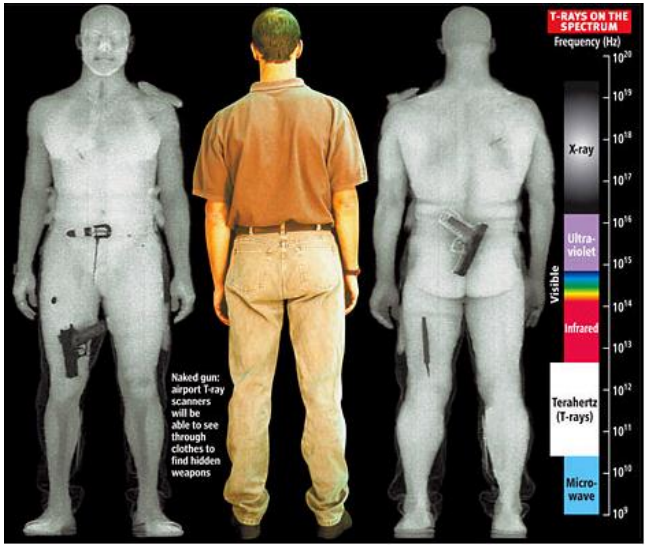
94 GHz Applications

- Imaging system at 94 GHz
  - Anti-terrorist security systems
  - Aviation safety systems
  - Atmospheric sensing systems



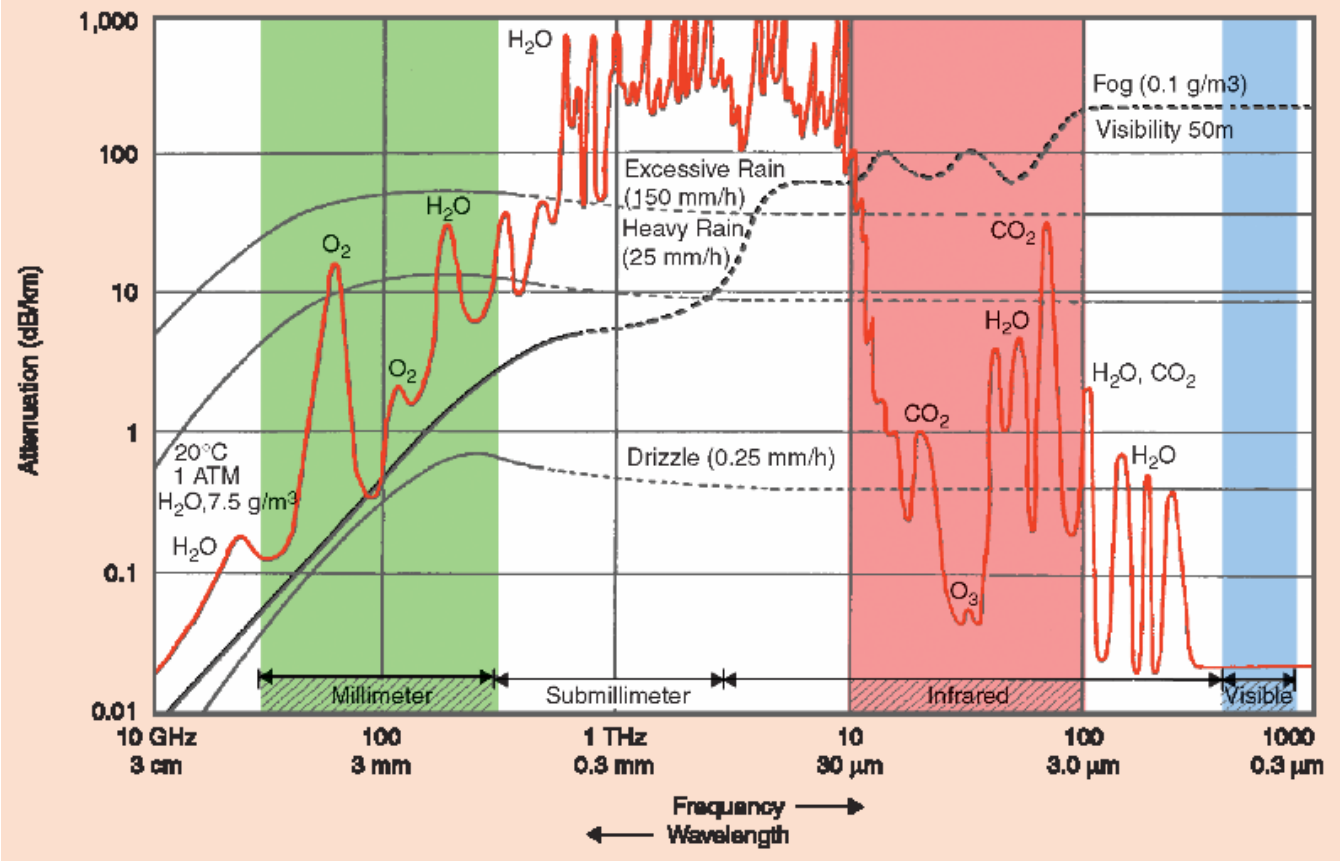


Runway image at foggy weather



Security imaging system

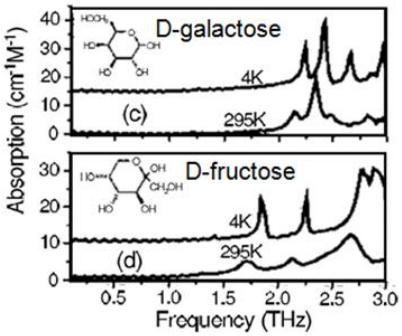
mm-wave Propagation in Atmosphere



L. Yujili et al, Microwave Magazine, 2003

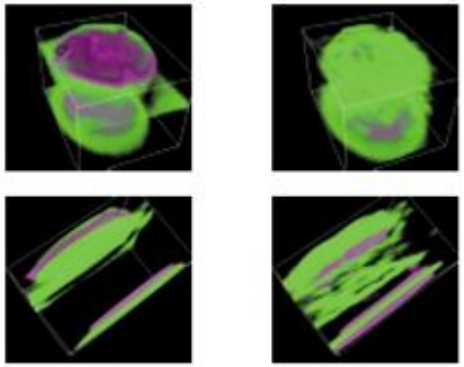
Applications beyond 100 GHz

Spectroscopy

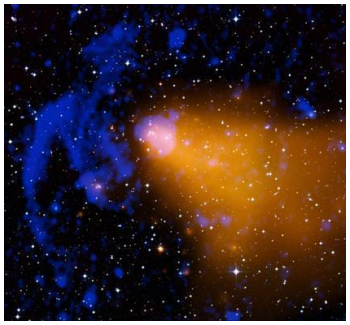


Sakai et al, 2005

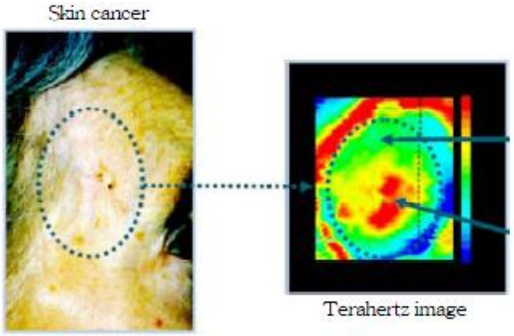
Imaging



Atmospheric/Space



Bio/Medical



Paek et al 2007

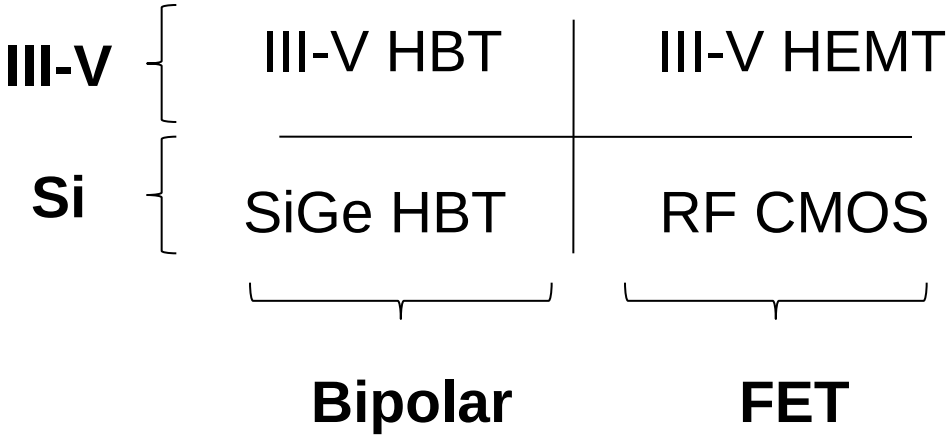
Broadband Communication

Outline

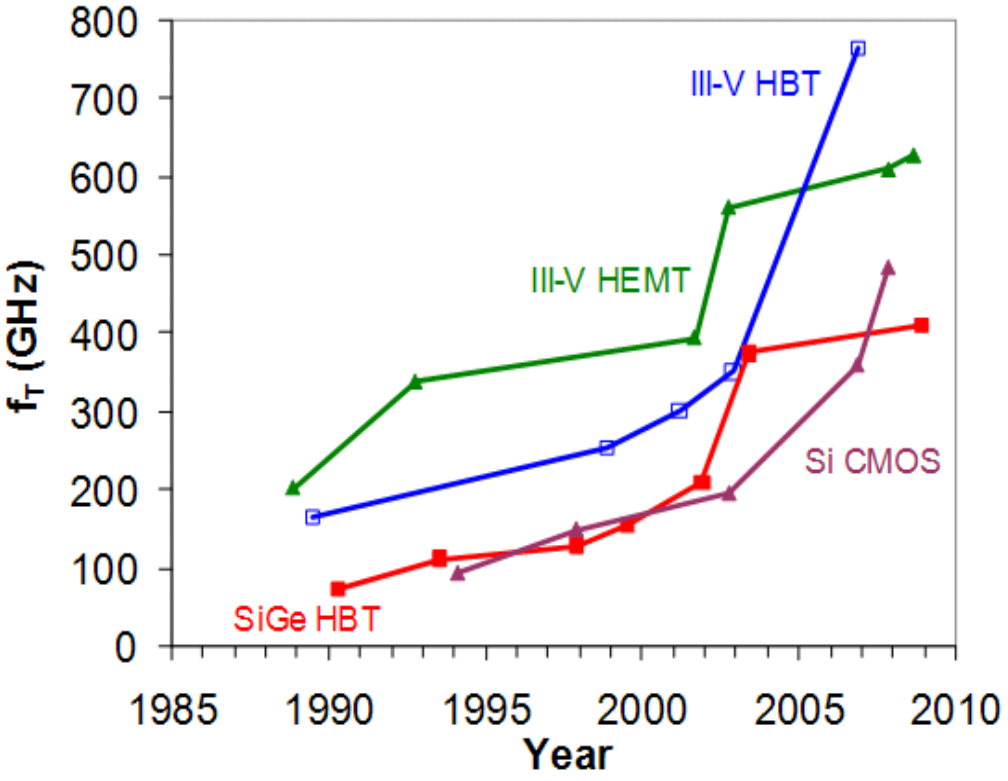
- High Frequency Applications
- **High Frequency Semiconductor Devices**
- High Frequency Semiconductor Circuits

High Frequency Semiconductor Devices

- III-V devices (GaAs or InP based)
  - HBT (heterojunction bipolar transistor)
  - HEMT (high electron mobility transistor)
- Si-based devices
  - SiGe HBT
  - RFCMOS



Device Operation Speed Trend



Device Comparison: III-V vs Si (I)

- Advantage of III-V
  - Superior electron transport characteristic
    - High low field mobility for relaxed dimension
    - High ballistic velocity for aggressively scaled dimension

      → High operation frequency

      → High gain and low noise for a given operation frequency
  - High substrate resistance
    - Resistivity 10^7 – 10^9 ohm-cm (compared with ~10 ohm-cm for Si)

      → Low loss for transmission lines, high-Q for inductors
  - High breakdown voltage
    - Breakdown voltage increases with wider bandgap E_g
    - Si: 1.12 eV, GaAs: 1.42 eV, InP: 1.27 eV, GaN: 3.44 eV

      → High power performance

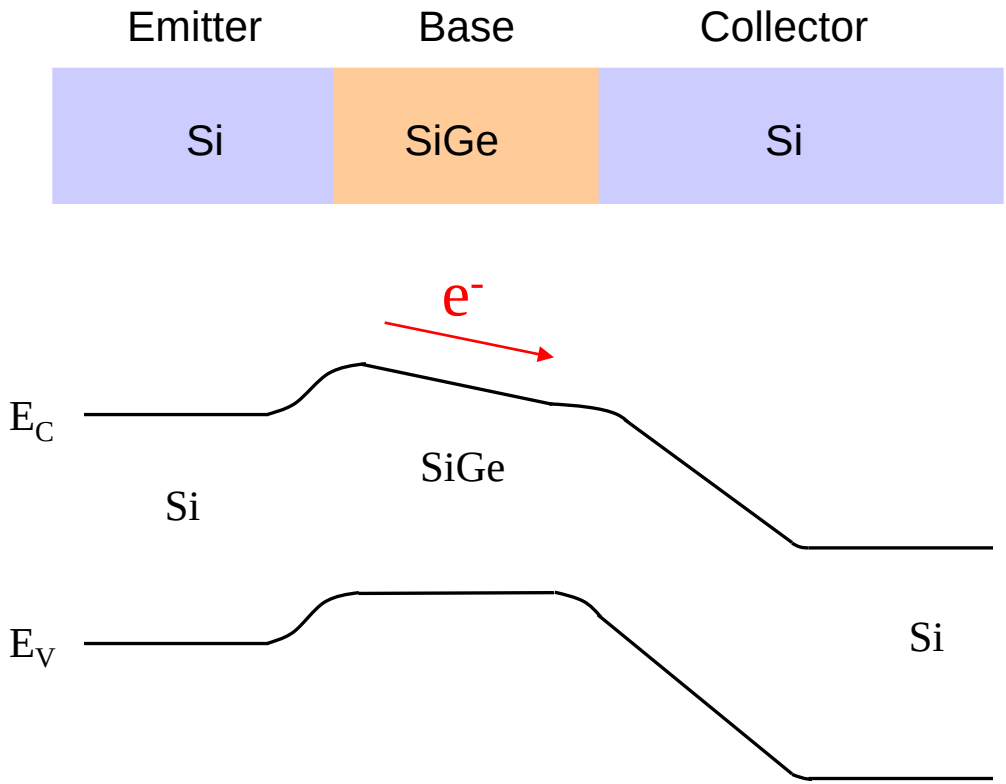
Device Comparison: III-V vs Si (II)

- Advantage of Si
  - Compatibility with baseband circuits (digital circuits)
  - Based on highly developed fabrication infrastructure
  - Higher reliability
    - Excellent interface/surface properties, low defect density, and low thermal resistivity
  - Lower cost
    - Larger wafer dimension, lower wafer cost
    - No need for costly epitaxial processes, e-beam litho
    - But, expensive mask sets leads to high cost for low volume

SiGe HBT vs Si CMOS

- Advantage of SiGe HBT
  - Higher device operation frequency of commercially available devices
  - Higher transconductance g_m
  - Superior low frequency noise (1/f noise)
  - Vertical path of current inside the device
    - → Smaller lateral dimension fluctuation
    - → Smaller device performance variation
  - No need for the expensive phase shift mask for acceptable operation frequency
- Advantage of Si CMOS
  - Fully compatible with baseband circuits (digital circuits)
    - → High level integration such SoC very feasible
    - → Device model can be obtained by a simple modification of digital CMOS model
  - Less complex fabrication process
  - Low cost for high volume (such that the cost of phase shift mask becomes less significant)

Properties of SiGe HBTs



Quasi E-field in the base (30~50 kV/cm)

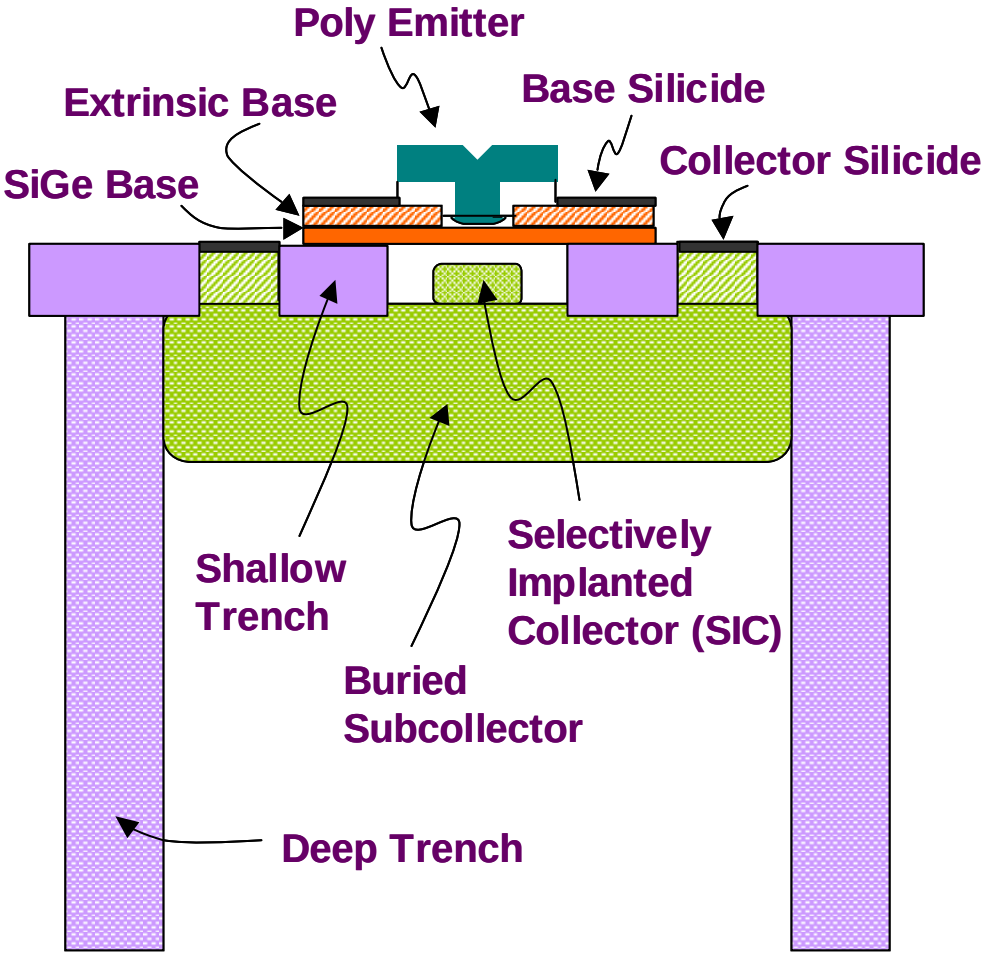
- Base transit time reduction → speed enhancement

Increased n_i in the base

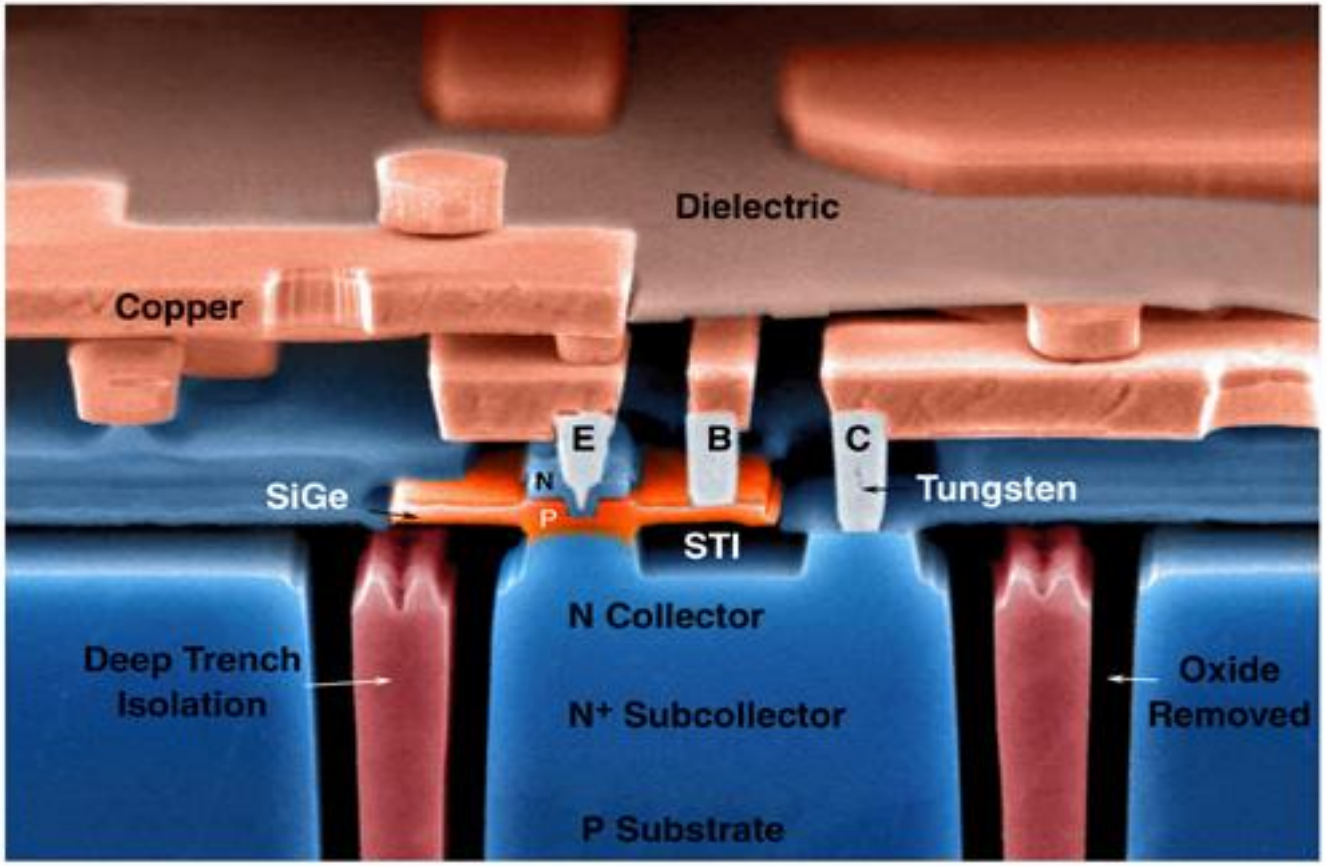
- Increased Ic → current gain enhancement

→ allow high base doping → low R_B/ low NF_{min} or W_B reduction

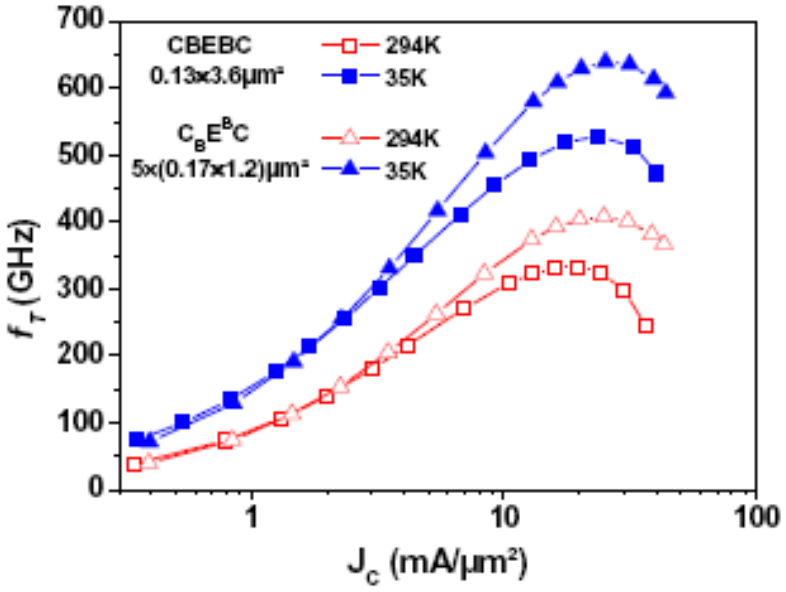
SiGe HBT Structure Schematic

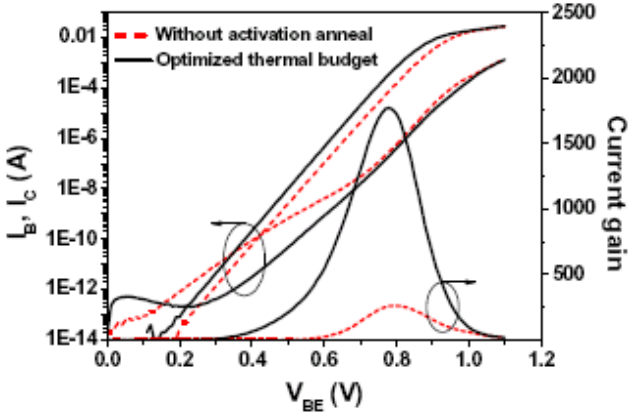


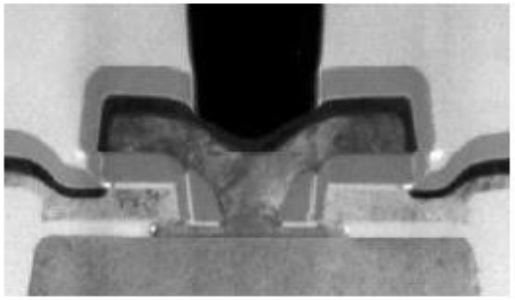
SEM Image of Fabricated SiGe HBT



SiGe HBT Record Performance



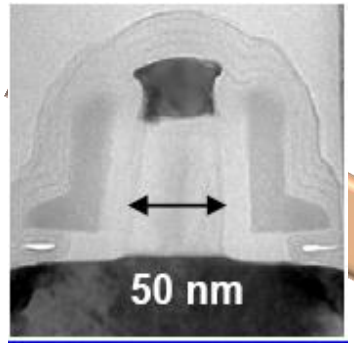




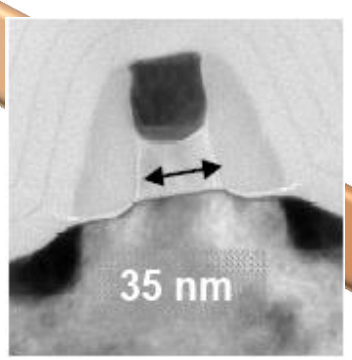
- ST Microelectronics
- 0.13 um SiGe HBT
- C_BE^BC layout: Peak f_T / f_{max} = 410/150 GHz
- CBEBC layout: Peak f_T / f_{max} = 340/260 GHz

Geynet et al BCTM 2008

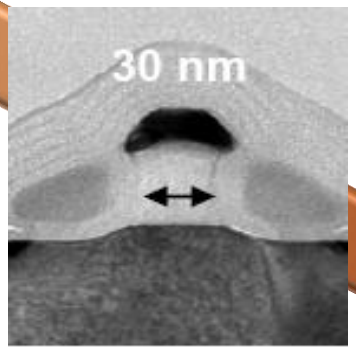
MOSFET scaling down (Intel)



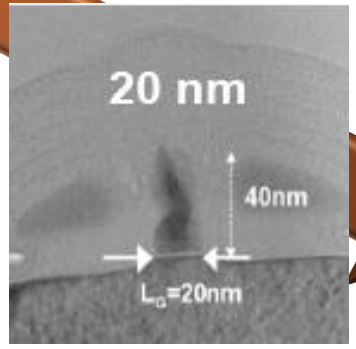
90 nm (2003)



65 nm (2005)

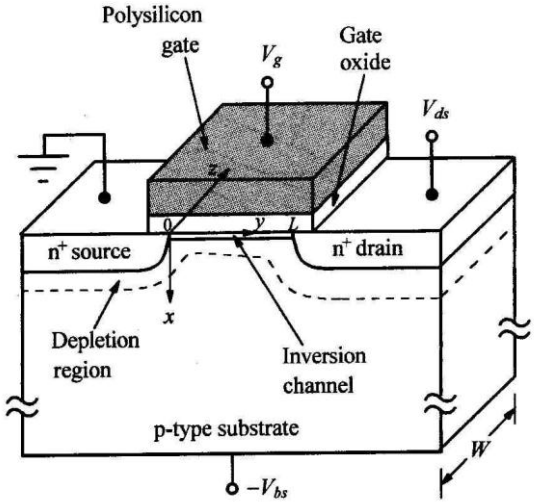


45 nm (2007)



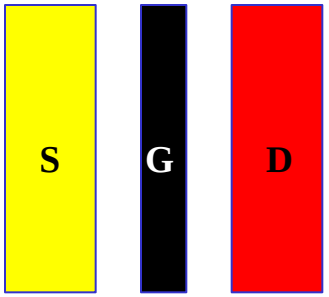
32 nm (2009)

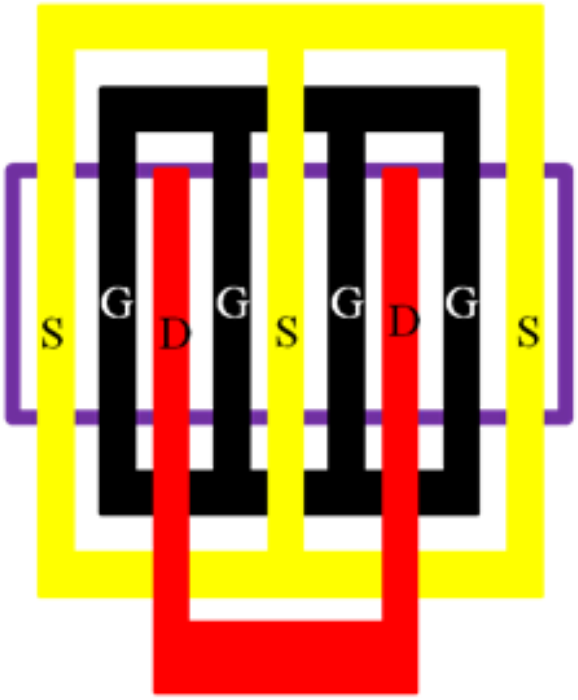
Technology Generation



- Performance Improvement
- Cost Down

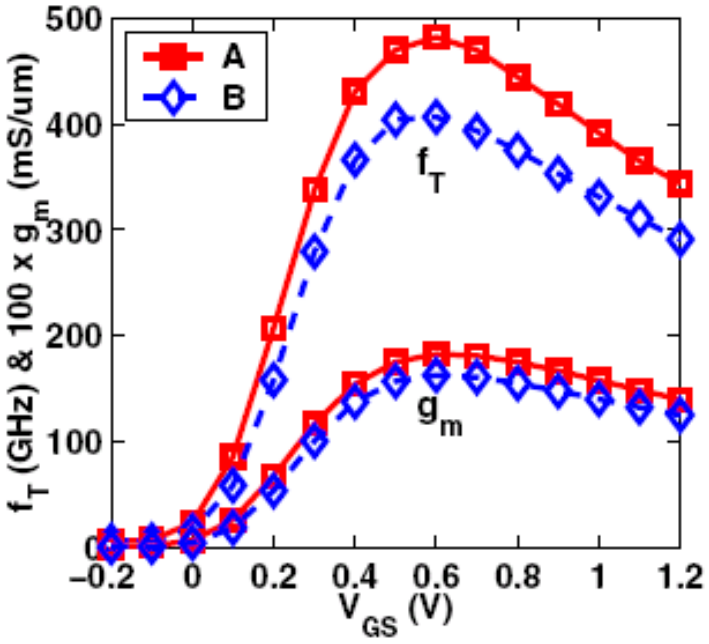
Layout of RF MOSFET

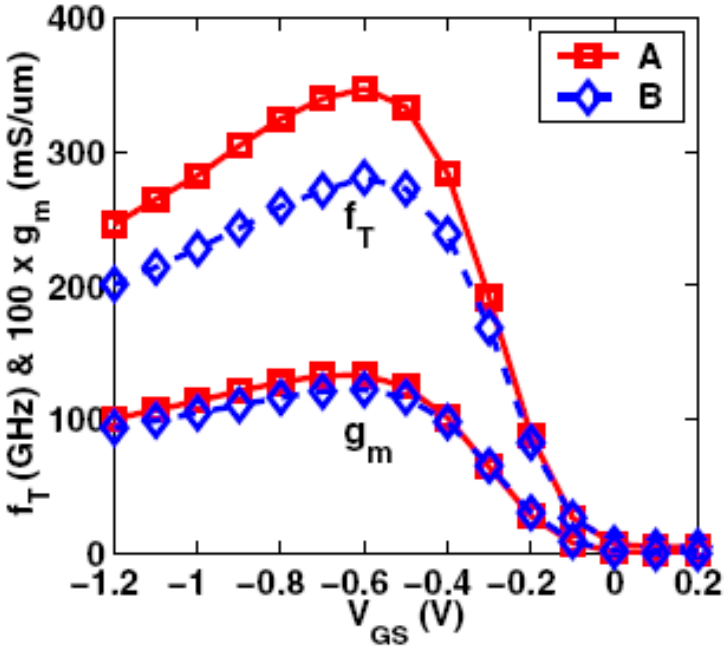




- Digital MOSFET
- RF MOSFET

RFCMOS Record Performance





- NFET: 45 nm SOI (L_{poly}=29 nm)
- Peak f_T = 485 GHz

- PFET: 45 nm SOI (L_{poly}=31 nm)
- Peak f_T = 345 GHz

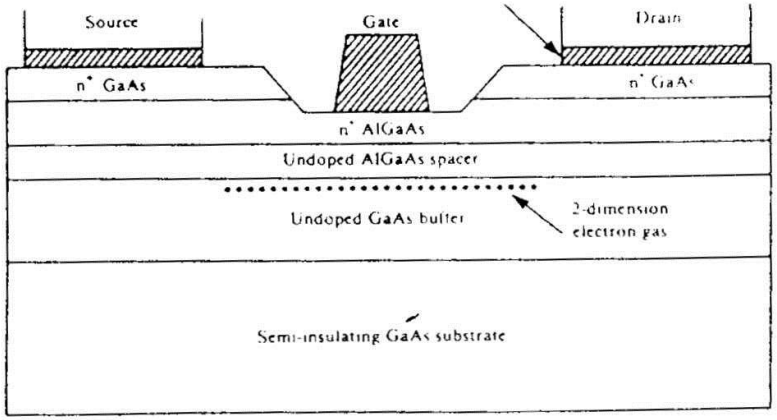
A: Relaxed poly pitch, B: Minimum poly pitch

Lee et al IEDM 2007

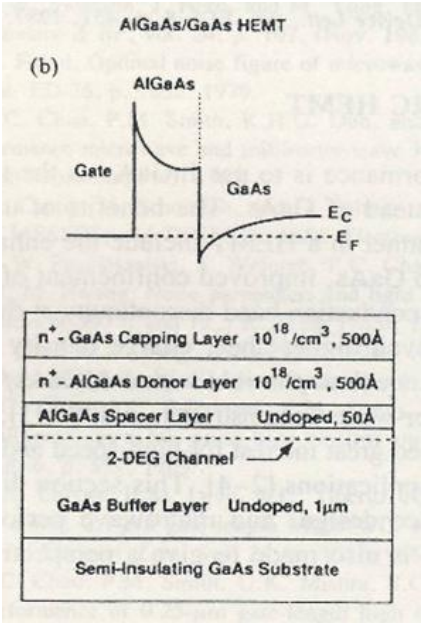
III-V HEMT Overview

- Employs modulation-doped structure
  - Channel is undoped and the carriers are provided from the barrier layer
  - Coulomb scattering is greatly reduced and the mobility if increased

  → 'high electron mobility' is achieved → 'HEMT'



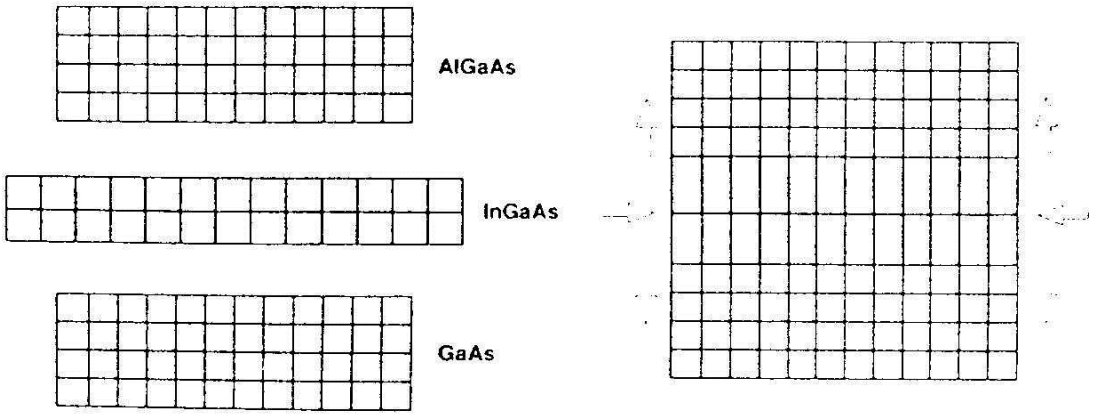
Structure of typical III-V HEMT

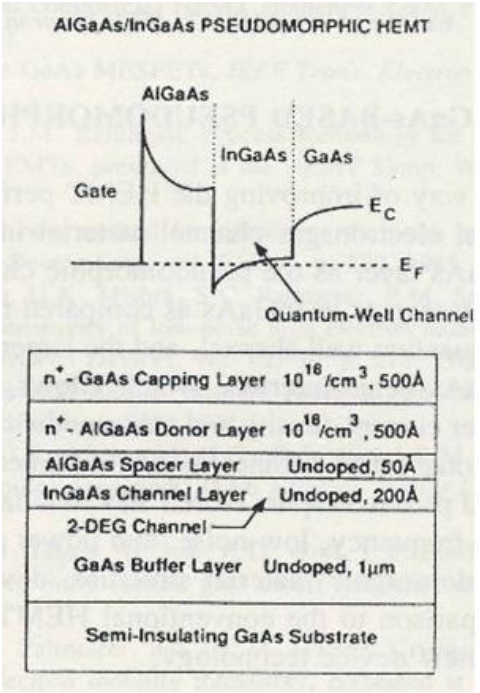


Band diagram of typical III-V HEMT

Pseudomorphic HEMT (PHEMT)

- Lattice mismatched strained pseudomorphic channel layer
  - Channel with smaller bandgap possible
  - → Improved carrier confinement and improved carrier transport

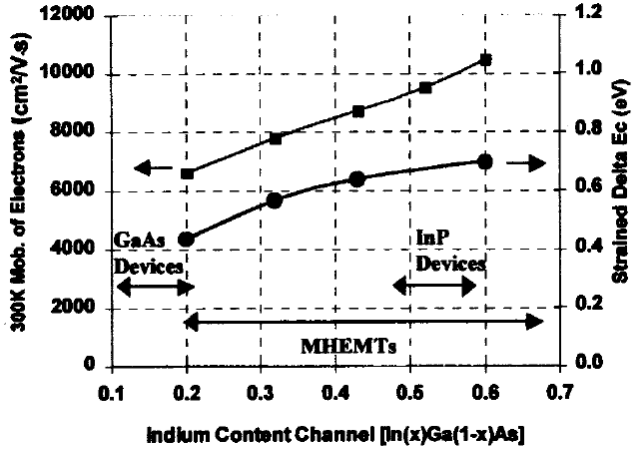




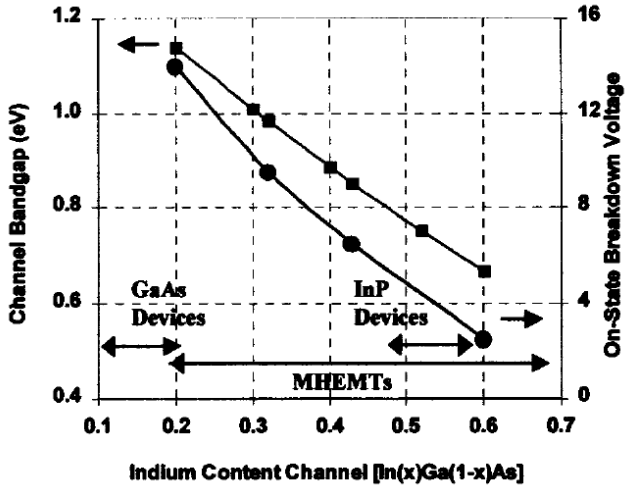
Metamorphic HEMT (MHEMT)

- Strain relaxed metamorphic buffer on GaAs
  - Layers with wide range of lattice constant can be grown on low cost GaAs substrate

  → High performance HEMT based on GaAs wafer possible

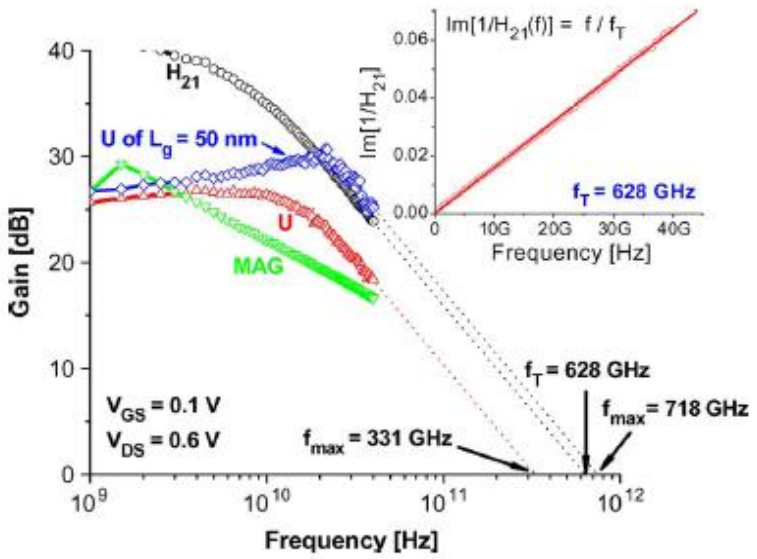


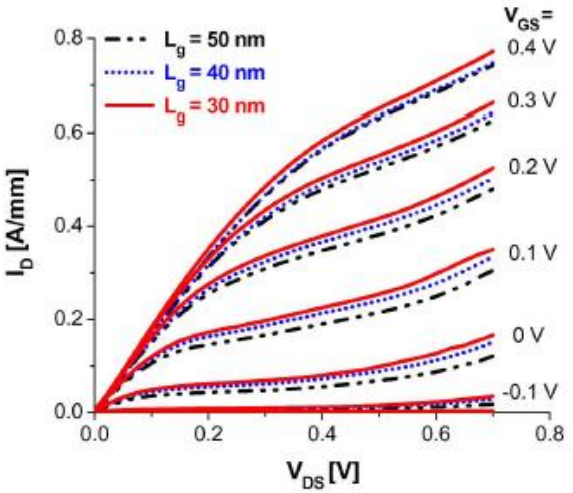
Cap layer
InGaAlAs Barrier
InGaAs channel (high In %, lattice matched to InP)
Graded InGaAlAs Buffer (Lattice mathing from GaAs to InP)
GaAs Substrate

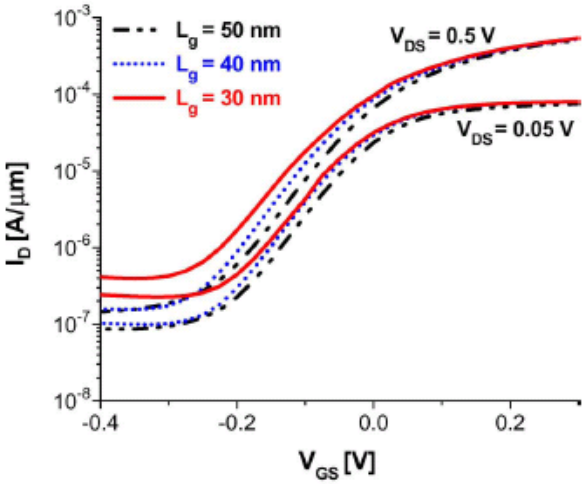


Whelan et al, 2000 IPRM

III-V HEMT Record Performance





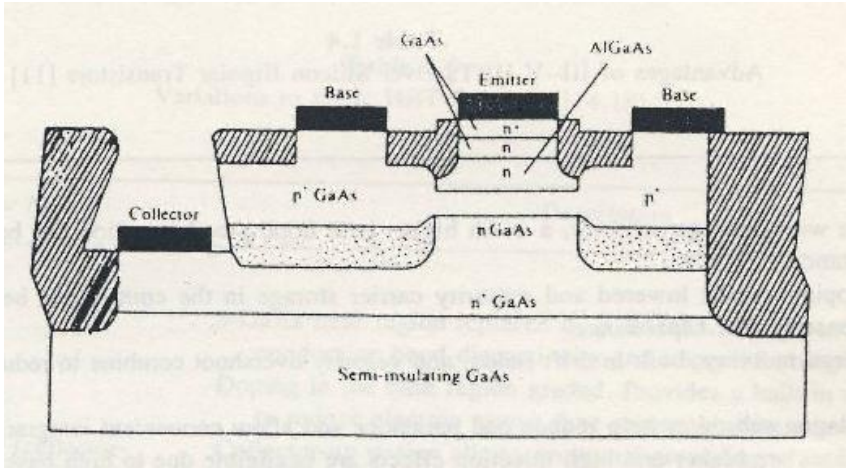


- MIT
- 30 - 50 nm gate length InP HEMT
- L_g = 30 nm: Peak f_T / f_{max} = 628/331 GHz
- L_g = 50 nm: Peak f_T / f_{max} = 557/718 GHz

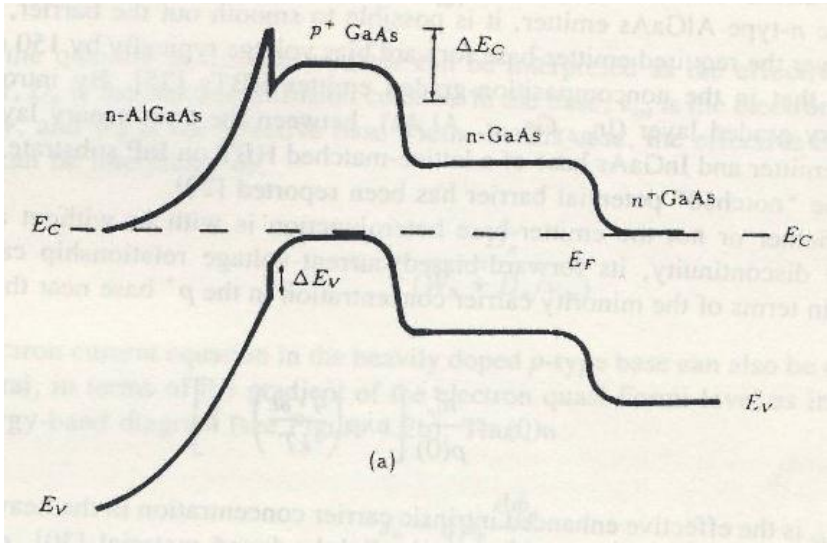
Kim et al EDL 2008

III-V HBT Overview

- Employs emitter with larger bandgap than base bandgap
  - Base doping can be increased
  - Bases resistance reduced → f_{max} and F_{min} improved
  - Thin gate can be employed → base transit time reduced

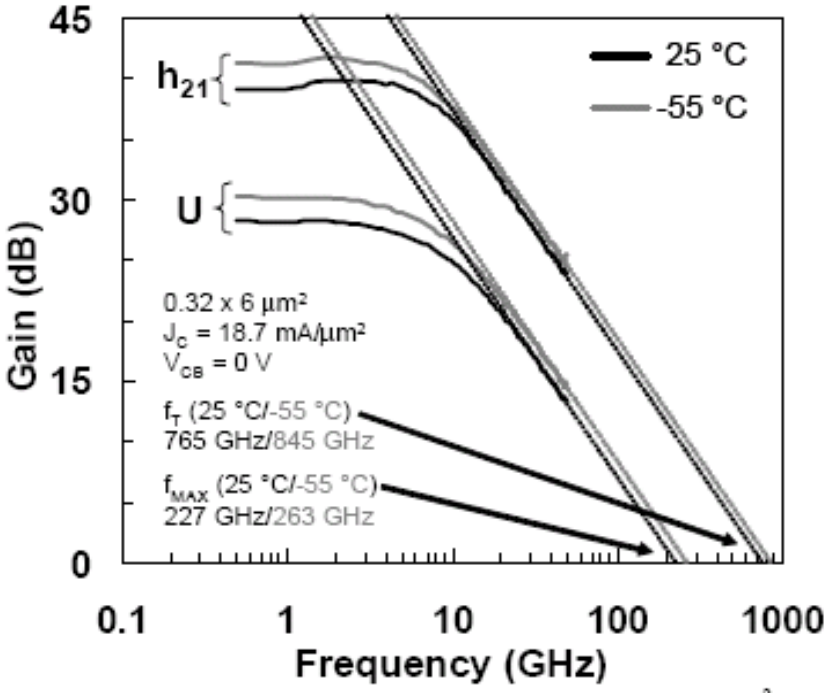


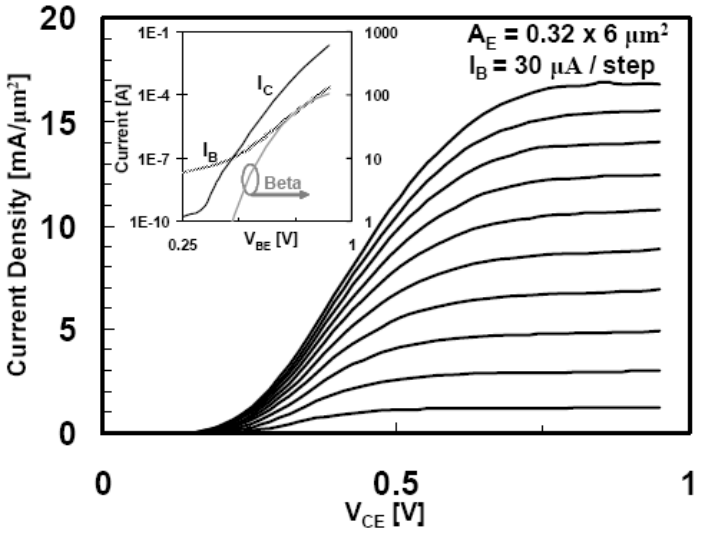
Structure of typical III-V HBT

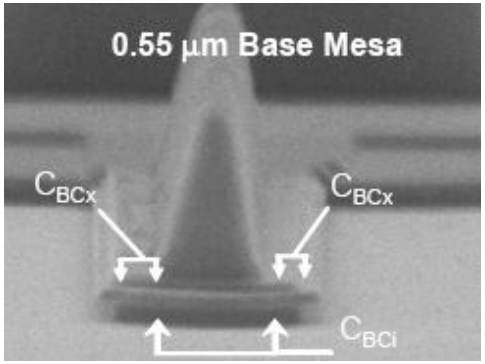


Band diagram of typical III-V HBT

III-V HBT Record Performance



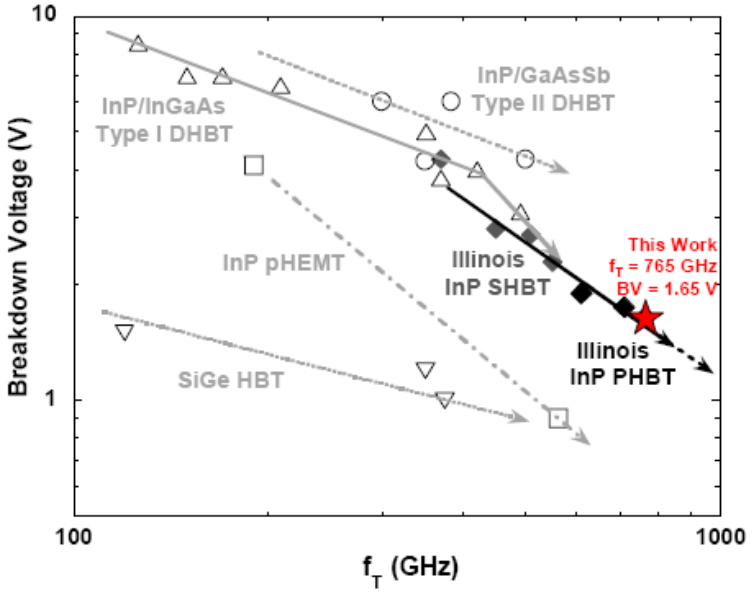


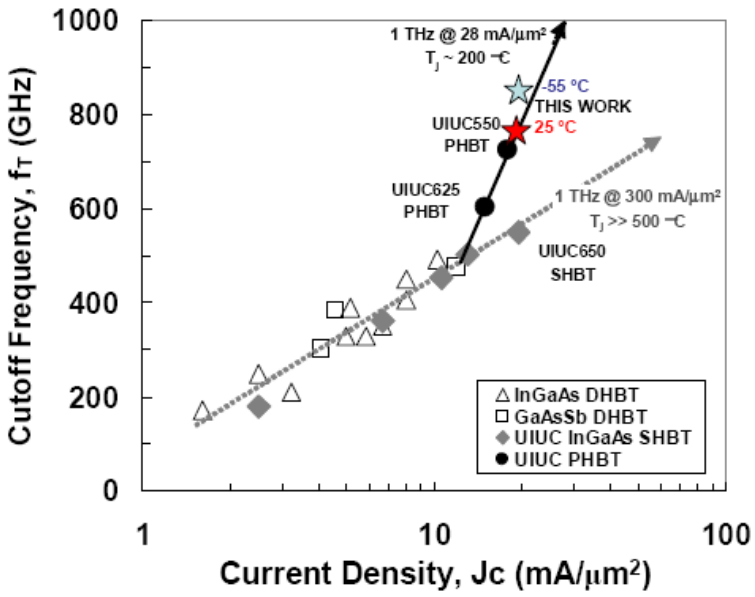


- UIUC
- Peak f_T = 765 GHz at 25C
- Peak f_T = 845 GHz at -55C

Snodgrass et al IEDM 2006

III-V HBT Performance Issues





- Issues with increasing operation frequency
  - Reduction in breakdown voltage → Limits safe operation region
  - Increase in collector current density → Influences reliability

Snodgrass et al IEDM 2006

Inductors

- RF applications
  - RF decoupling
  - Matching networks
  - Feedback inductors
  - LC tank for oscillators
  - Filters
  - Transformers

- Features of interest
  - Inductance (density)
  - Quality factor
  - Self resonance frequency (SRF)

$$Q = \frac{\omega L}{R_s} = -\frac{\mathrm{Im}\left(Y_{11}\right)}{\mathrm{Re}\left(Y_{11}\right)} = \frac{\mathrm{Im}\left(1/Y_{11}\right)}{\mathrm{Re}\left(1/Y_{11}\right)}$$

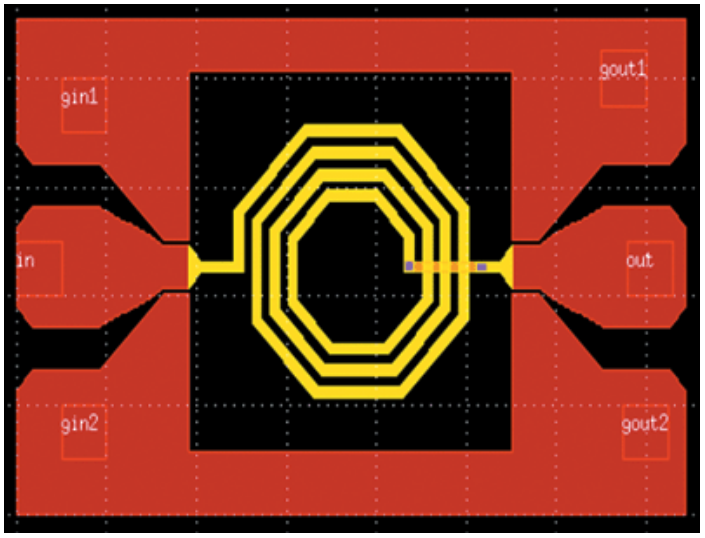
$$L = -\frac{\mathrm{Im}\left(1/Y_{11}\right)}{\omega}$$

Inductors Types

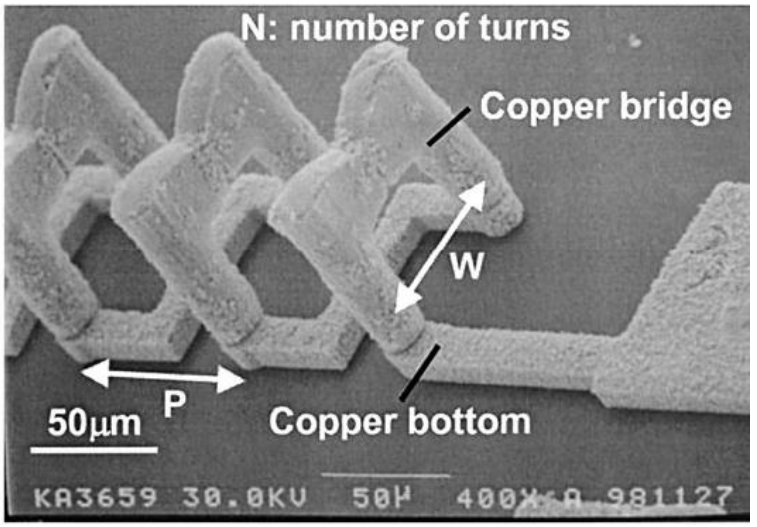
- Spiral inductors
- Solenoid inductors
- Line inductors

Line inductor

Spiral inductor



Solenoid inductor



Yoon et al EDL1999 p487

Capacitors (I)

- RF applications
  - Bias networks
  - DC decoupling
  - Matching networks
  - Filters

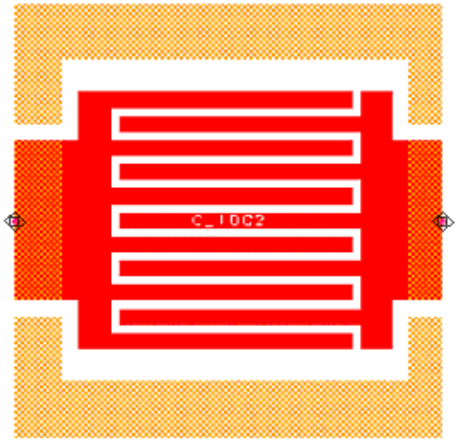
$$Q = \frac{1}{\omega C R_s} = \frac{\mathrm{Im}\left(Y_{11}\right)}{\mathrm{Re}\left(Y_{11}\right)} = -\frac{\mathrm{Im}\left(1/Y_{11}\right)}{\mathrm{Re}\left(1/Y_{11}\right)}$$

$$C = -\frac{1}{\omega\,\mathrm{Im}\left(1/Y_{11}\right)}$$

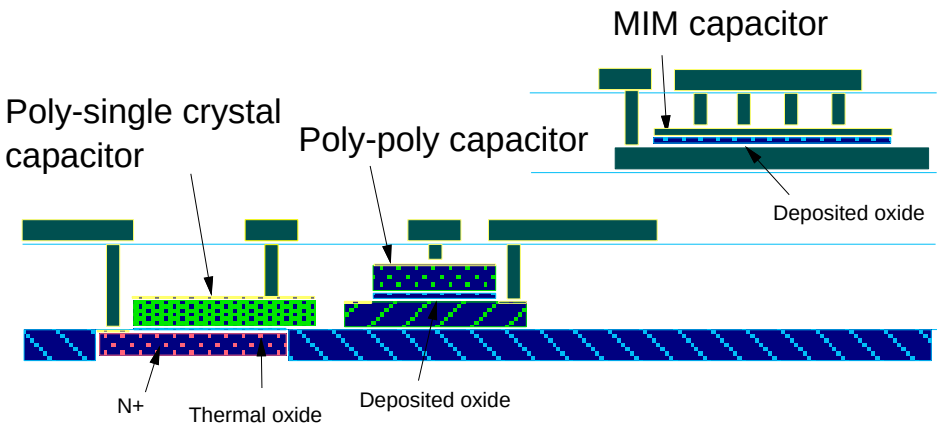
- Features of interest
  - Capacitance (density)
  - Voltage capability
  - Quality factor
  - Voltage coefficient
  - Thermal coefficient
  - Thermal stability
  - Parasitic capacitance
  - N+ dopant influence on oxide

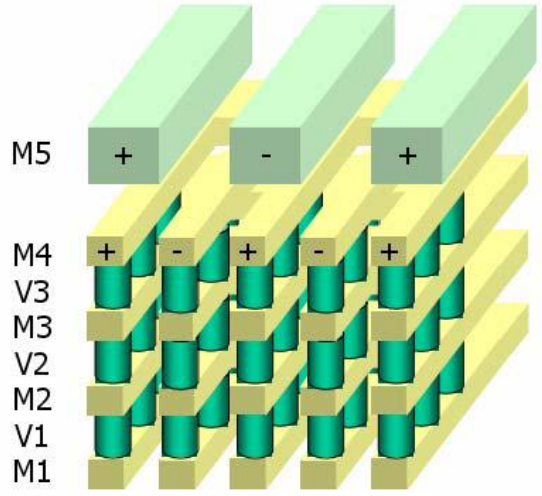
Capacitors (II)

- Device types
  - Interdigitated capacitors
  - MOS capacitors
  - Poly-poly capacitors
  - MIM capacitors
    - Various dielectric materials
  - Vertical natural capacitor (VNCAP)
    - 3D interdigitated cap



Interdigiated cap

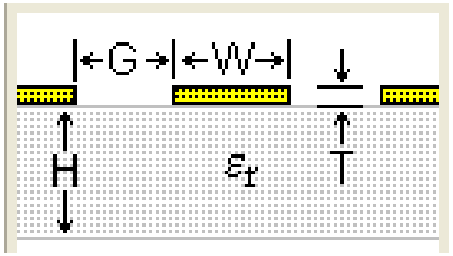




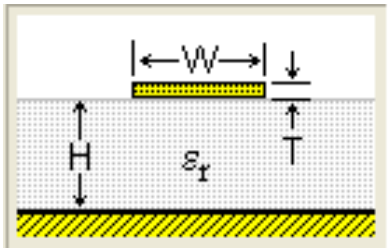
VNCAP (Chen et al 2005 IRPS)

Transmission Lines (I)

- Transmission lines
  - Inherently scalable → one model can be used for various lengths
  - No need to consider the parasitics from interconnection lines
  - Cleary defined ground return path → minimized effect on neighbors
- CPW lines
  - Planar process
  - Subject to high loss when implemented on Si substrate
- Microstrip lines
  - Complex process if backside ground plane employed
  - Provide shield against lossy substrate if M1 used for ground plane



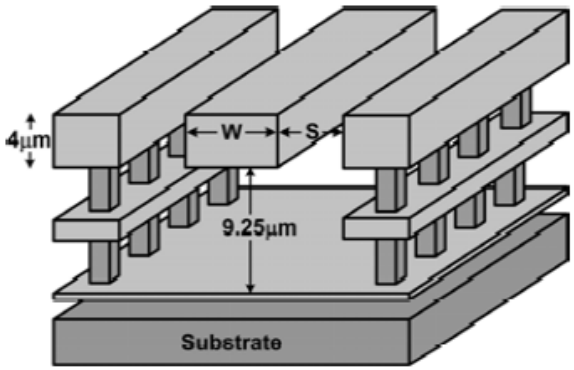
CPW line

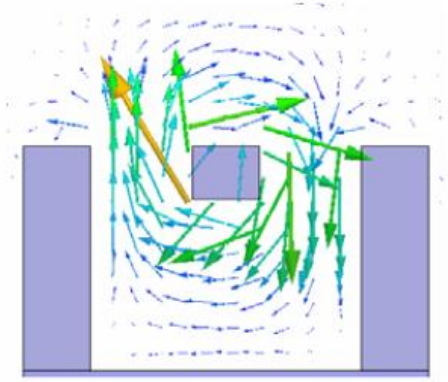


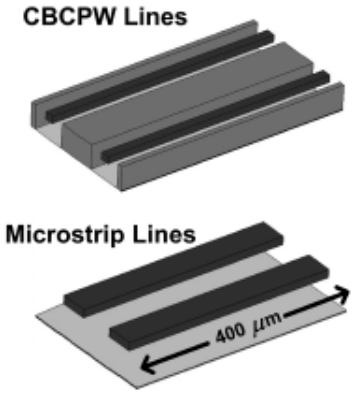
Microstrip line

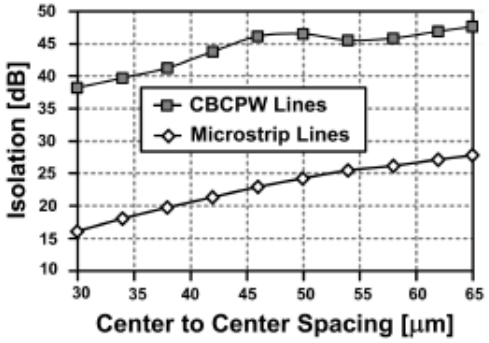
Transmission Lines (II)

- Guided microstrip lines (= Conductor-Backed CPW (CBCPW))
  - Improved loss compared to CPW
  - Improved isolation between parallel lines compared to microstrip









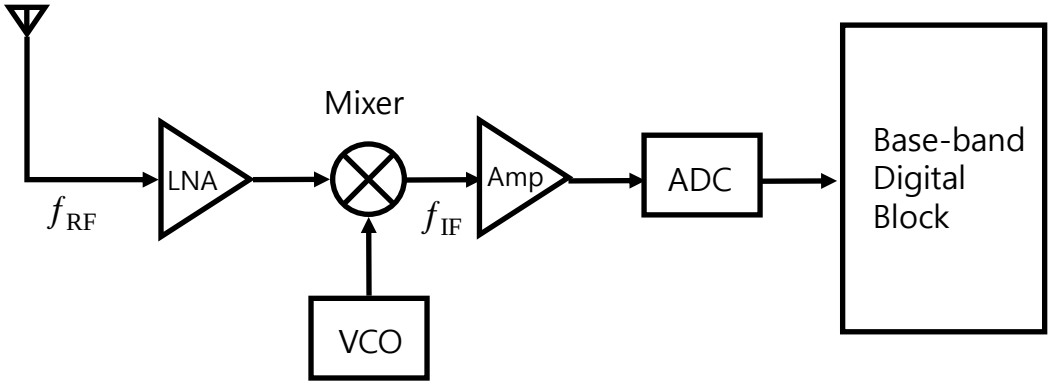
Komijani et al JSSC2006 p.1749

Outline

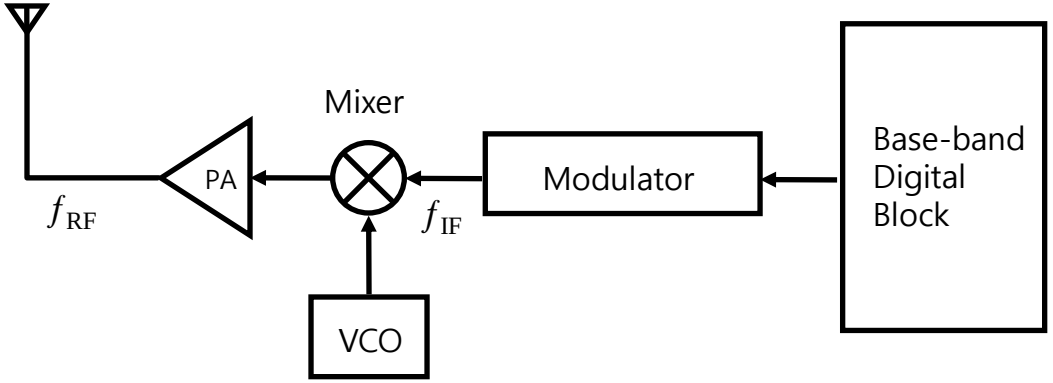
- High Frequency Applications
- High Frequency Semiconductor Devices
- **High Frequency Semiconductor Circuits**

Typical Heterodyne Receiver

- Receiver (RX)



- Transmitter (TX)



Issues for mm-wave LNA Design

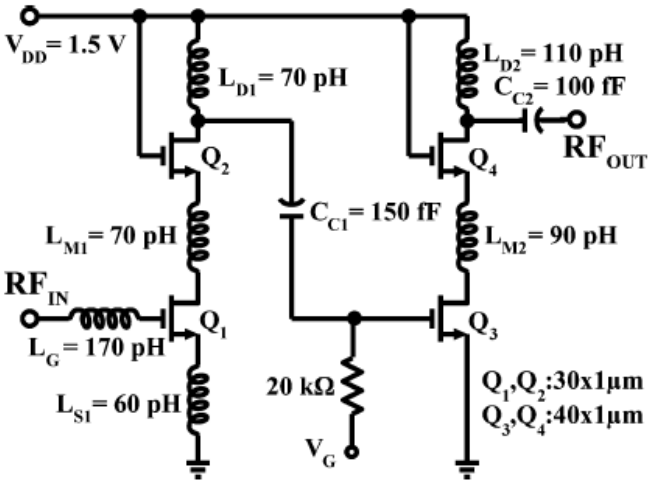
- Gain
  - Limited operation speed of transistors at mm-wave range
  - → Low transconductance and thus gain
- Noise
  - RF noise dominated by transconductance
  - → Low transconductance results in poor NF
- Linearity
  - There is trade-off between linearity and gain
  - Efforts to improve conversion gain degrades linearity
- DC power dissipation
  - Bias current increased for high gain
  - → DC power dissipation increased

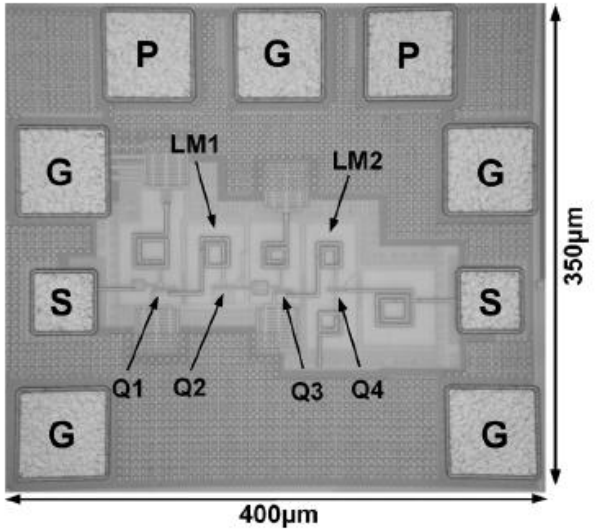
Topology Comparison

- Common Source (Common Emitter)
  - Acceptable power gain
  - Low noise
- Common Gate (Common Base)
  - Acceptable power gain
  - Broadband input impedance match
- Cascode
  - High power gain
  - High noise
  - Better stability (possible to make it unconditionally stable) than CS
  - Better reverse isolation (smaller S12) than CS

58 GHz LNA by U of Toronto (I)

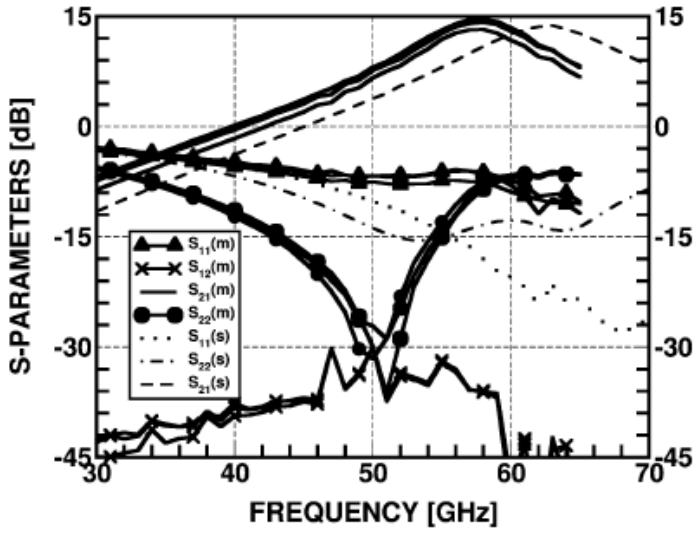
- Basic structure
  - TSMC 90 nm CMOS
  - 2-stage single-ended cascode
  - fT/fmax = 120/200 GHz
- Performance (at 60 GHz)
  - Gain: 14.6 dB
  - NF: 5.5 dB
  - P_{DC}: 24 mW (V_{DD} = 1.5 V)
  - IIP3 = -6.8 dBm
- Notable feature
  - Heavy use of inductors

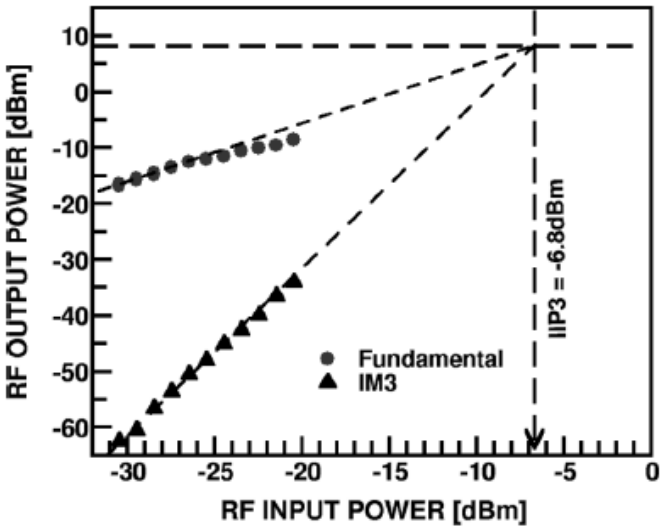




T. Yao, JSSC 2007 p.1044

58 GHz LNA by U of Toronto (II)

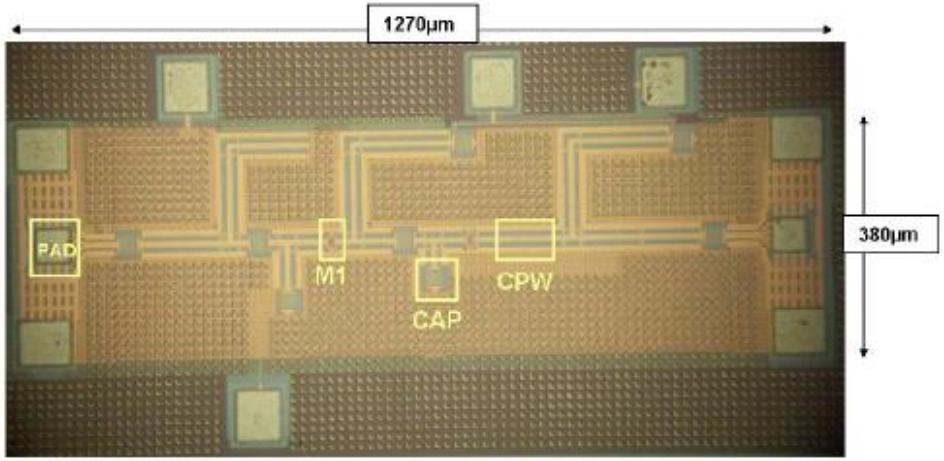


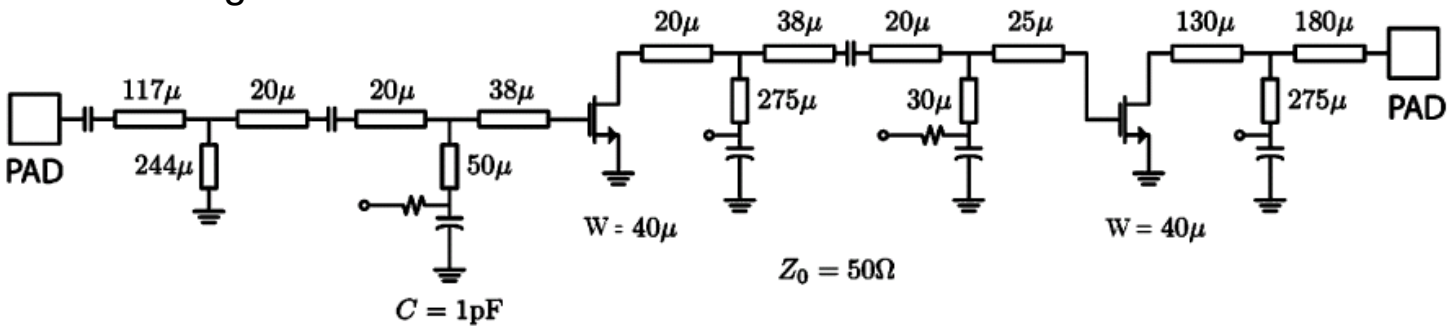


T. Yao, JSSC 2007 p.1044

60 GHz LNA by UC Berkeley (I)

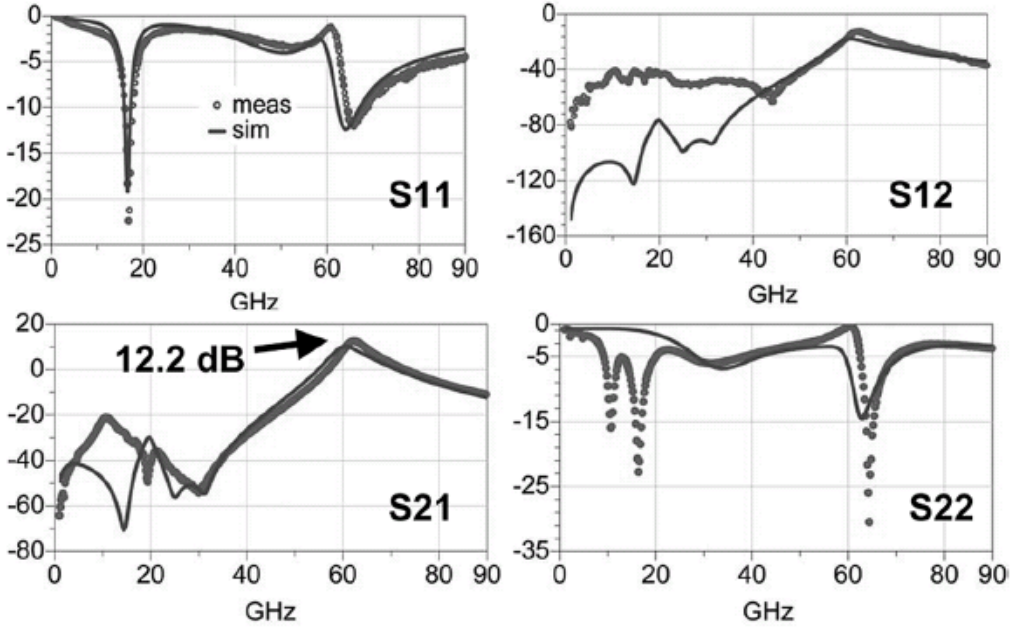
- Basic structure
  - STM 90 nm CMOS
  - 2-stage single-ended CS
  - fmax = 300 GHz
- Performance
  - Gain: 12.2 dB
  - NF: 6 dB (simulated)
  - P_{DC}: 10.5 mW (V_{DD} = 1 V)
  - P_{-1dB} : +4 dBm
- Notable features
  - Round table layout for CMOS
  - CPW matching

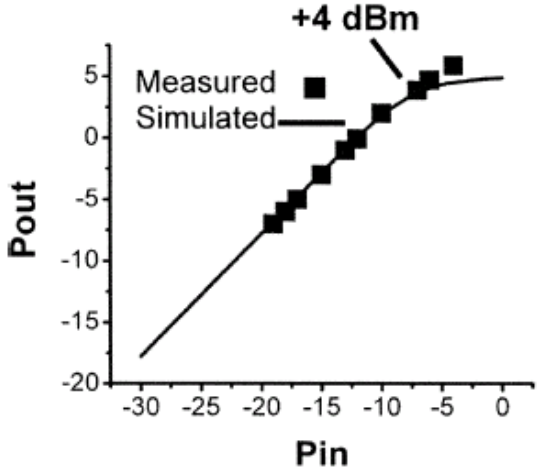


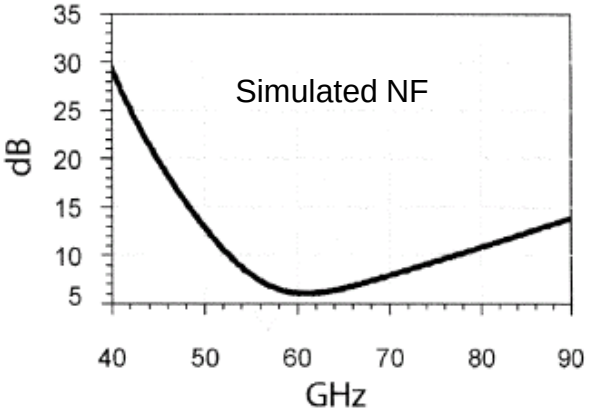


B. Heydari, ISSCC 2007 p.200, JSSC 2007 p.2893

60 GHz LNA by UC Berkeley (II)







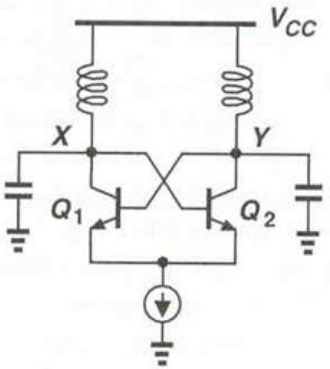
B. Heydari, ISSCC 2007 p.200, JSSC 2007 p.2893

Issues for mm-wave VCO Design

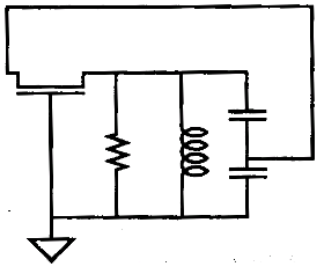
- Phase noise
  - Low Q-factor of LC tank
    → Dominated by the low varactor Q-factor
- Tuning range
  - Capacitance from varactors only a fraction of total capacitance of LC tank
- DC power dissipation
  - Enough g_m required for start-up condition
  - Large bias current required for sufficient g_m
- RF output power
  - Limited by V_{DD} for sufficient tail current
    → Trade-off with DC power dissipation
  - Buffer gain limited by active device g_m

Topologies for VCOs

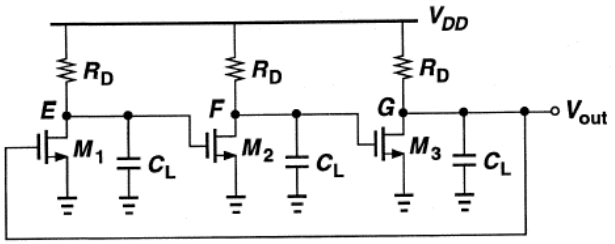
- LC cross-coupled oscillator
  - Relatively easy oscillation start-up condition
  - Lower DC power dissipation



- Colpitts oscillator
  - Better phase noise
  - Large output power
  - Less influence from buffer stage

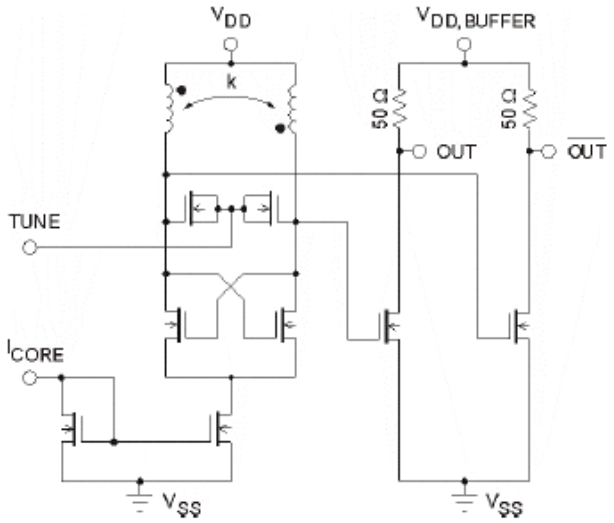


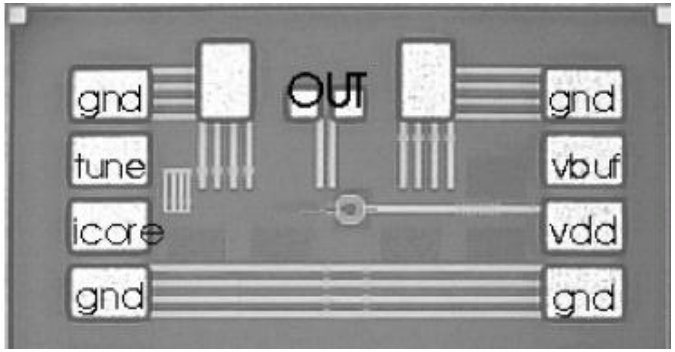
- Ring oscillator
  - Limited phase noise
  - Limited speed



51 GHz VCO by Infineon (I)

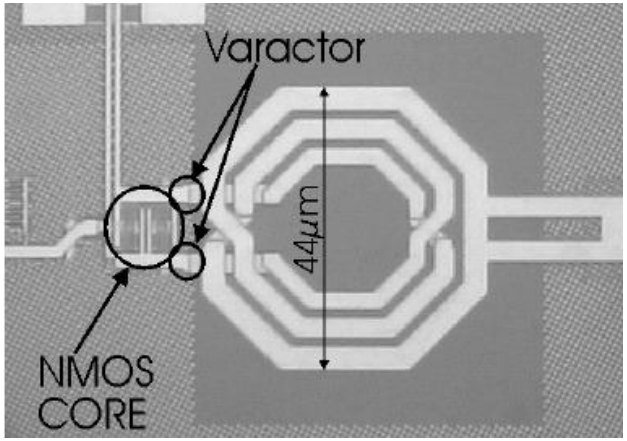
- Basic structure
  - 0.12 um CMOS
  - fT/fmax = 100/60 GHz
  - LC cross-coupled, fundamental
- Performance
  - f_o = 50.2 - 51.6 GHz
  - PN = -85 dBc/Hz at 1 MHz offset
  - P_{DC} (Core)= 1 mW (V_{DD} = 1 V)
  - P_{DC} (Buffer)= 8.25 mW (V_{DD} = 1.5 V)
  - P_{out} = -15 dBm
- Notable features
  - Center-tap inductor
    - Reduced area and substrate capacitance
  - Tapered inductor
    - 20% increase in metal line width for each outward turn

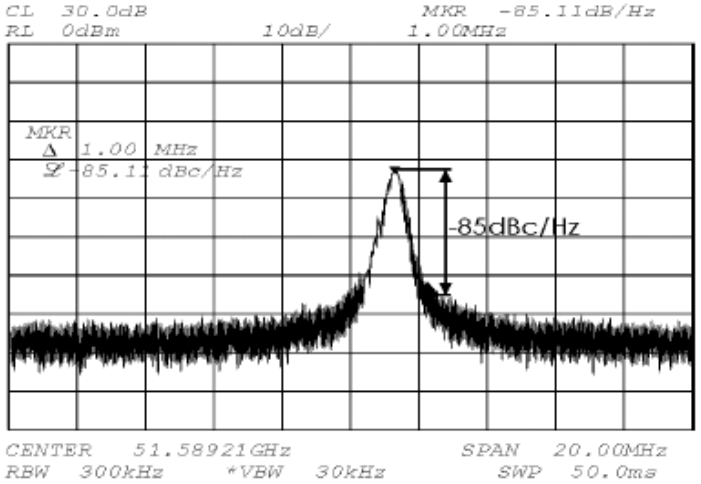


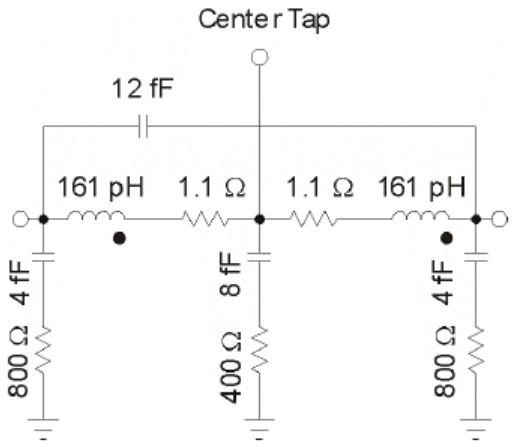


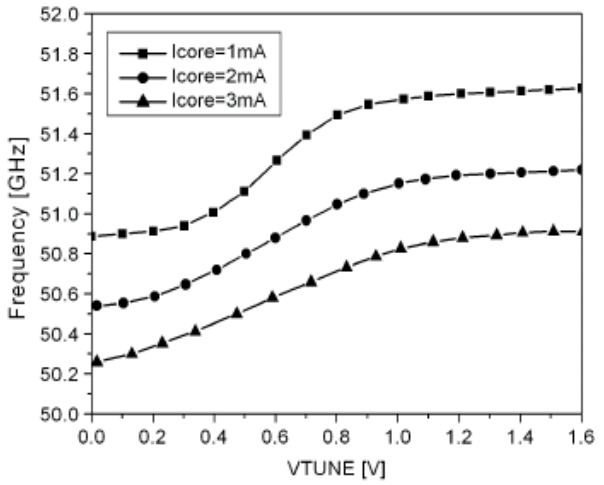
M. Tiebout, ISSCC 2002 p.300

51 GHz VCO by Infineon (II)









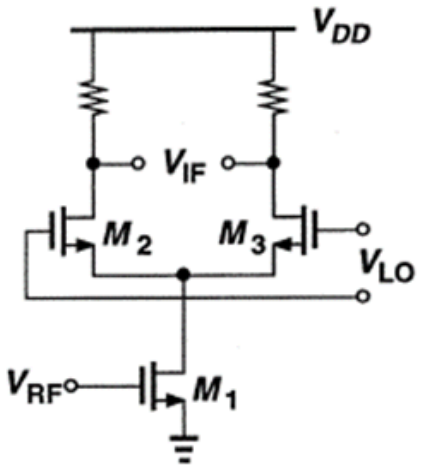
M. Tiebout, ISSCC 2002 p.300

Issues for mm-wave Mixer Design

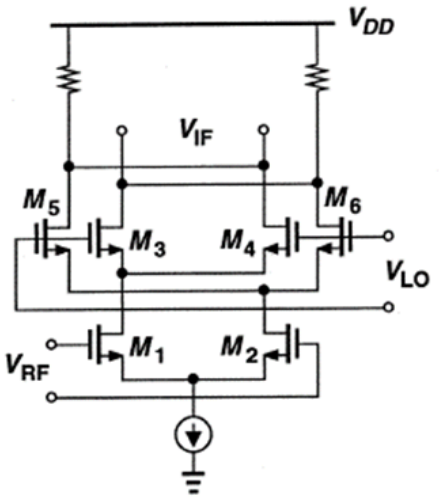
- Conversion gain
  - Limited operation speed of transistors at mm-wave range
  - → Low transconductance and thus conversion gain
- Noise
  - RF noise dominated by transconductance
  - → Low transconductance results in poor NF
- Linearity
  - There is trade-off between linearity and conversion gain
  - Efforts to improve conversion gain degrades linearity
- DC power dissipation
  - Bias current increased for high conversion gain
  - → DC power dissipation increased

Topologies for Mixers (I)

- Single-balanced
  - One input port is balanced, the other is single-ended
  - Compatible with single-ended LNA
  - Compact size and relaxed voltage budget

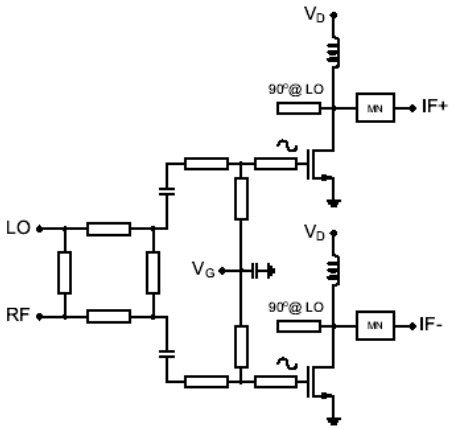


- Double-balanced
  - Both input ports are balanced
  - Excellent immunity to even-mode noise
  - Less LO-IF feedthrough

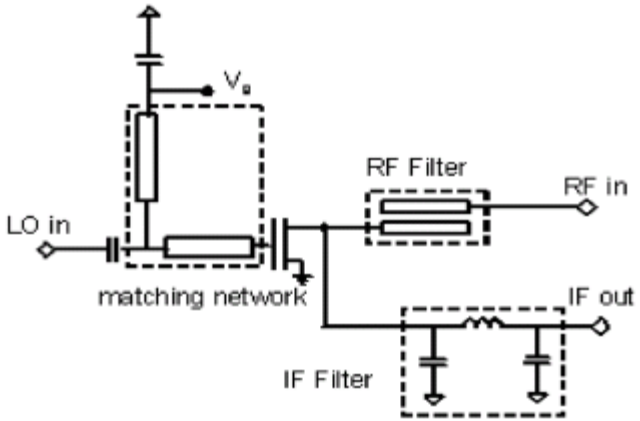


Topologies for Mixers (II)

- Mixer with hybrid coupler
  - Based on nonlinearity of FET devices
  - LO, RF signals are injected through a hybrid coupler
  - Single-ended LO, RF input, differential IF output



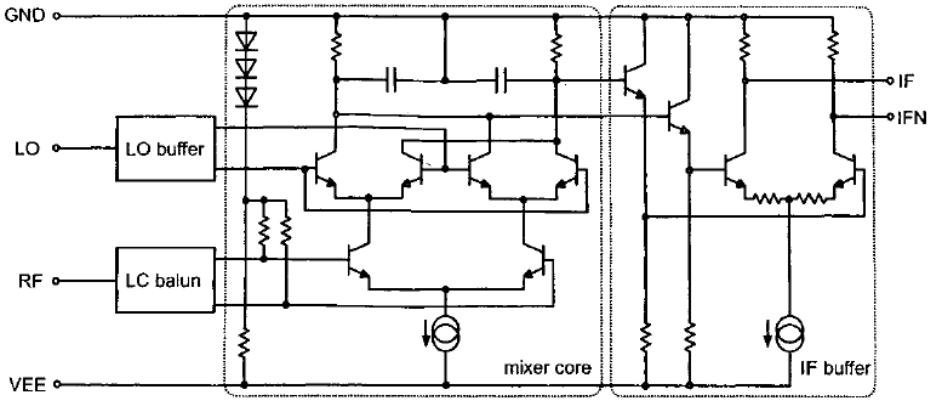
- Resistive mixer
  - Based on a unbiased FET (passive mode operation)
  - LO, RF, and IF applied to electrodes of TR (many options possible)
  - FET operates at triode region
  - Shows very high linearity

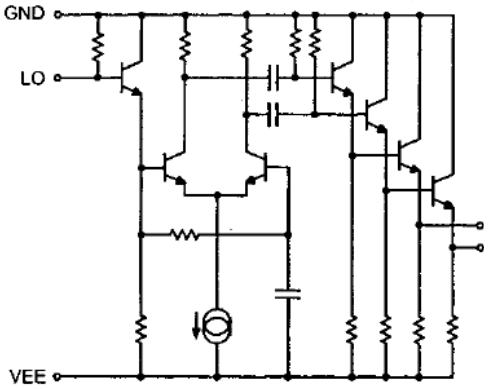


S. Maas, TMTT 1987, p. 425

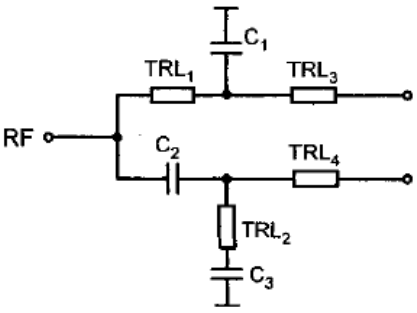
77 GHz Mixer by TUV (I)

- Basic structure
  - Infineon 200 GHz SiGe HBT
  - Double-balanced active
- Performance
  - Conv. Gain > 24 dB
  - SSB NF < 14 dB
  - P_{DC}: 300 mW (V_{CC} = 5 V)
  - P_{-1dB} : -4 dBm
- Notable features
  - LO TR size optimized for best fT
  - RF TR size optimized for best NF
  - On-chip LPF before IF buffer for improved isolation





LO balun



LC Balun for RF input

77 GHz Mixer by TUV (II)

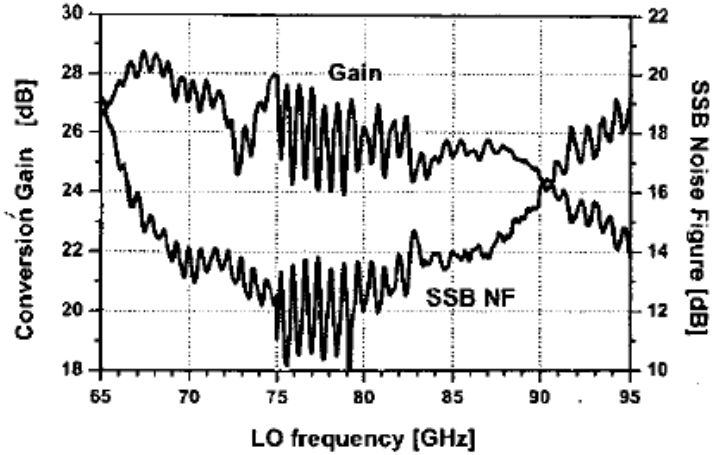


Fig. 6. Measured conversion gain and SSB noise figure versus LO frequency. IF frequency is 500 MHz, LO power is 2 dBm.

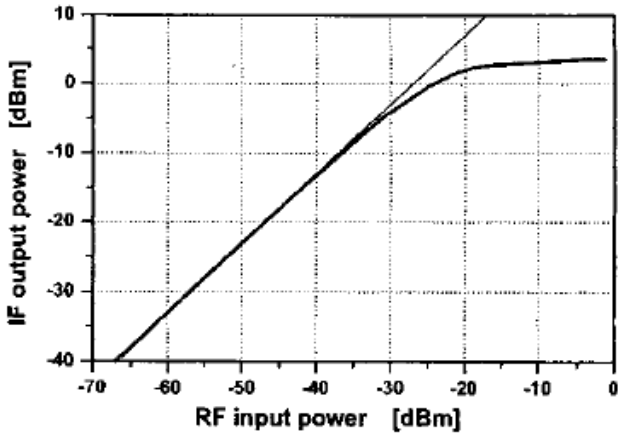


Fig. 7. Measured IF output power versus RF input power. LO frequency is 78.5 GHz, RF frequency is 79 GHz, IF frequency is 500 MHz, LO power is 2 dBm.

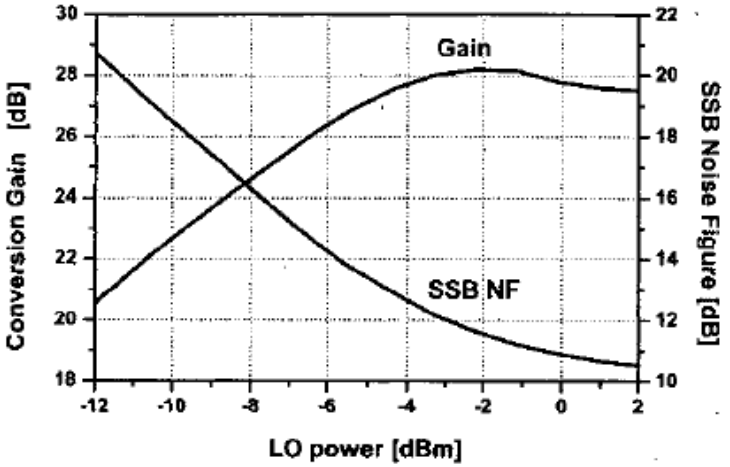
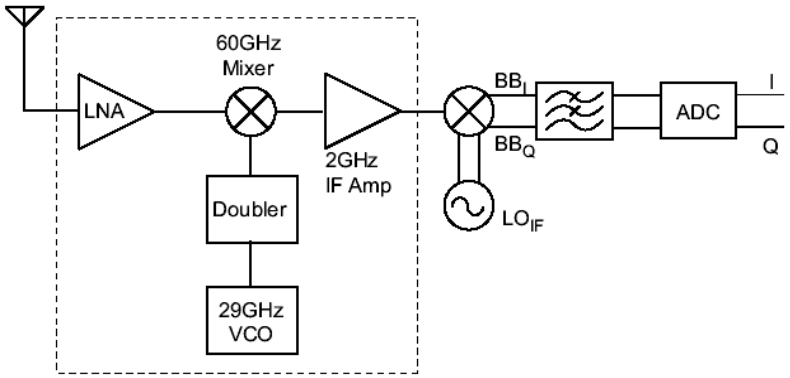


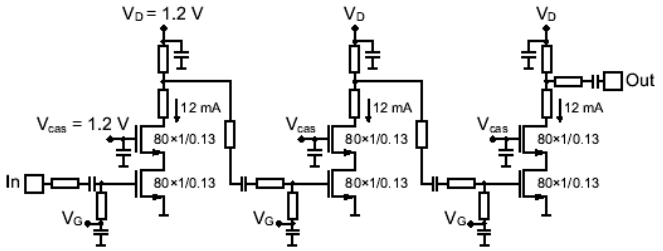
Fig. 8. Measured conversion gain and SSB noise figure versus LO power. IF frequency is 500 MHz, LO frequency is 78.5 GHz.

Integrated 60 GHz RX – SiBeam (I)

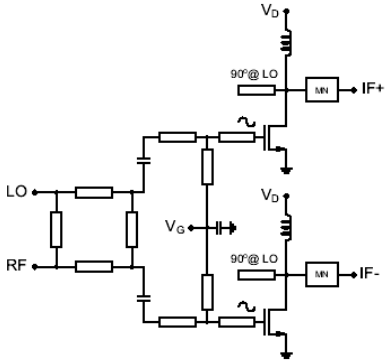


- STM 0.13 um CMOS
- Heterodyne configuration
- RF = 60 GHz
- LO = 58 GHz
- IF = 2 GHz

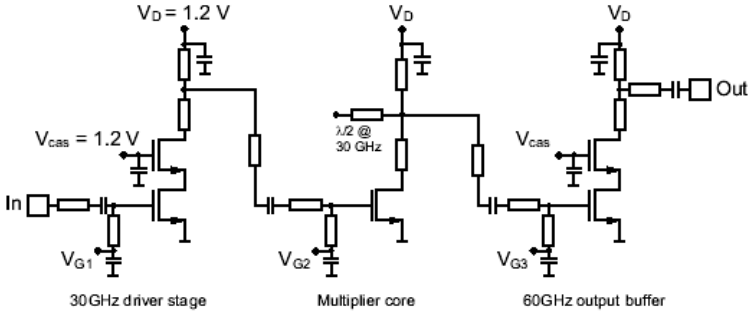
LNA



Mixer

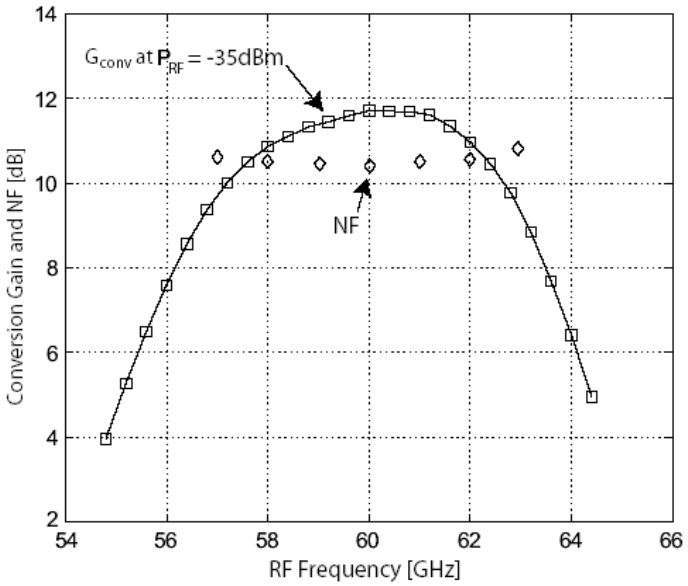


Frequency doubler



Emami et al ISSCC 2007

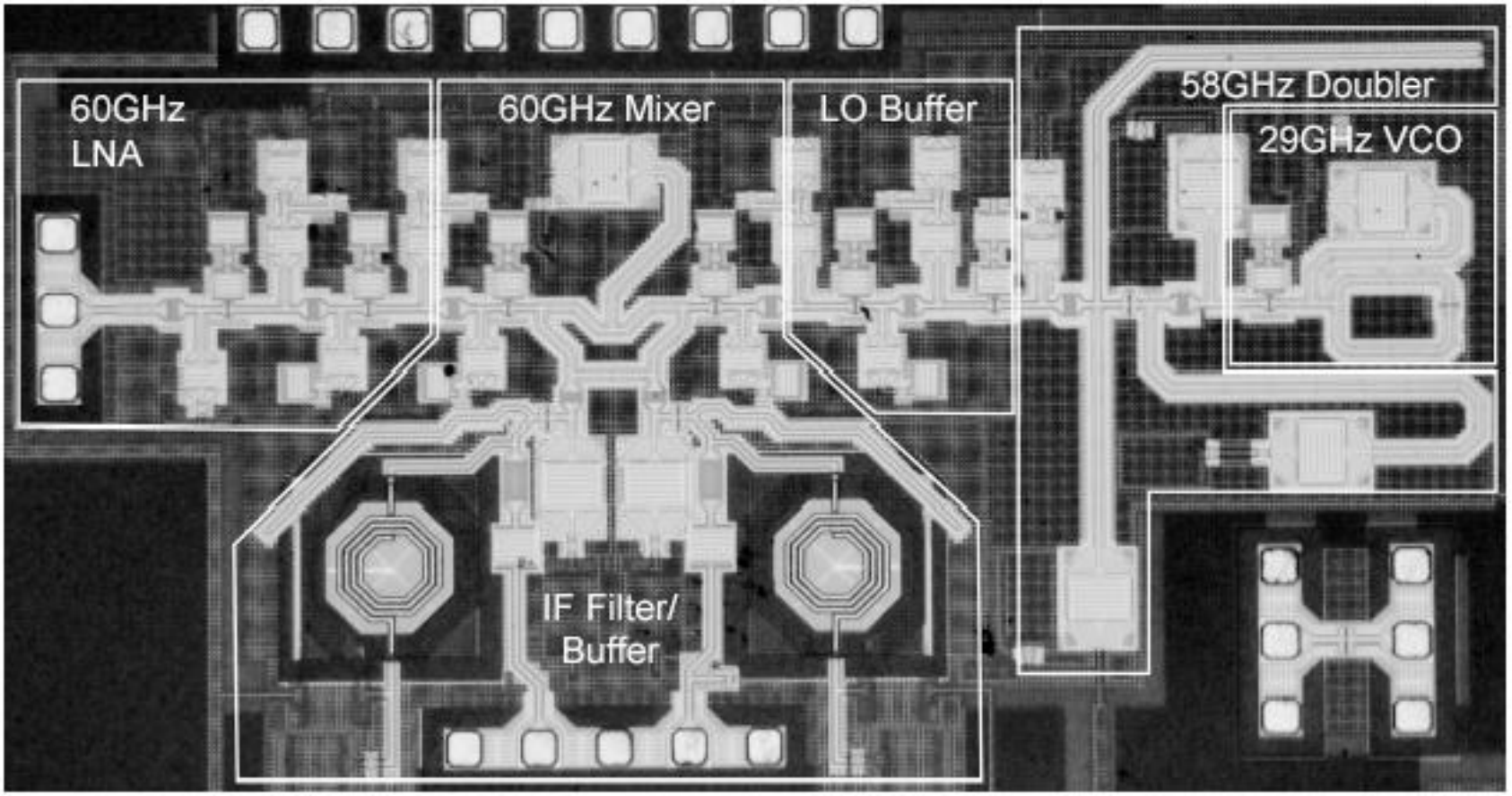
Integrated 60 GHz RX – SiBeam (II)



NF	**10.4 dB**
Gain	**11.8 dB**
1-dB compression	**-15 dBm**
LO phase noise (1 MHz offset)	**-86 dBc/Hz**
Power dissipation	**77 mW**
Supply voltage	**1.2 V**

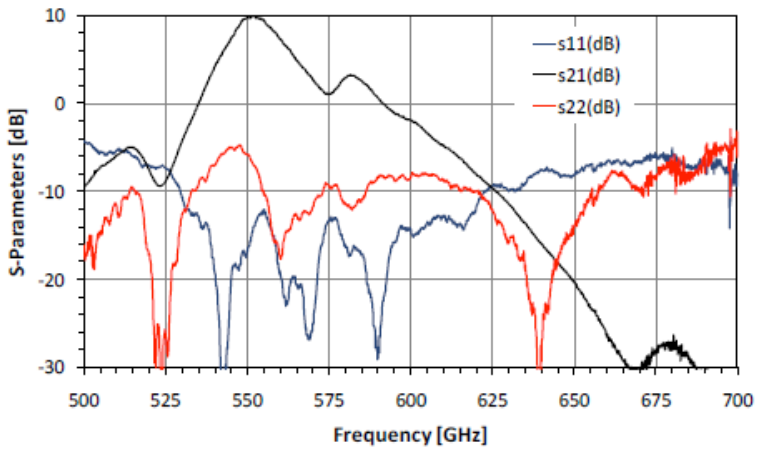
Emami et al ISSCC 2007

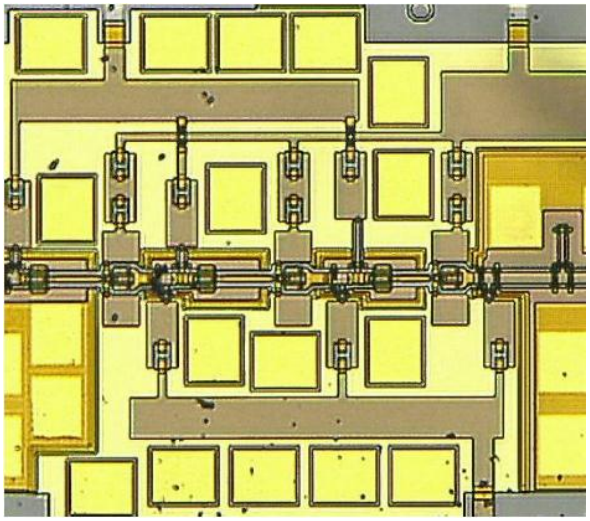
Integrated 60 GHz RX – SiBeam (III)



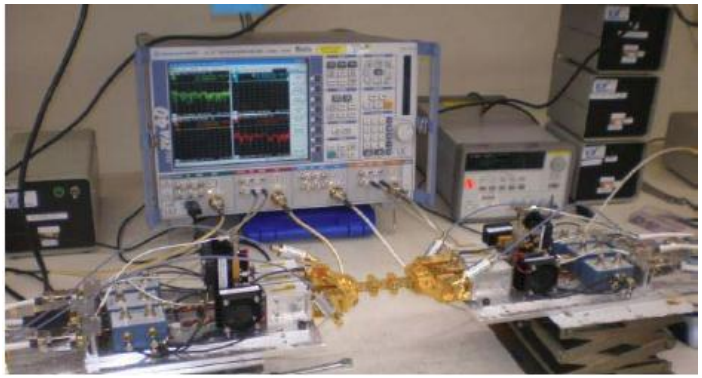
Emami et al ISSCC 2007

550 GHz InP HEMT Amplifier



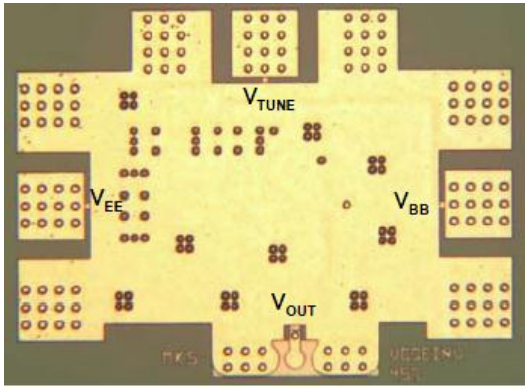


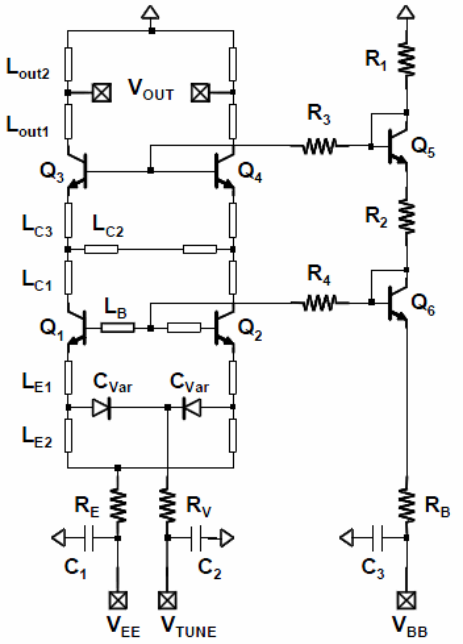
- Northrop Grumman Company
- 50nm NGC InP HEMT
- f_{max} ~ 1.2 THz (estimated)
- 3 stage
- Gain = 10 dB at 550 GHz
  (~15 dB for intrinsic amplifier)
- Integrated dipole probes



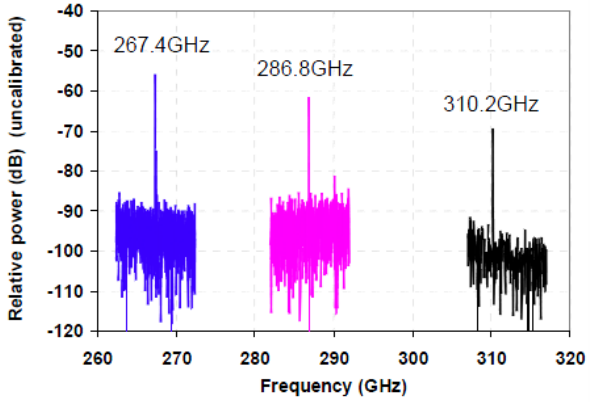
W. Deal et al, CSIC 2010

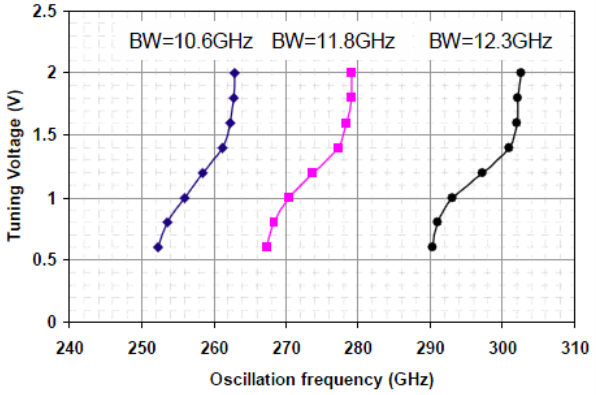
346 GHz InP HBT Fundamental Oscillator





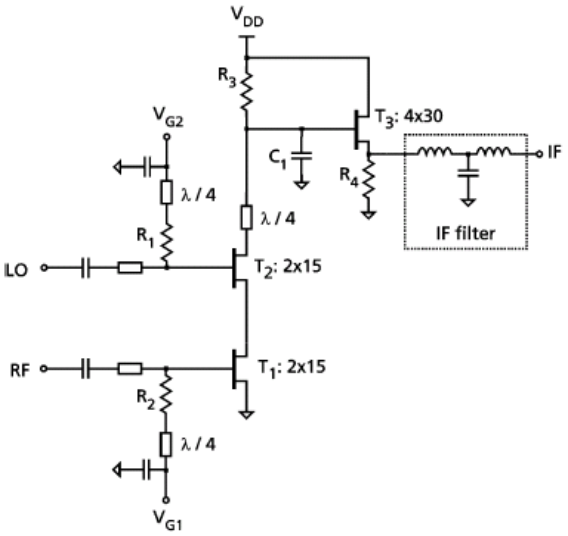
- Teledyne
- 256 nm Teledyne InP HBT
- DC power = 35 mW
- Output power = -11 dBm at 346 GHz
- Frequency tuning around 267, 289, 310, 346 GHz



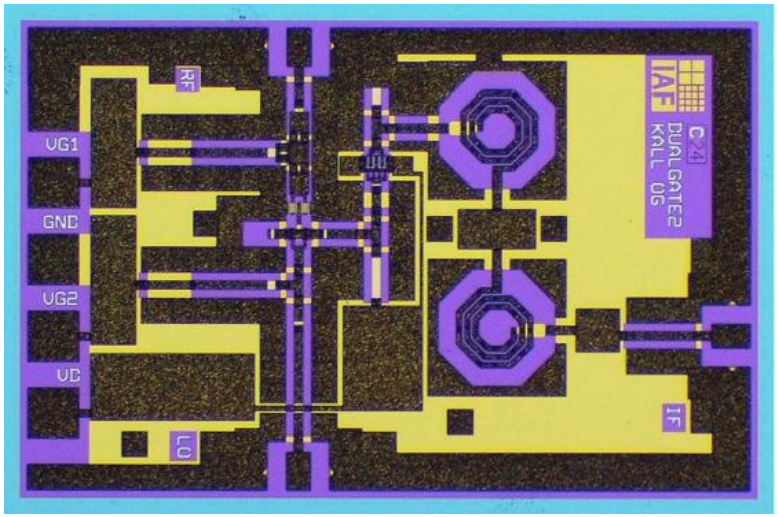


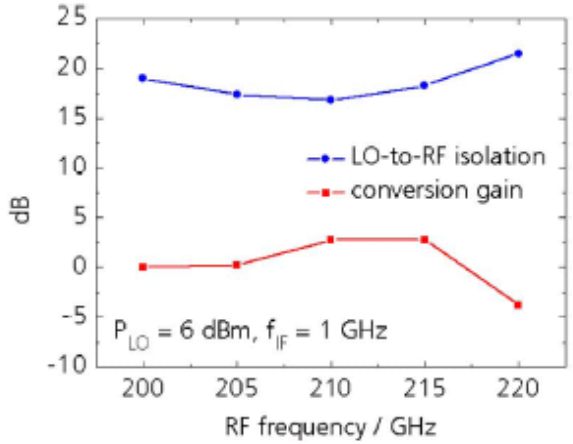
Seo et al, IMS 2010

215 GHz MHEMT Active Mixer



- Fraunhofer Institute
- 0.1 um GaAs MHEMT
- Conversion gain = ~2.8 dB at 215 GHz
- LO-RF isolation = 18.3 dB





Kallfass et al, MWCL 2008