Introduction to Data Converters

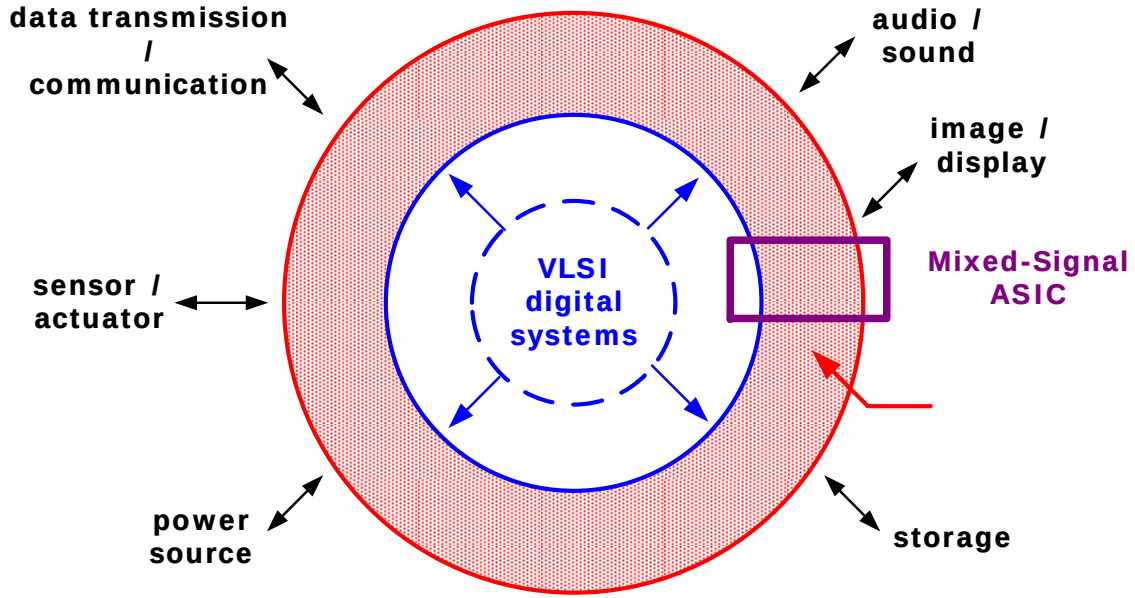
서울시립대학교 최중호

jchoi@uos.ac.kr

2011년 4월 8일

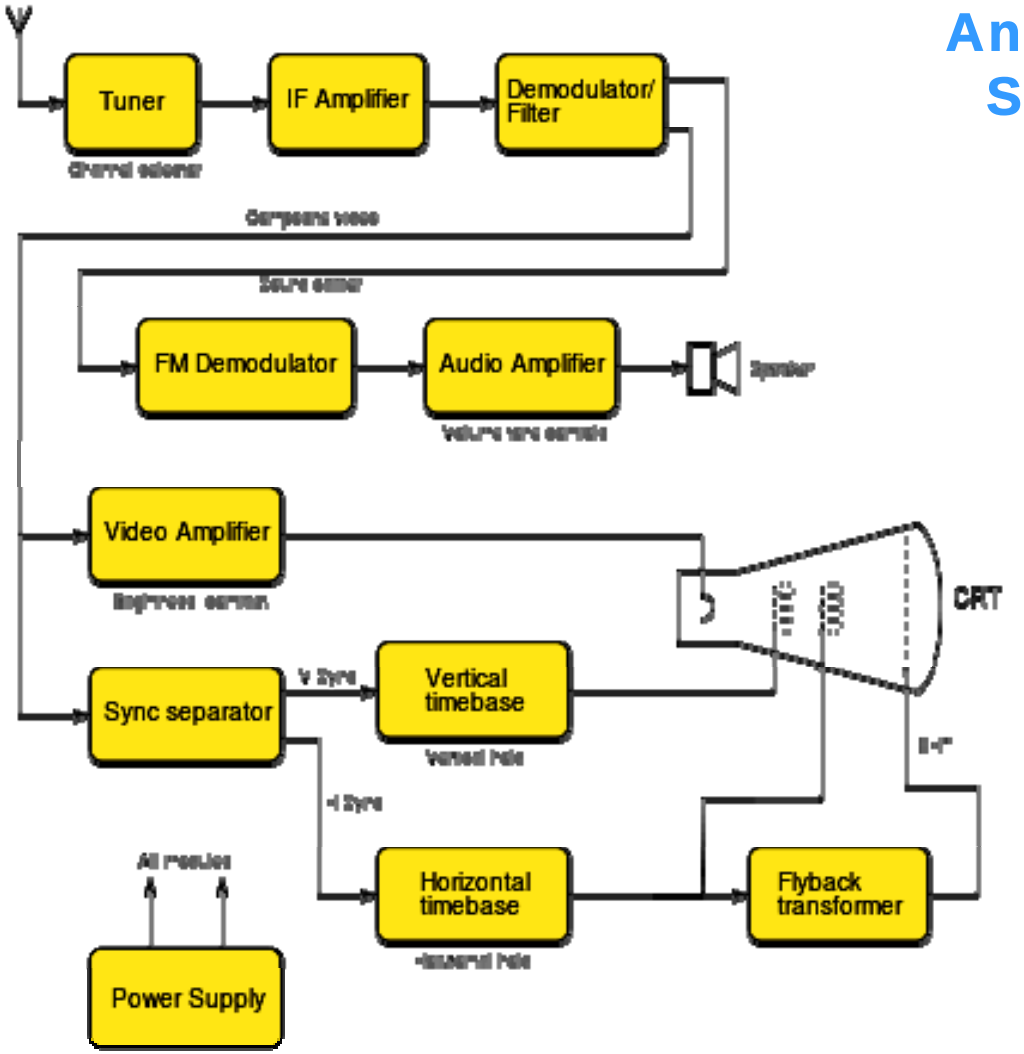
Data Converter Basic

Data Converters for Digital Processing



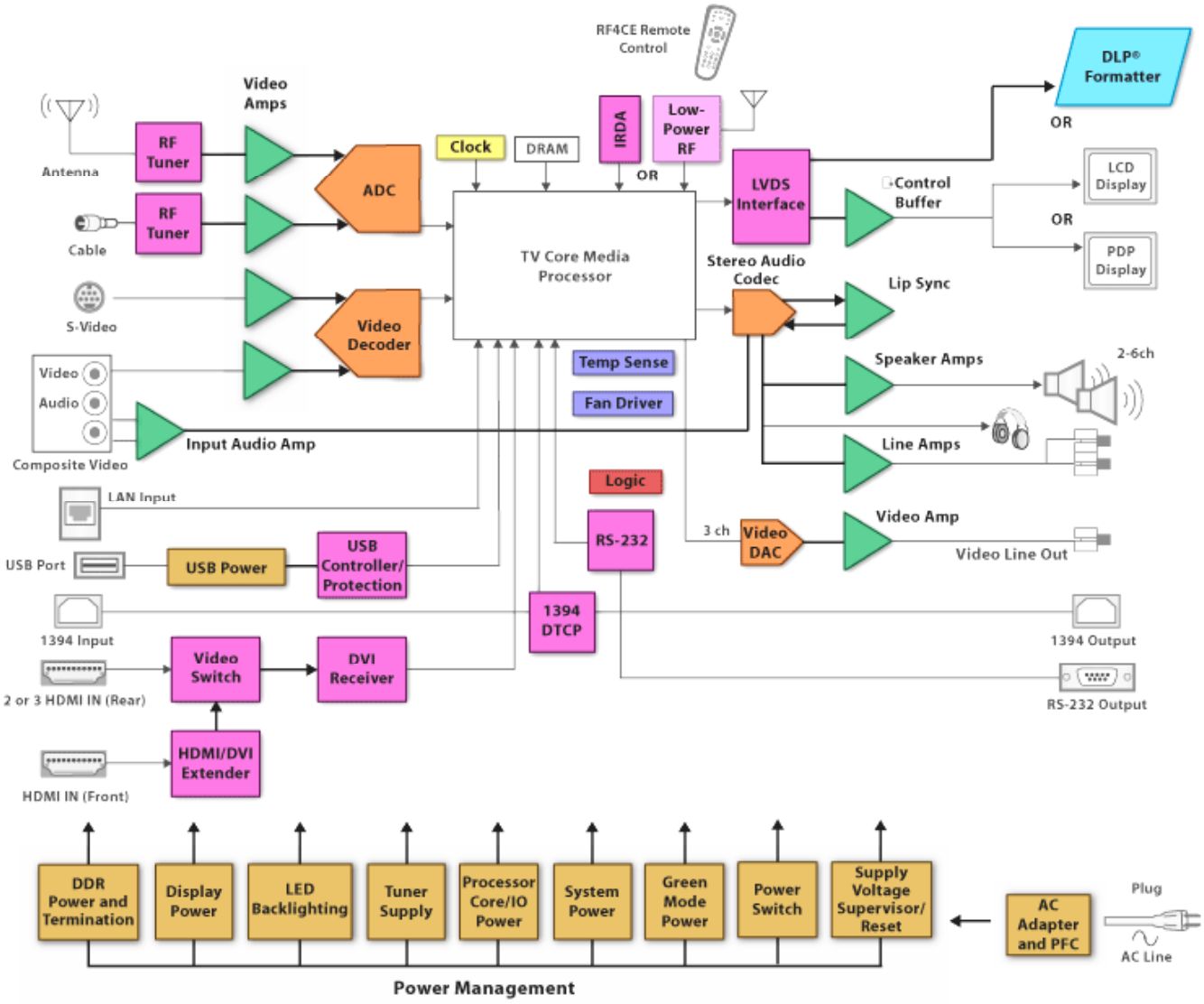
- ADC / DAC : Interface Between Analog Media and Digital Signal Processing System
- Higher Performance of Data Converters Required
- Trends of SoC Implementation
- Main Bottleneck of Design Time and Resources

Data Converter Example for Video (1)



Analog TV System

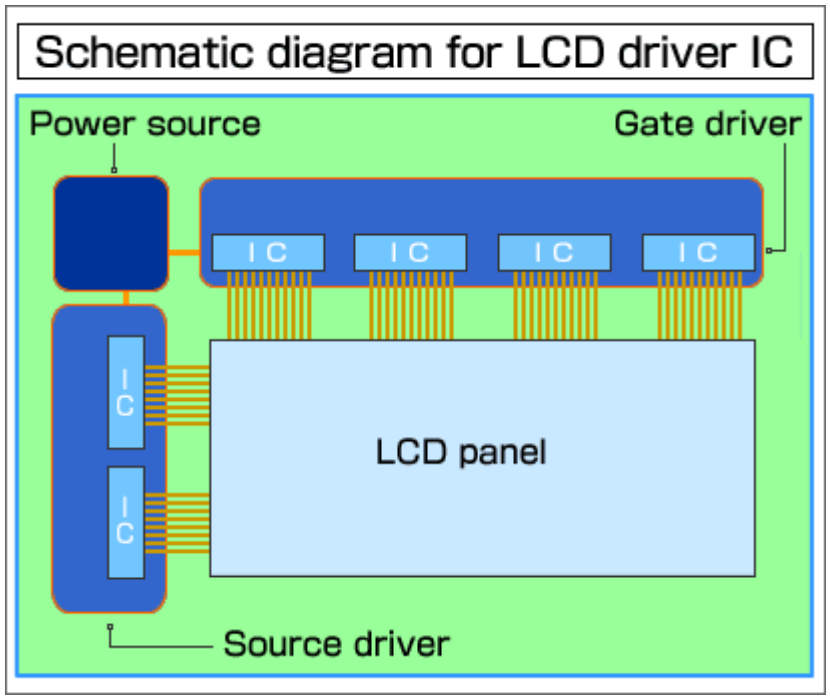
Data Converter Example for Video (2)

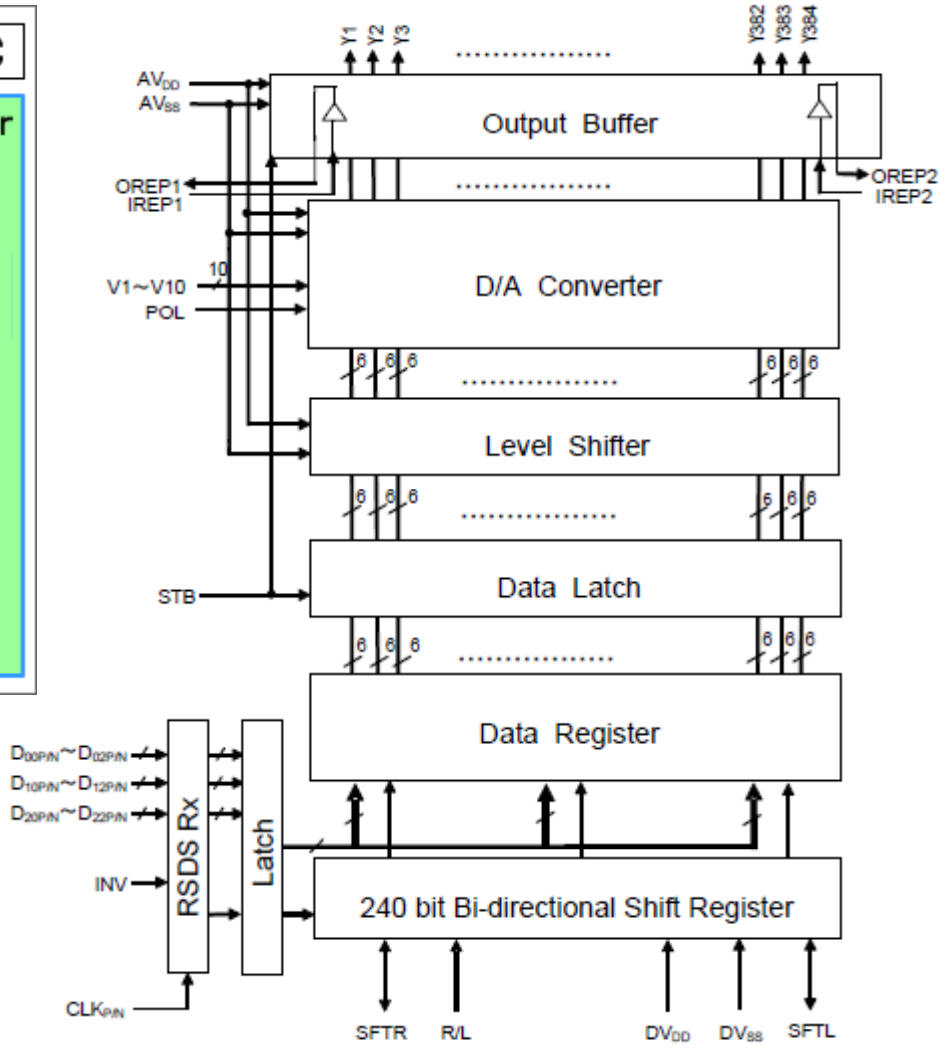


Digital TV System

http://www.ti.com

Data Converter Example for Video (3)

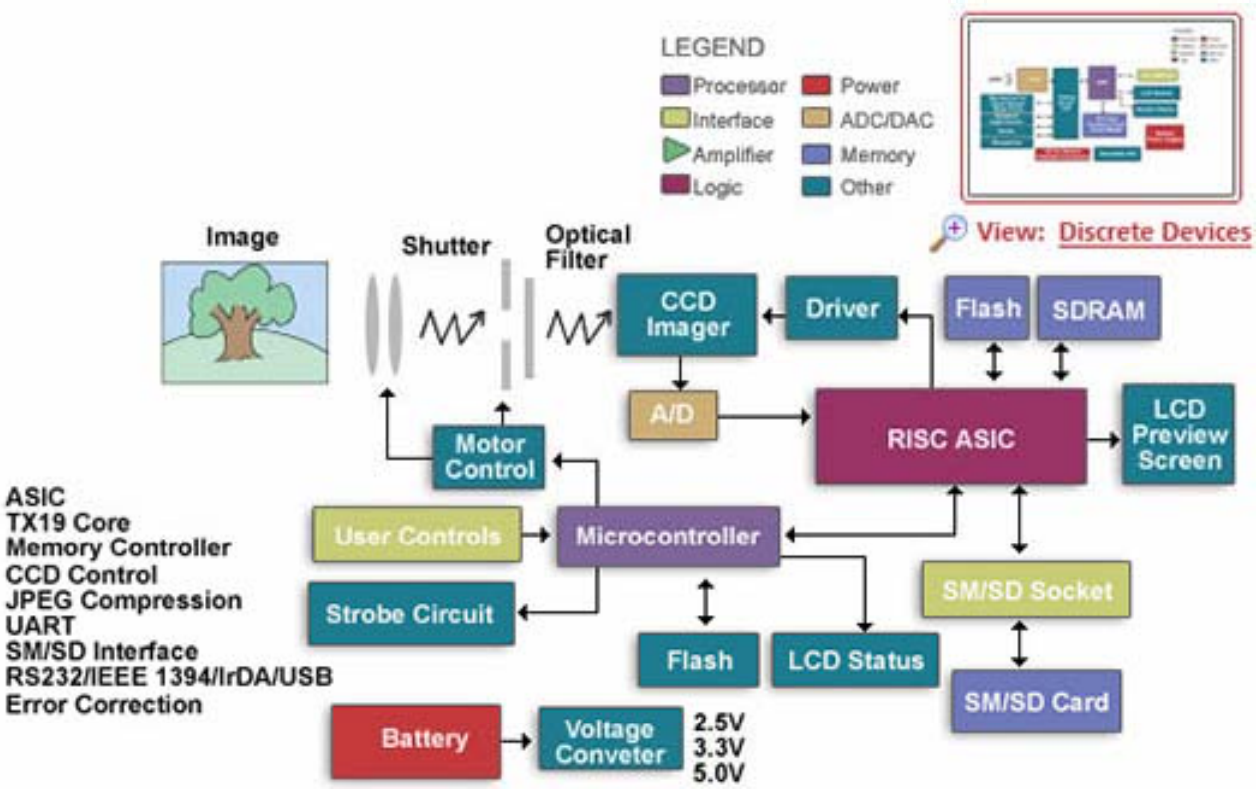




http://www.rohm.com

Data Converter Example for Video (4)

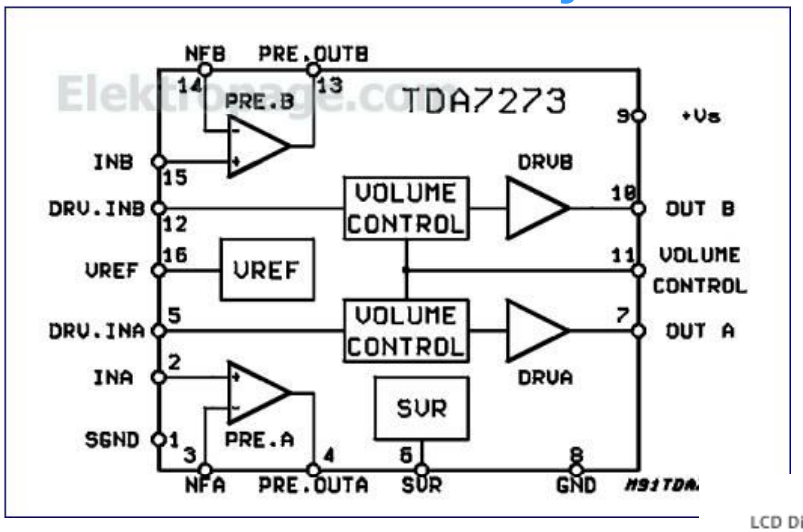
Digital Camera System



http://www.toshiba.com

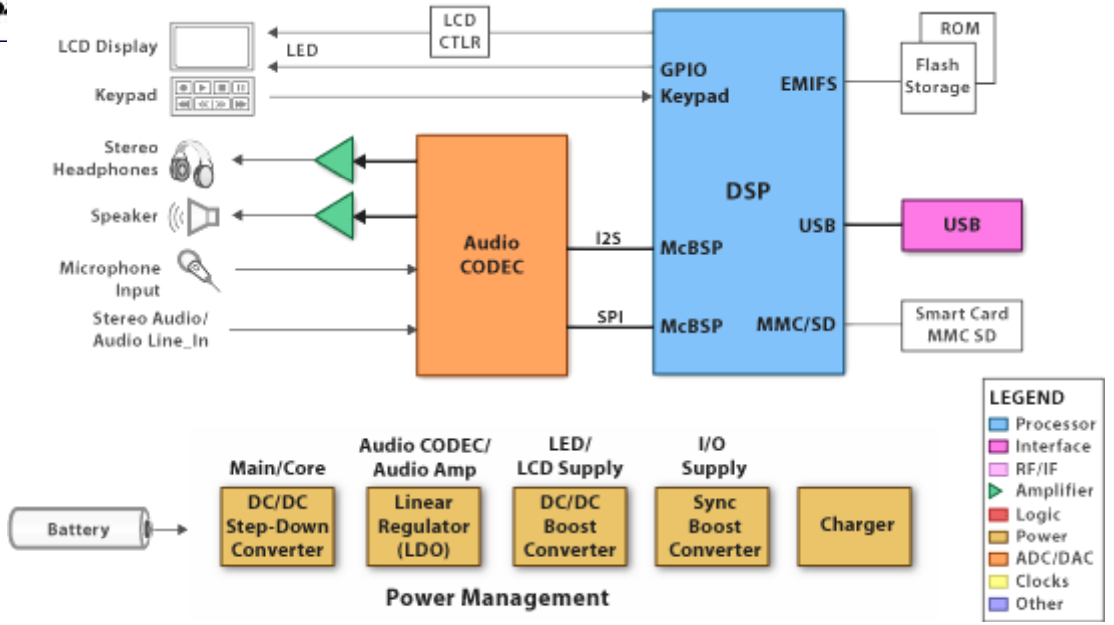
Data Converter Example for Audio

Cassette Player



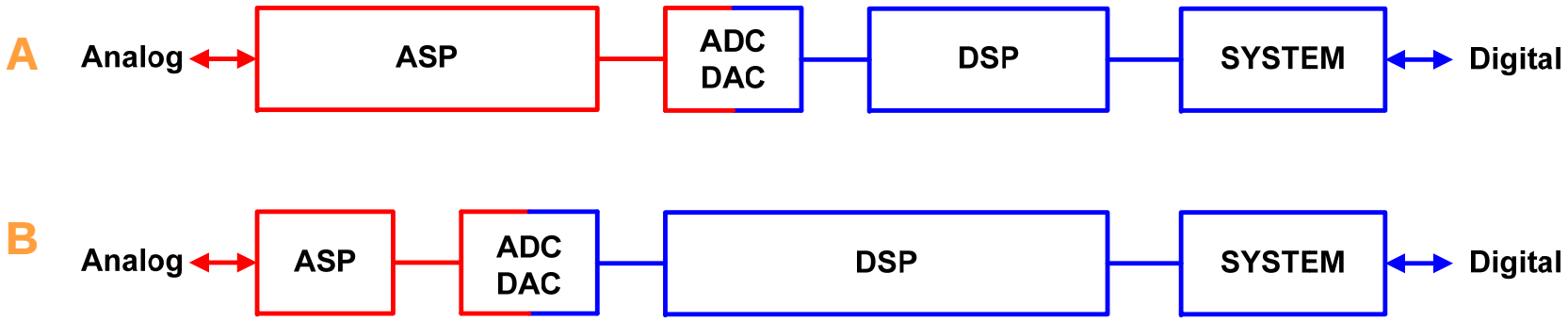
http://www.st.com

MP3 Player



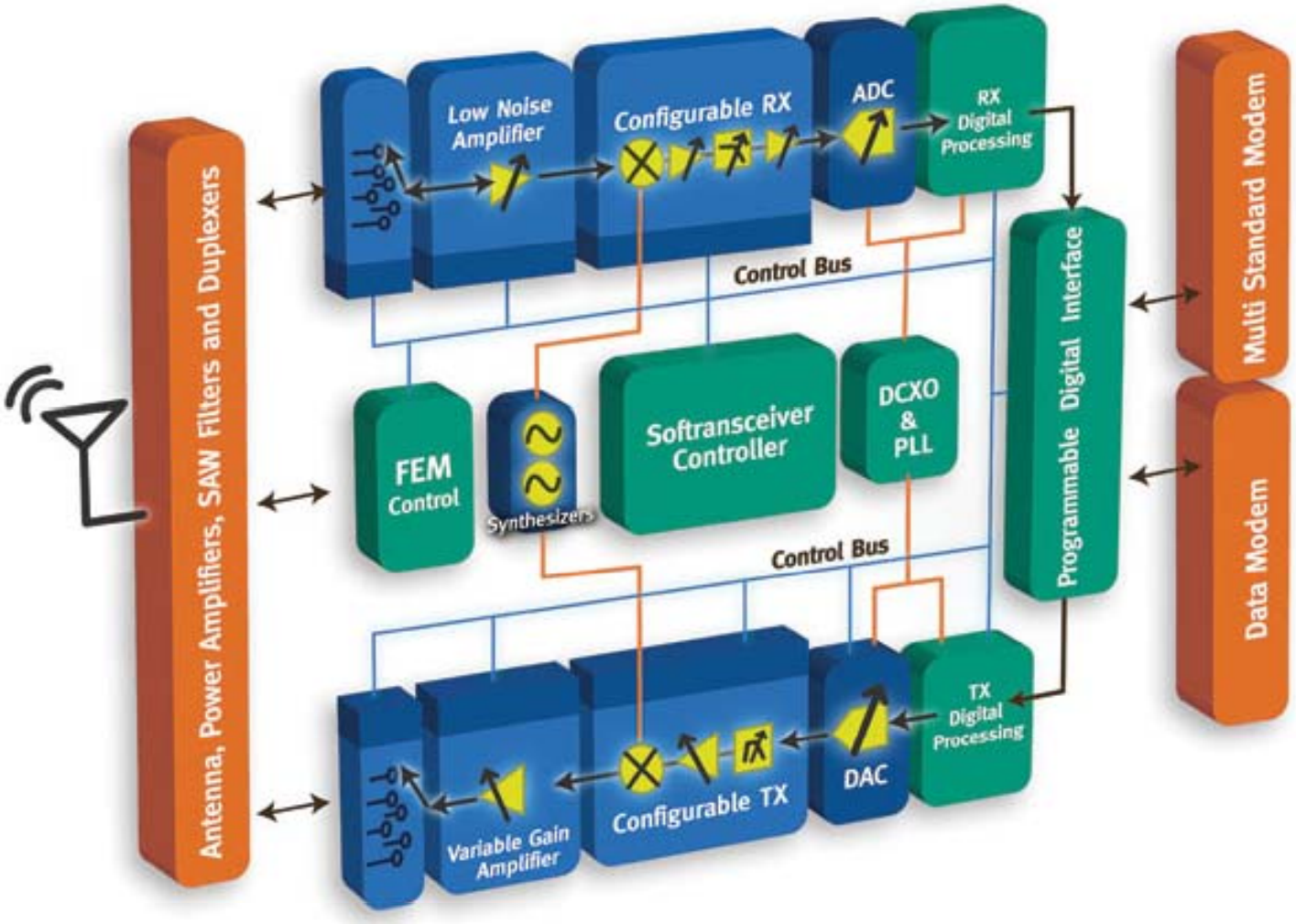
http://www.ti.com

Mixed-Signal ASIC



- VLSI Design & Technology Improvement
  - More Signal Processing Performed in Digital Signal Domain
  - Implementation Trend : A ➔ B
- **Partition** Criteria Determined Mainly By
  - Available Design Resources of Analog Front End
    Such as ADC/DAC & ASP (Analog Signal Processing)
  - Required Performance Specifications : **(B) > (A)**
  - Applications & System Requirements

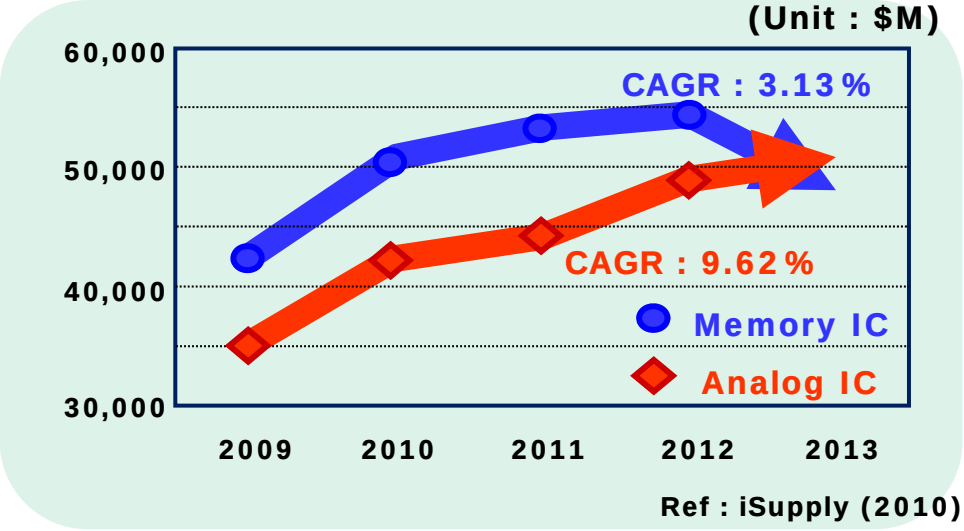
SDR : Software Defined Radio



Analog IC Market

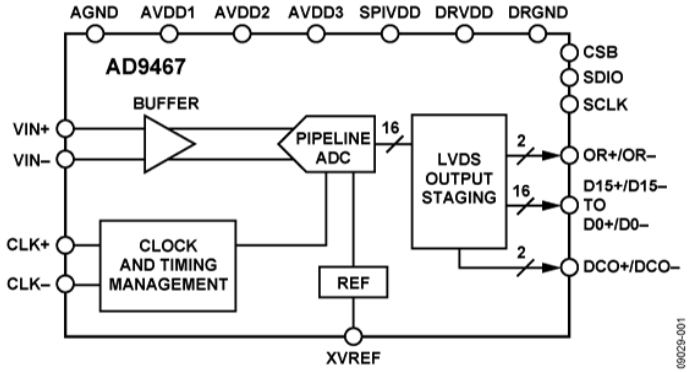
2008년 세계 반도체 분야별 매출 (억$)

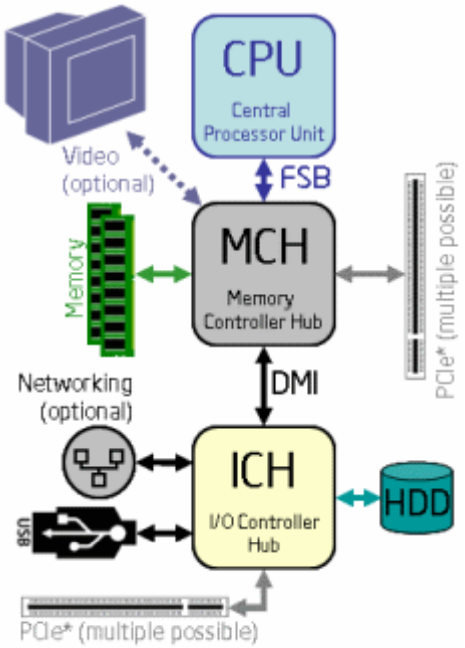
전체 (2,585)				
메모리 (456)		비 메모리반도체 (2,219)		
		시스템반도체 (1,715)		기타 소자 (414)
RAM (254)	ROM (202)	디지털 반도체 (1,283)	아날로그 반도체 (432)	



IC Price Comparison

AD9467-250	16-Bit, 250 MSPS Analog-to-Digital Converter	16	250MSPS	1	-	Multi(+3.3, +1.8)	1.32W	-40 to +85	$100.30

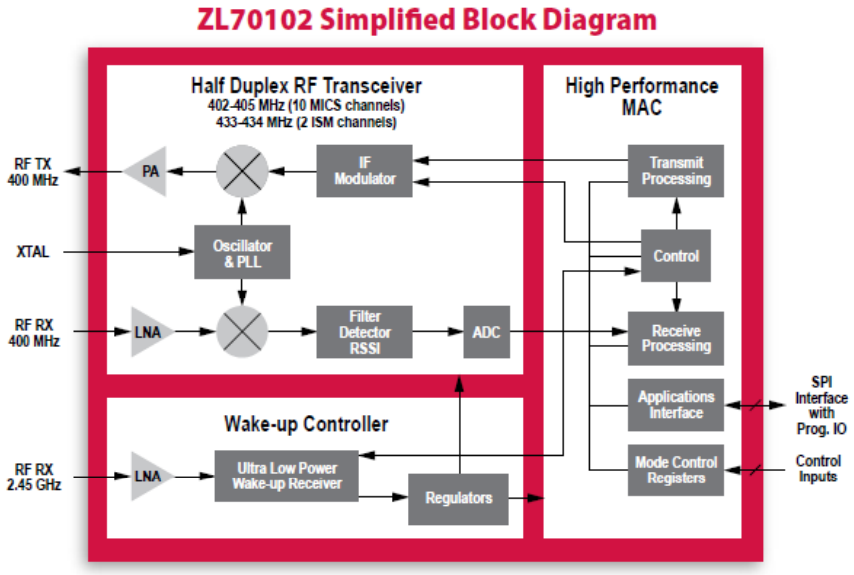




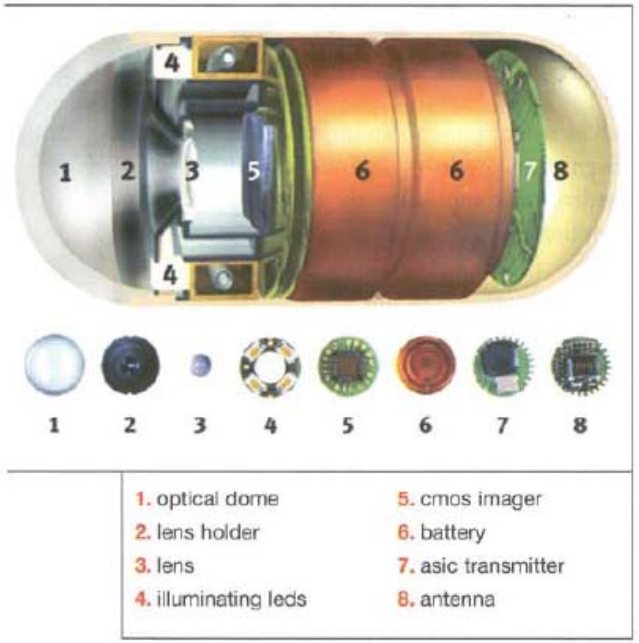
☐	Intel® Core™2 Duo Processor T9600 (6M Cache, 2.80 GHz, 1066 MHz FSB)	No	35 Watts	2C / 2T	Yes	No	$316.00	Launched

Emerging Applications (1)

Implantable Medical Devices



Wireless Endoscopy



http://www.zarlink.com

Emerging Applications (2)

- Wireless Telemetry
- Ubiquitous Sensor Network
- Battery Management System
- Power Control & Energy Harvest

Data Converter Fundamentals

- **Number of Bits**
- **Data Conversion Rate**
- **Power Dissipation / Hardware Area**
- **Static Parameters**
  - Gain & Offset Errors
  - Non-Linearity : DNL (Differential), INL (Integral)
  - Non-Monotonicity, Missing Codes
- **Dynamic Parameters**
  - SNR (Signal-to-Noise Ratio)
  - THD (Total Harmonic Distortion)
  - SNDR (Signal-to-{Noise+Distortion} Ratio)
  - ENOB (Effective Number of Bits)
  - Analog Signal Bandwidth

Input/Output Relation

- **DAC**

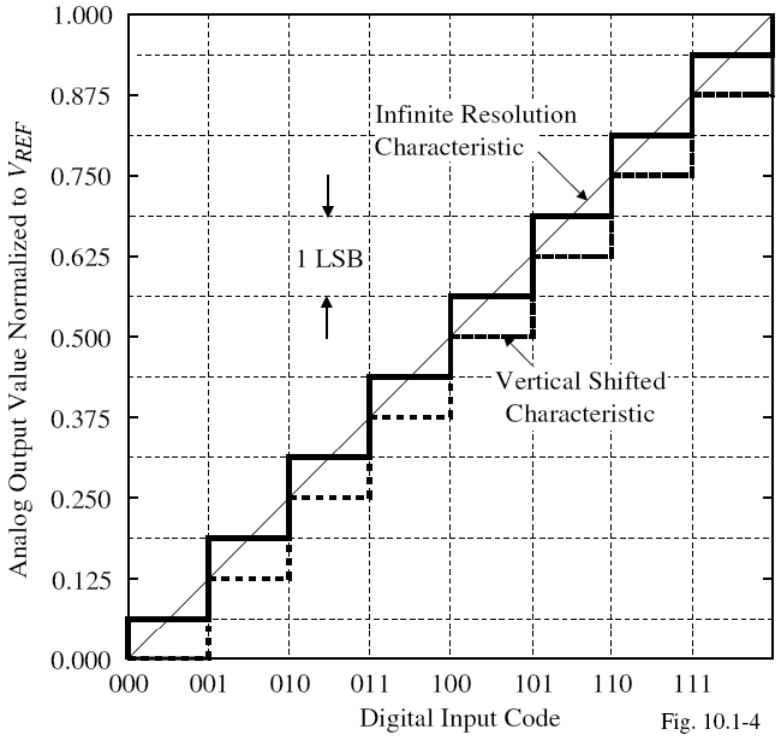
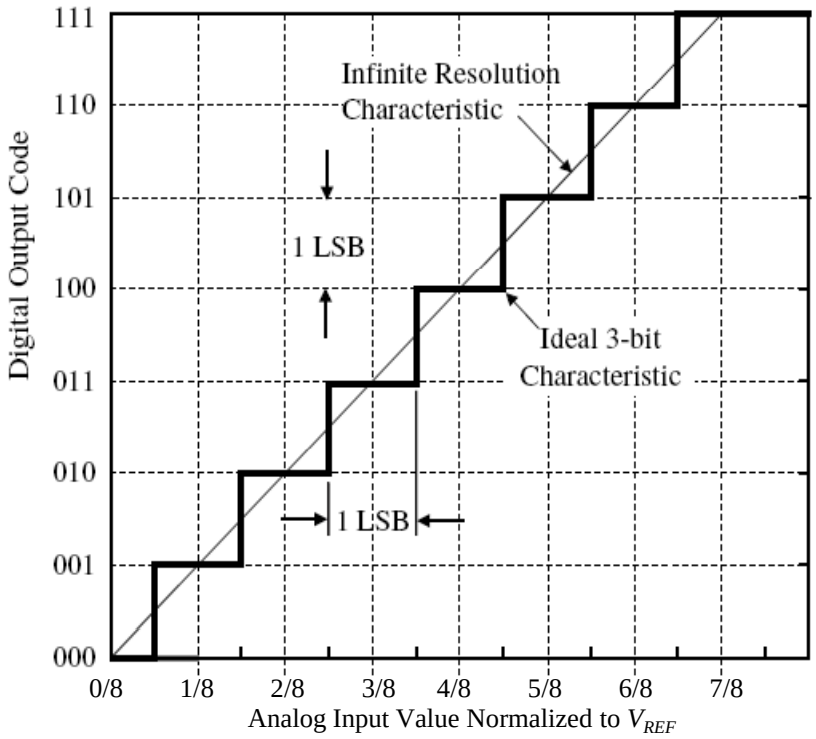


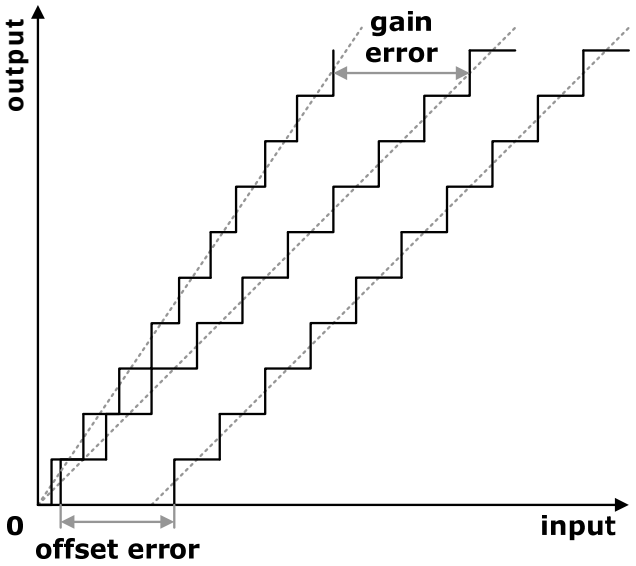
Fig. 10.1-4

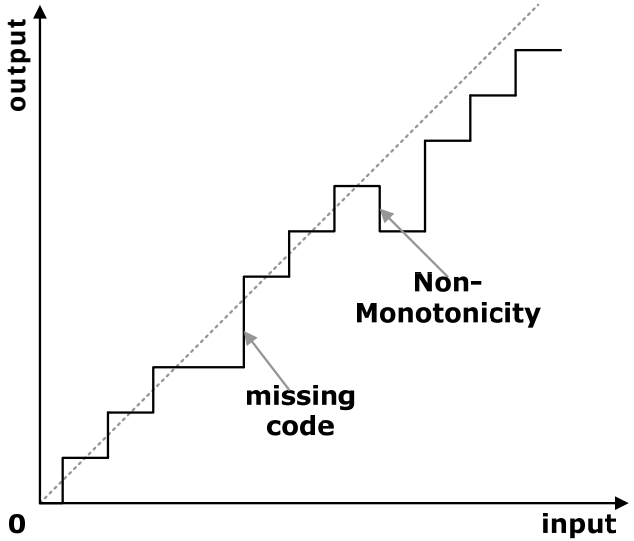
- **ADC**



- **Resolution**
- **Full Scale** $V_{FS} \equiv \frac{V_{REF}}{2^N}\left(2^N - 1\right) \approx V_{REF}$
- **LSB (Least-Significant Bit)** $1\,\mathrm{LSB} = \frac{V_{REF}}{2^N} \approx \frac{V_{FS}}{2^N}$

Static Errors – 1





- **Offset Error**
- **Gain Error**

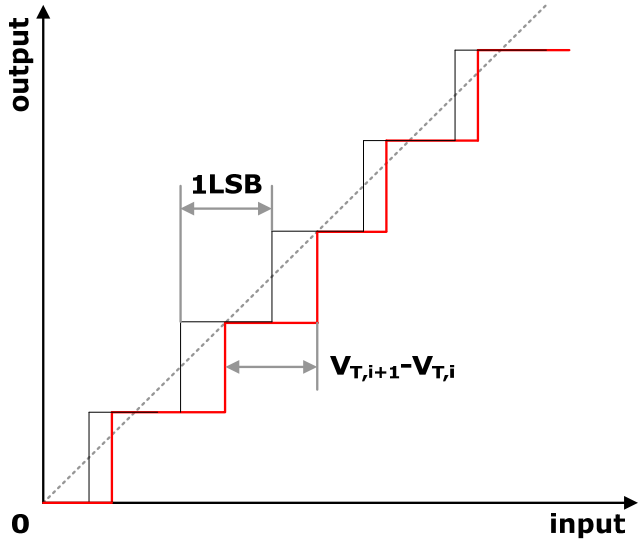
} **Linear Errors**

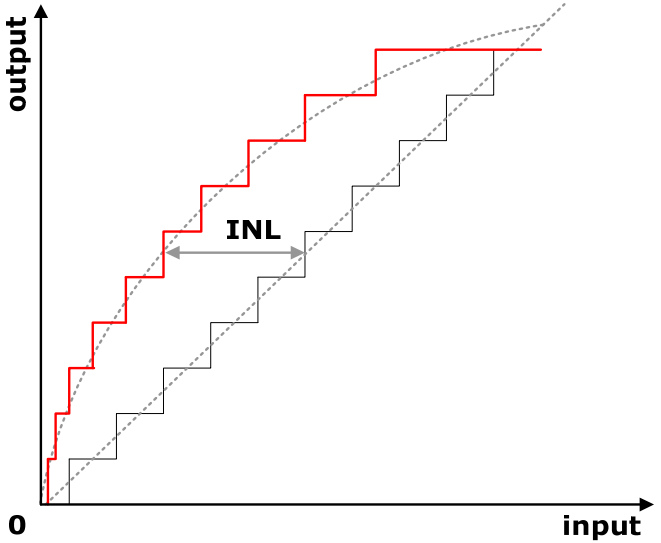
➔ Both Errors Can be Corrected

- **Non-Monotonicity**
- **Missing Codes**

➔ **Non-Linear Errors**

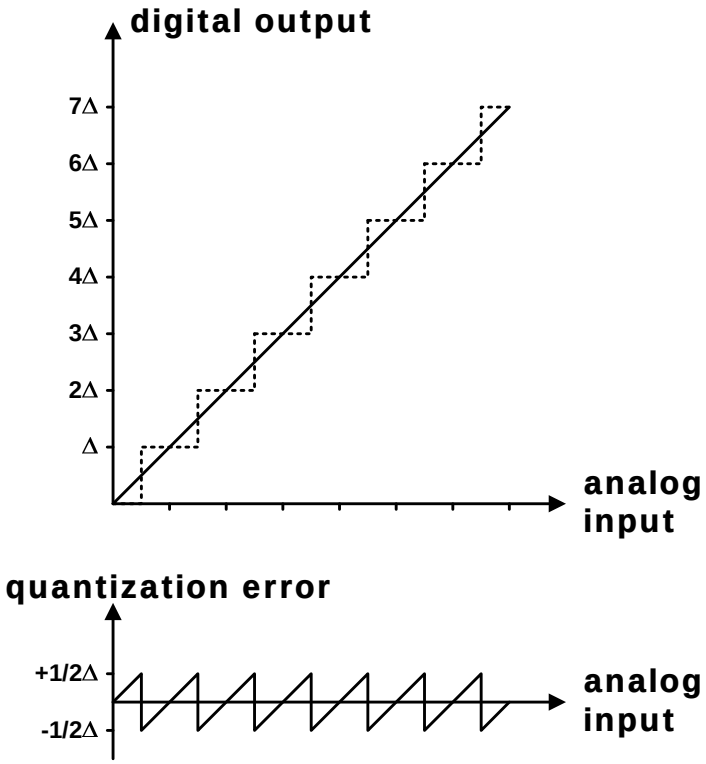
Static Errors – 2





- Differential Non-Linearity
- Integral Non-Linearity

Quantization Error (Noise)



- **LSB in N-bit Quantization**

$$\Delta = \frac{V_{FS}}{2^N - 1} \cong \frac{V_{FS}}{2^N}$$

- **Quantization Noise Power**

$$P_E = \frac{1}{\Delta}\int_{-\Delta/2}^{+\Delta/2} x^2 dx = \frac{\Delta^2}{12}$$

- **Signal Power (Sinusoidal)**

$$P_S = \frac{(V_{FS}/2)^2}{2} = \frac{(2^N \cdot \Delta)^2}{8}$$

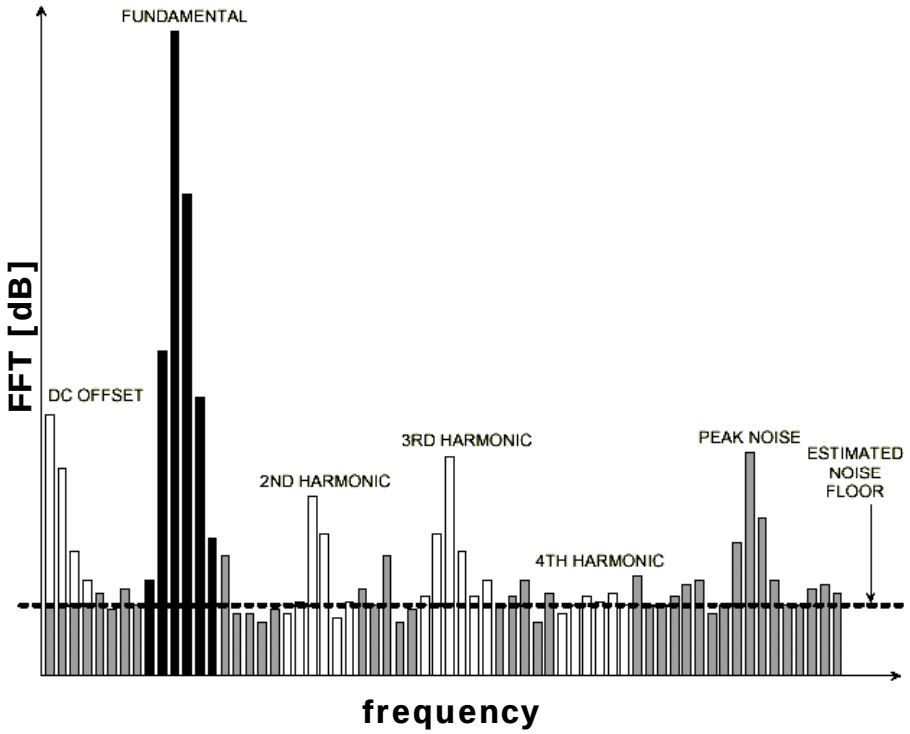
- **SNR**

$$SNR\big|_{dB} \equiv \frac{P_S}{P_E}\bigg|_{dB} = 6.02N + 1.76\,[dB]$$

1bit = 6dB of SNR

Dynamic Performance

- **Through FFT Spectrum of Output Data**



- **Signal-to-Noise Ratio**

$$\mathrm{SNR} = \frac{\mathrm{Signal}}{\mathrm{Noise}}$$

- **Total Harmonic Distortion**

$$\mathrm{THD} = \frac{\mathrm{Harmonic\ Distortions}}{\mathrm{Fundamental\ Signal}}$$

- **Signal-to-(Noise+Distortion) Ratio**

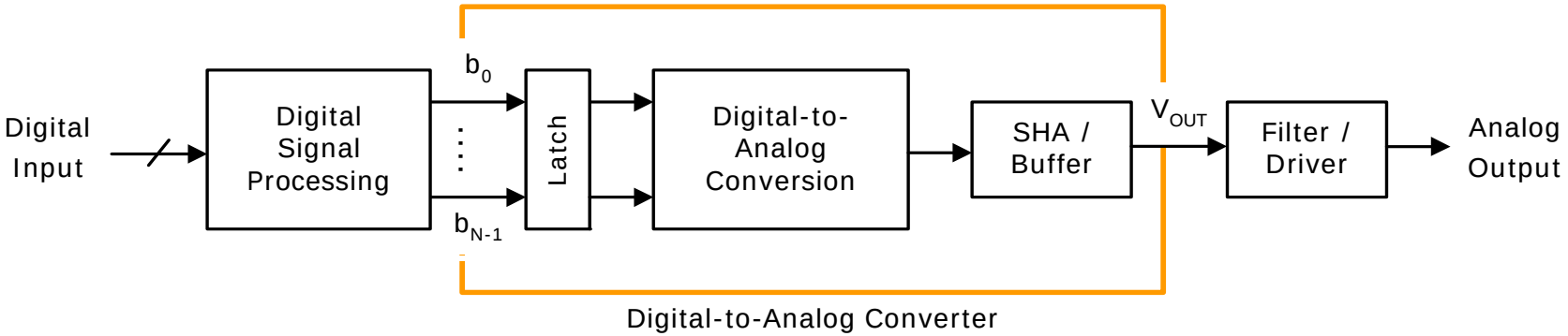
$$\mathrm{SNDR} = \frac{\mathrm{Signal}}{\mathrm{Noise} + \mathrm{Distortion}}$$

- **Effective Number of Bits**

$$\mathrm{ENOB} = \frac{\mathrm{SNDR[dB]} - 1.76}{6.02}$$

Digital-to-Analog Converter

DAC : Introduction



$$V_{OUT} = \left(\frac{b_0}{2^1} + \frac{b_1}{2^2} + \ldots + \frac{b_{N-1}}{2^N} \right) \cdot V_{REF} = D \cdot V_{REF}$$

- **Input Latch**
- **Digital-to-Analog Conversion Circuit**
- **Sample-and-Hold Amplifier or Filter**
- **Buffer or Driver**

DA Conversion Method

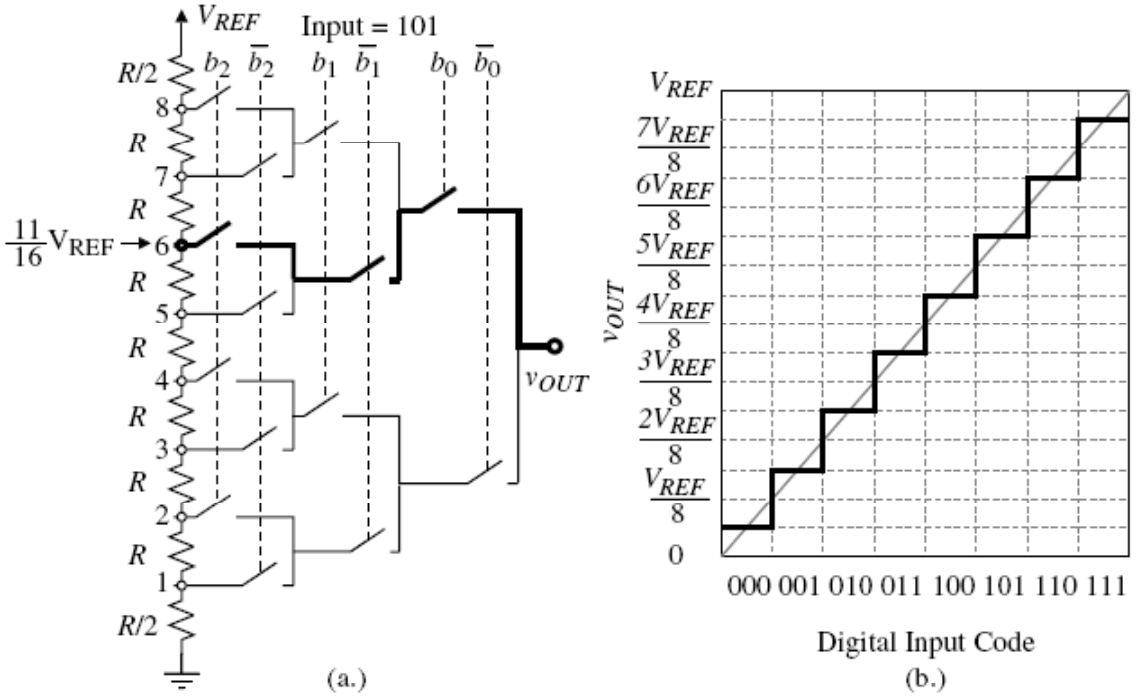
$$V_{OUT} = \left(\frac{b_0}{2^1} + \frac{b_1}{2^2} + \ldots + \frac{b_{N-1}}{2^N} \right) \cdot V_{REF} = D \cdot V_{REF}$$

- **Voltage Division Using Resistor String**
- **Binary-Weighted Elements**
  - ➔ Resistors : Current Division
  - ➔ Capacitors : Charge Division
  - ➔ Transistors : Current Division
- **Thermometer Code Implementation**
- **Segmented Architecture**
- **Serial Approach**

Voltage Division

☑ Resistor String

Resistor String 1



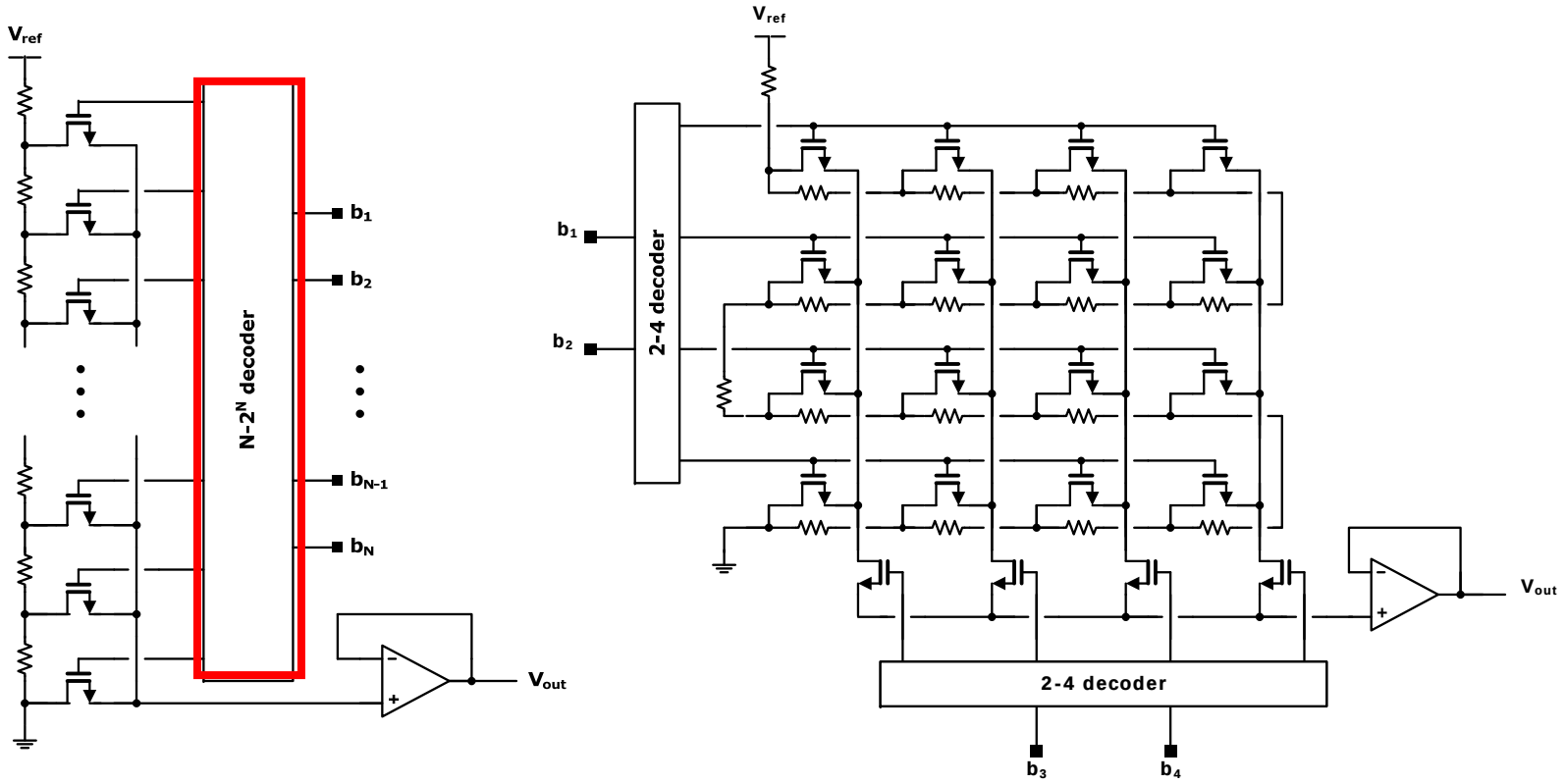
PROS

Simplicity, Guaranteed Monotonicity

CONS

Large Area, Long Switch Delay, Sensitive to Parasitic, Buffer

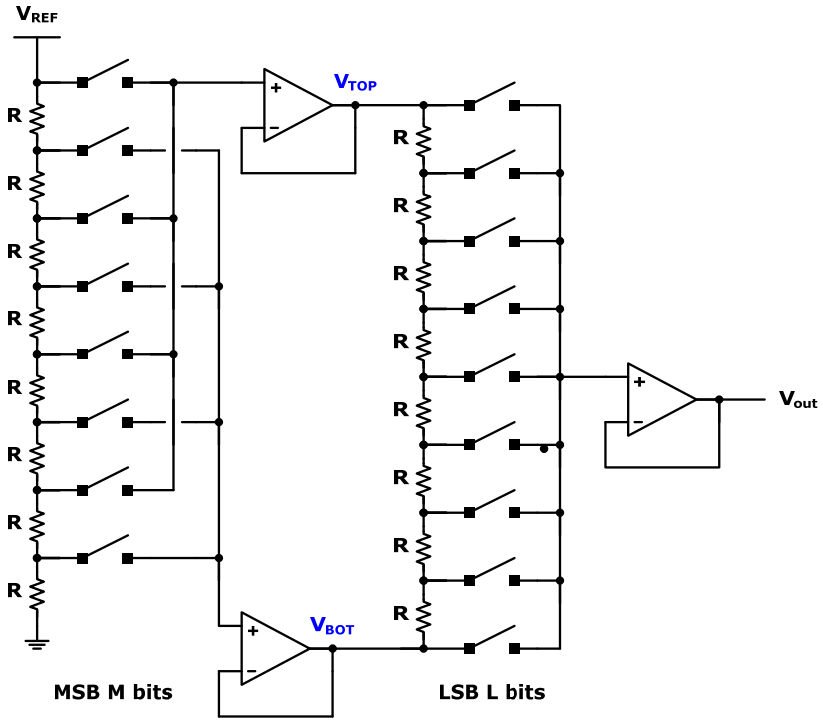
Resistor String 2



- **Using Decoder** ➔ One or Two Switches Used
- **Folded Version** ➔ Preferred for Large N
- **Cons**

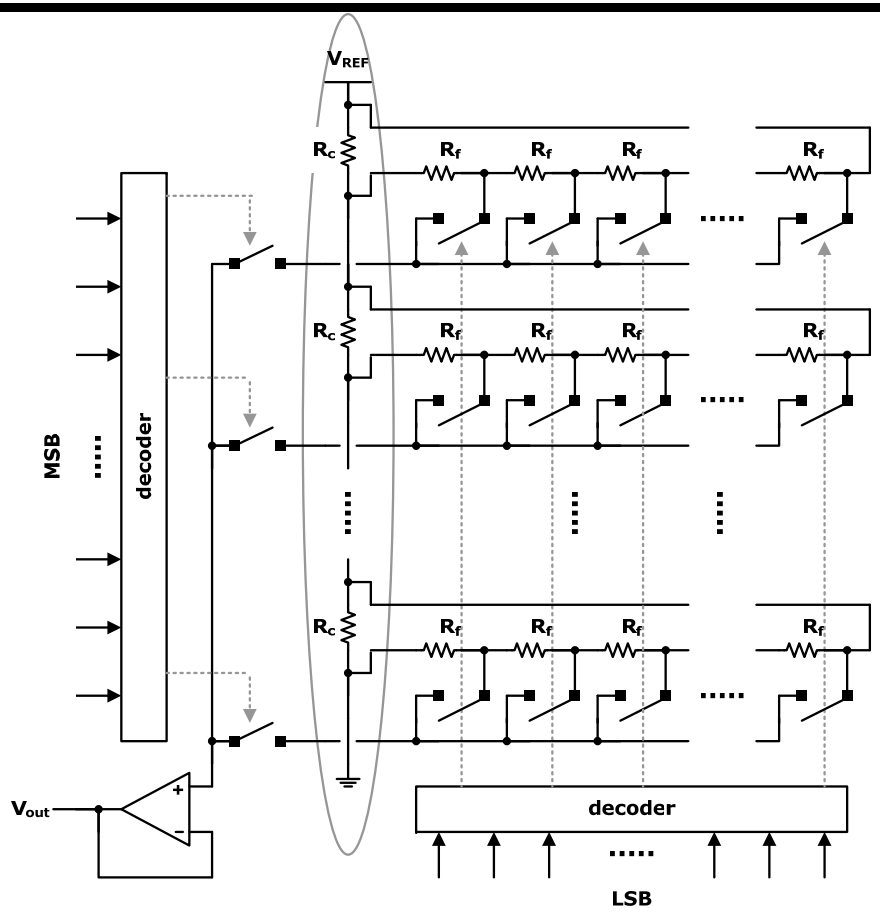
  Large Area, Sensitive to Parasitic, Buffer

Resistor String 3



- **Sub-Range :** Required Resistors 2^N ➔ $2^M + 2^L$
  - Coarse Resistor Array for MSB Processing
  - Fine Resistor Array for LSB Processing
- **Cons :** Offset Voltages of Multiple Op Amps

Resistor String 4

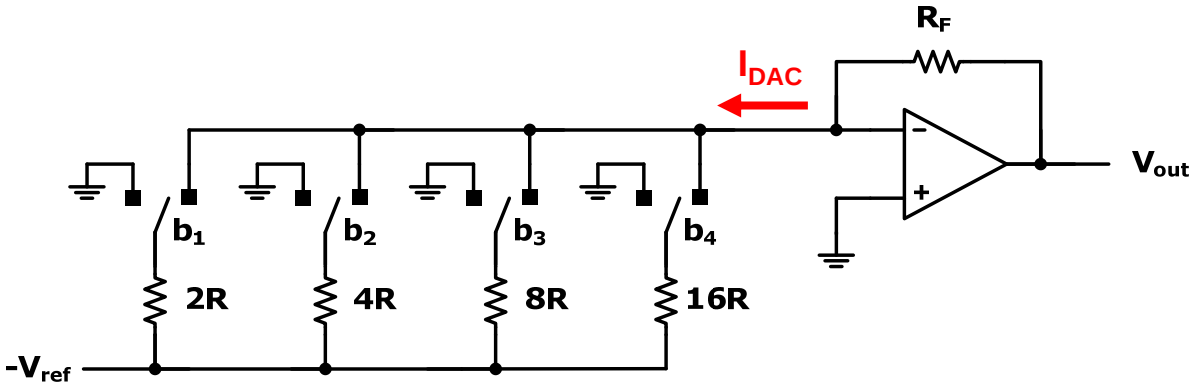


- **Inter-Mesh :** Required Resistors 2^N ➔ $2^M + M \cdot 2^L$
  - Coarse Resistor Array for MSB Processing
  - Fine Resistor Array for LSB Processing

Current Division

- ☑ Binary-Weighted Resistor
- ☑ R-2R Resistor
- ☑ Binary-Weighted MOSFET

Binary-Weighted Resistor

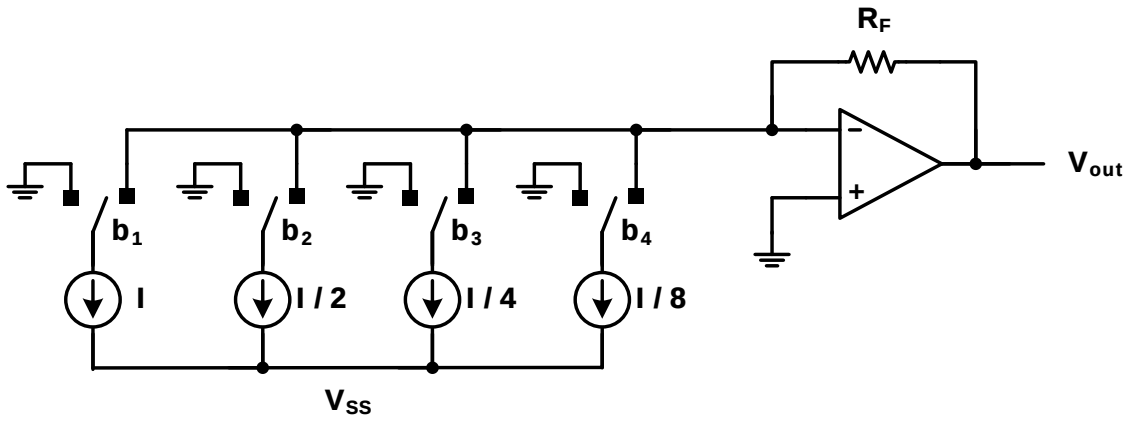


$$V_{OUT} = I_{DAC} \cdot R_F = \left[\frac{V_{REF}}{2R} b_1 + \frac{V_{REF}}{4R} b_2 + \frac{V_{REF}}{8R} b_3 + \frac{V_{REF}}{16R} b_4 \right] \cdot R_F$$

$$= \left[8 \cdot b_1 + 4 \cdot b_2 + 2 \cdot b_3 + 1 \cdot b_4 \right] \cdot \frac{R_F}{16R} \cdot V_{REF}$$

- O(2^N) Resistors Needed (Elements Wide-Spread)
- Switches Needed to be Binary-Scaled
- Monotonicity NOT Guaranteed {1000>0111 ?}

Binary-Weighted MOSFET



- Current Sources : Binary-Weighted MOSFET Current Sources
- 2(W/L) ➔ (W/L) + (W/L)
- Matching Property

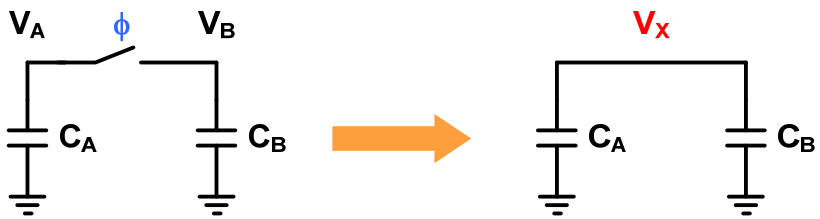
$$\frac{\Delta I}{I} = \frac{\Delta(\mu C_{ox})}{\mu C_{ox}} + \frac{\Delta W}{W} - \frac{\Delta L}{L} - \frac{2\Delta V_{TH}}{V_{GS} - V_{TH}}$$ for Long Channel

$$\frac{\Delta I}{I} = \frac{\Delta(C_{ox} v_{sat})}{C_{ox} v_{sat}} + \frac{\Delta W}{W} - \frac{\Delta V_{TH}}{V_{GS} - V_{TH}}$$ for Short Channel

Charge Division

☑ Binary-Weighted Capacitor

Charge Redistribution



Before ϕ $\quad Q_1 = C_A V_A + C_B V_B$

After ϕ $\quad Q_2 = (C_A + C_B) \cdot V_X$

$$\frac{\Delta C}{C} = \frac{\Delta W}{W} + \frac{\Delta L}{L} - \frac{\Delta t_{ox}}{t_{ox}}$$

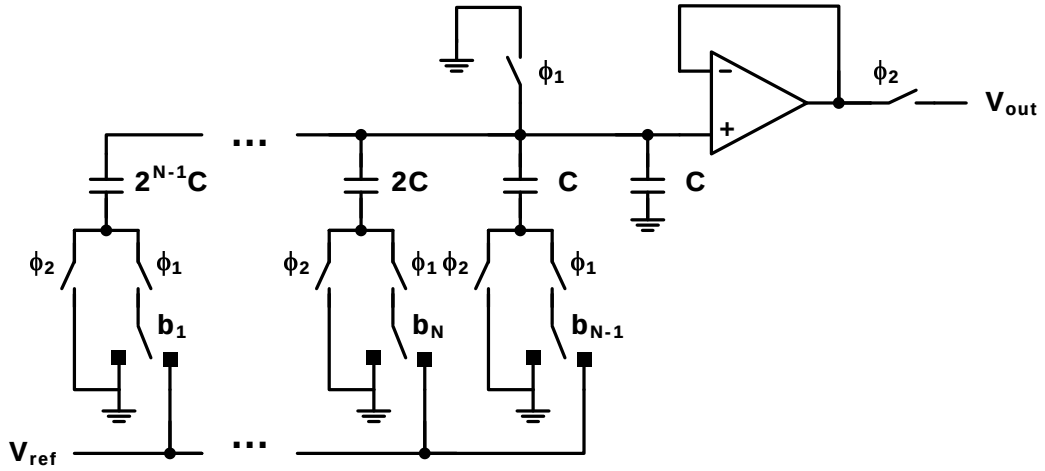
By Charge Conservation

$$Q_1 = Q_2$$

$$\therefore V_X = \frac{C_A V_A + C_B V_B}{C_A + C_B}$$

If $C_A = C_B = C$, $V_A = V_{REF}$, $V_B = 0$ ➔ $V_X = V_{REF}/2$

Charge Redistribution



- @ ϕ_1

  V_{REF} Selectively Sampled to Chosen Binary-Weighted Capacitors

- @ ϕ_2,

  V_{OUT} Evaluated by Charge-Redistribution through All Binary-Weighted Capacitors

Hybrid Approach

☑ Resistor + Capacitor

Hybrid : Resistor + Capacitor

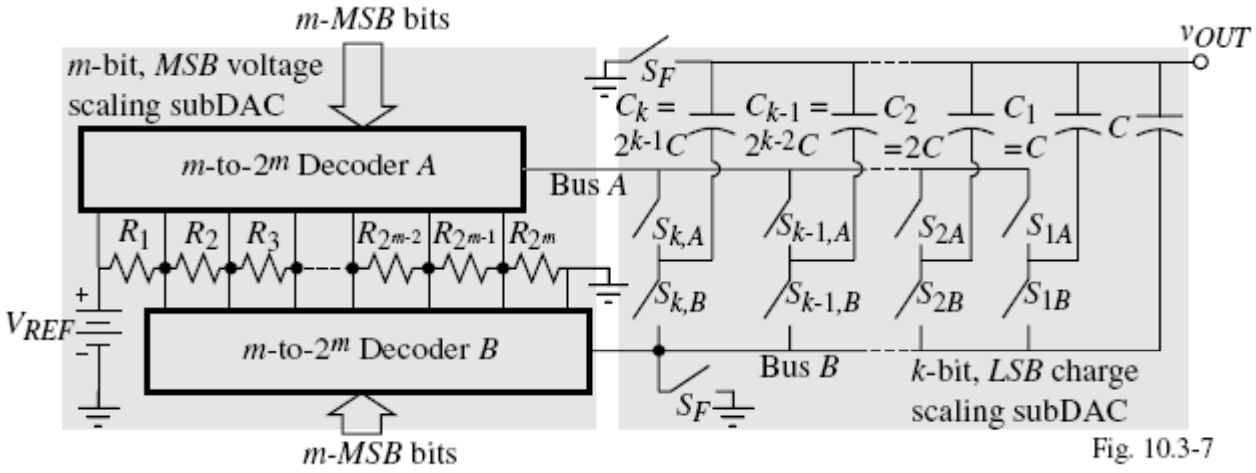


Fig. 10.3-7

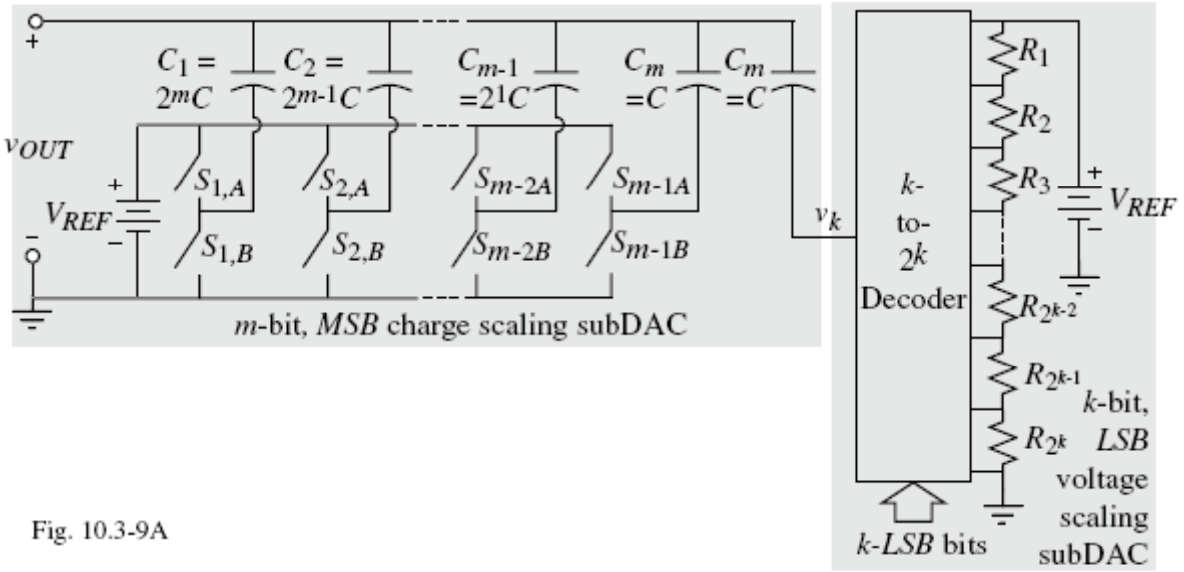
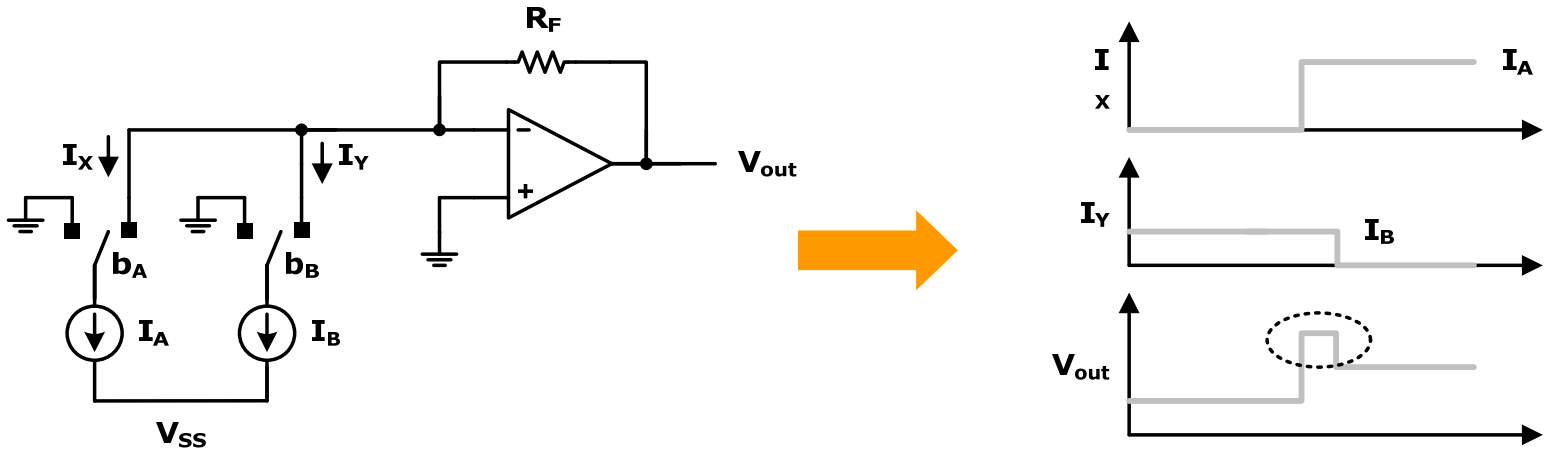


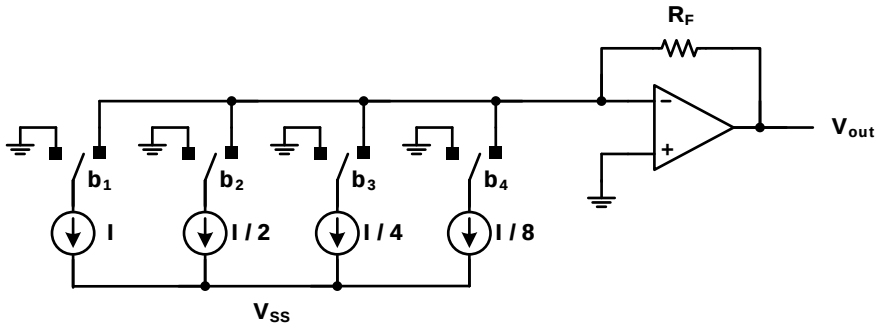
Fig. 10.3-9A

Using Thermometer Code

Glitch Problem



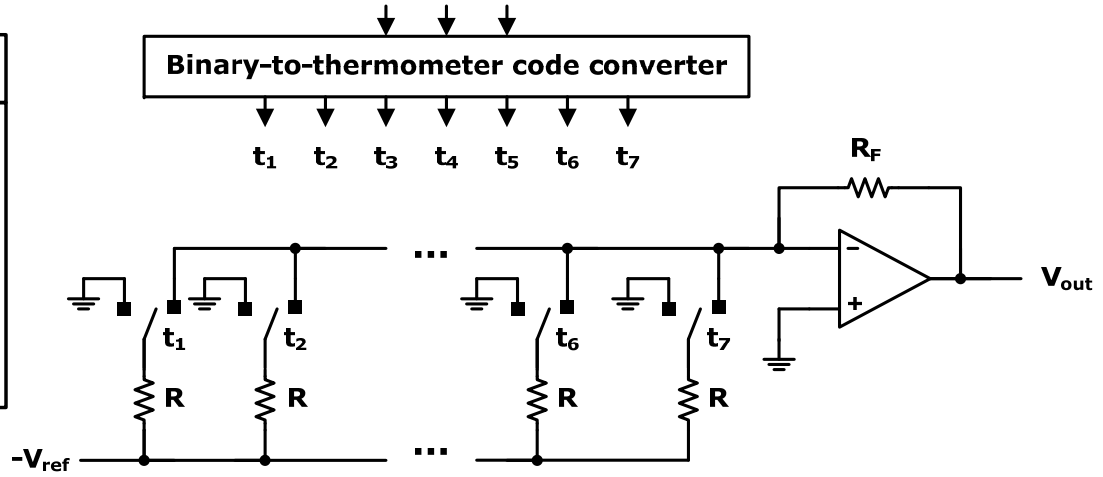
- Glitch Impulse Area
- When is the WORST case of Glitch Problem?



Glitch Solution

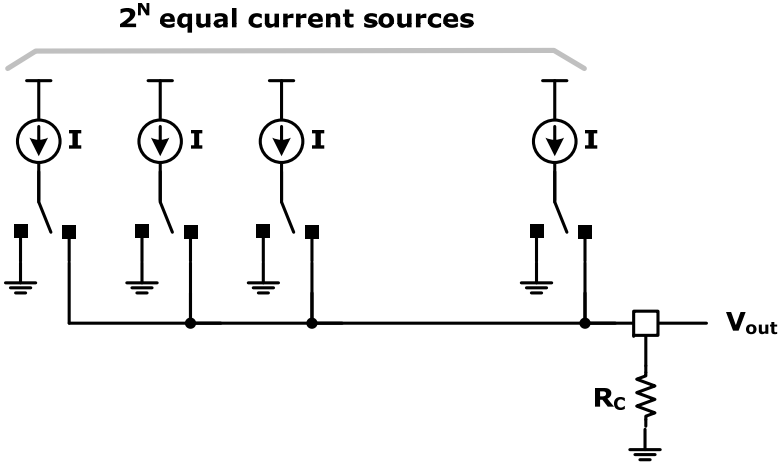
Using Thermometer Code (3-bit Example)

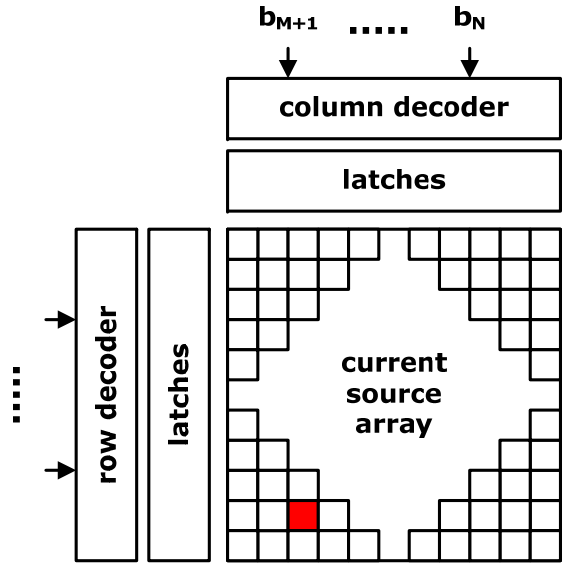
binary code b_i	thermometer code t_i
0 0 0	0 0 0 0 0 0 0
0 0 1	0 0 0 0 0 0 1
0 1 0	0 0 0 0 0 1 1
0 1 1	0 0 0 0 1 1 1
1 0 0	0 0 0 1 1 1 1
1 0 1	0 0 1 1 1 1 1
1 1 0	0 1 1 1 1 1 1
1 1 1	1 1 1 1 1 1 1



- Glitches Minimized Since Only 1 LSB Changes
- No Significance for Each Element (All Element Identical)
- Insignificant Increase in Hardware Resource

Current Mode DAC – Basic





- Currents from 2^N Current Sources Combined & Converted into Voltage (Through Usually External R_C)
- Using Thermometer Code
- 2-Dimensional Array of Current Cells
- Common-Centroid Placement
- High-Speed Operation Possible

Serial Approach

☑ Charge Stored on Capacitor

Serial DAC

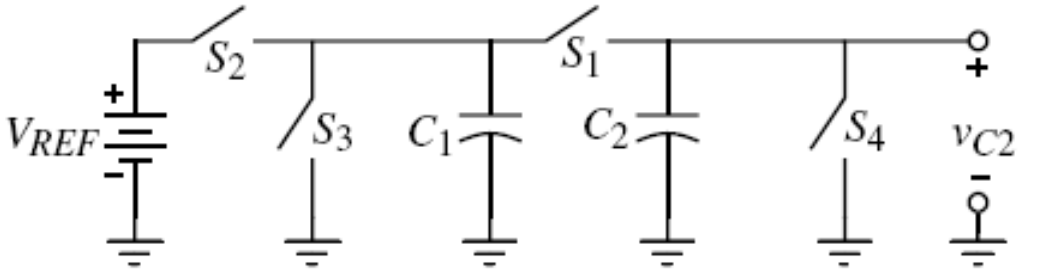


Fig. 10.4-1

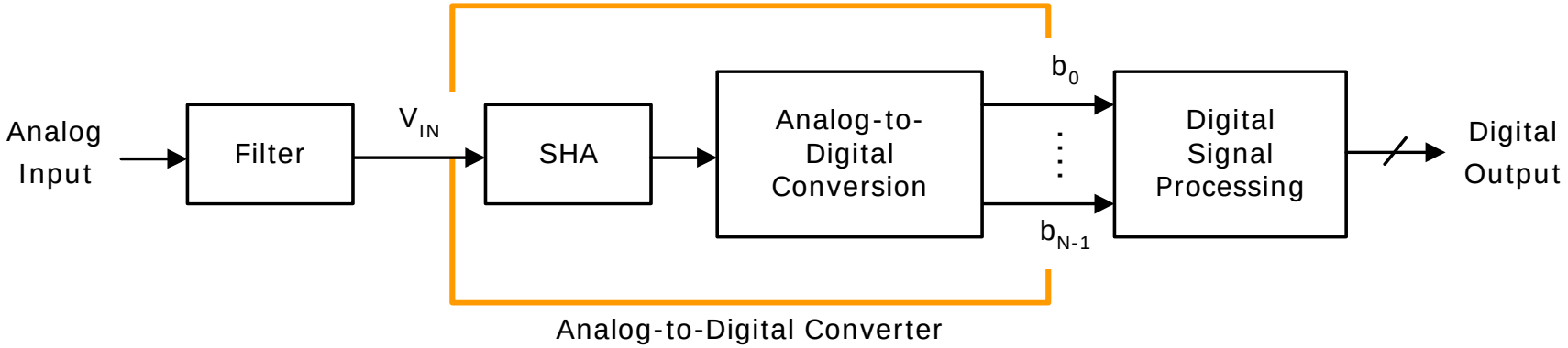
- Conversion Begins w/ LSB
- S_4 : Initialization ➔ C_2 Discharge
- S_2 : C_1 Charge to V_{REF} for $b_i = 1$

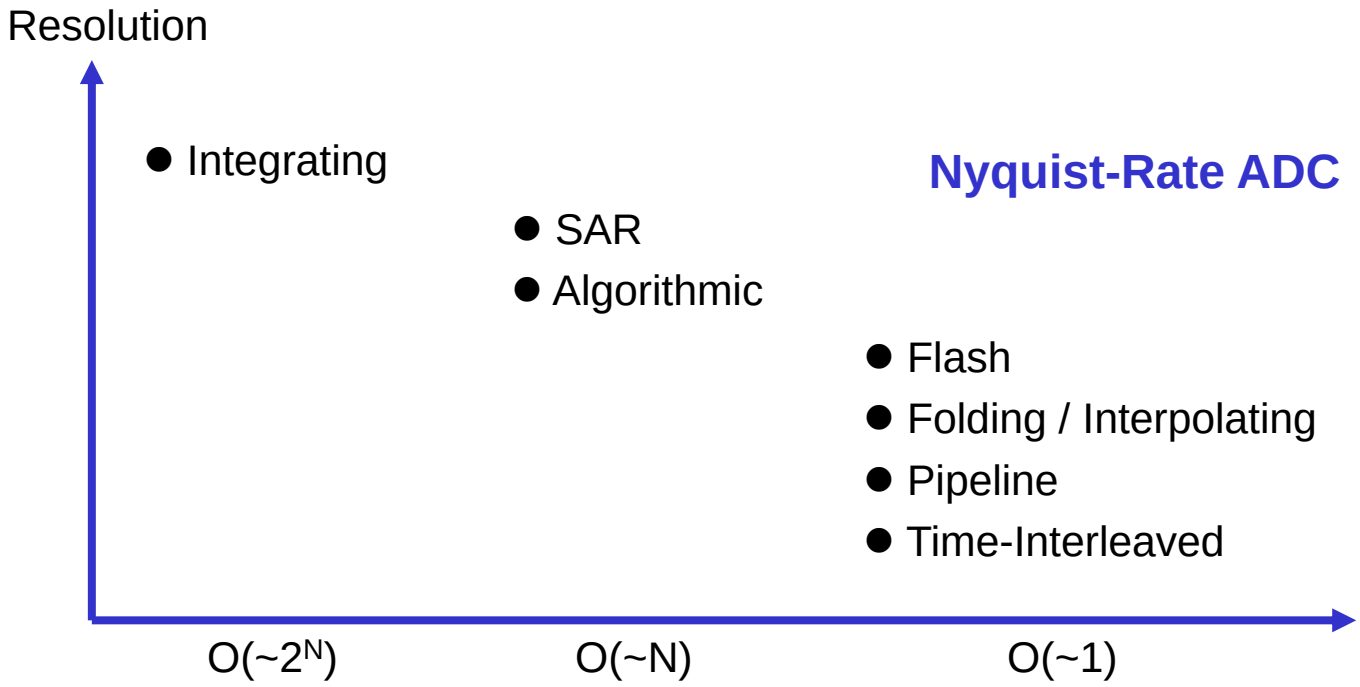
  S_3 : C_1 Discharge to 0 for $b_i = 0$
- S_1 : Redistribution of Charges into C_1+C_2
- S_2 : C_1 Charge to V_{REF} for $b_i = 1$

  S_3 : C_1 Discharge to 0 for $b_i = 0$
- S_1 : Redistribution of Charges into C_1+C_2
- And So On…

Analog-to-Digital Converter

ADC : Introduction





Why Sample-And-Hold Amplifier?

- **Input Signal**

$$V_{IN}(t) = A \cdot \sin(2\pi f_{IN} t)$$

$$\left|\frac{\Delta V_{IN}(t)}{\Delta t}\right|_{MAX} = 2\pi f_{IN} A$$

- **Conversion Time**

➔ Less Than ½LSB Change for Proper Conversion

$$T_{CONV} < \frac{(1/2)LSB}{\left|\frac{\Delta V_{IN}}{\Delta t}\right|_{MAX}} = \frac{\frac{1}{2}\cdot\frac{2A}{2^N}}{2\pi f_{IN} A} = \frac{1}{2\pi f_{IN} 2^N}$$

- **Maximum Conversion Rate**

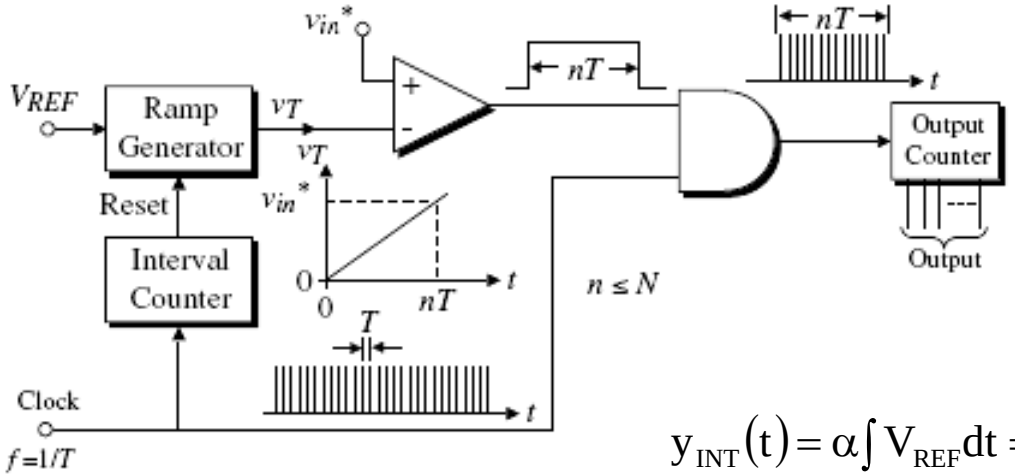
$$f_{CONV} > 2\pi f_{IN,MAX} 2^N$$

(Example) 16-bit Audio Signal ➔ f_{conv} = 8.23GHz!

Low-Speed ADC

☑ Integrating ADC

Integrating ADC



$$y_{INT}(t) = \alpha \int V_{REF} dt = \alpha V_{REF} \cdot t$$

Integrator Output

- Measure T_{DATA} When $V_{INT}=V_{IN}$

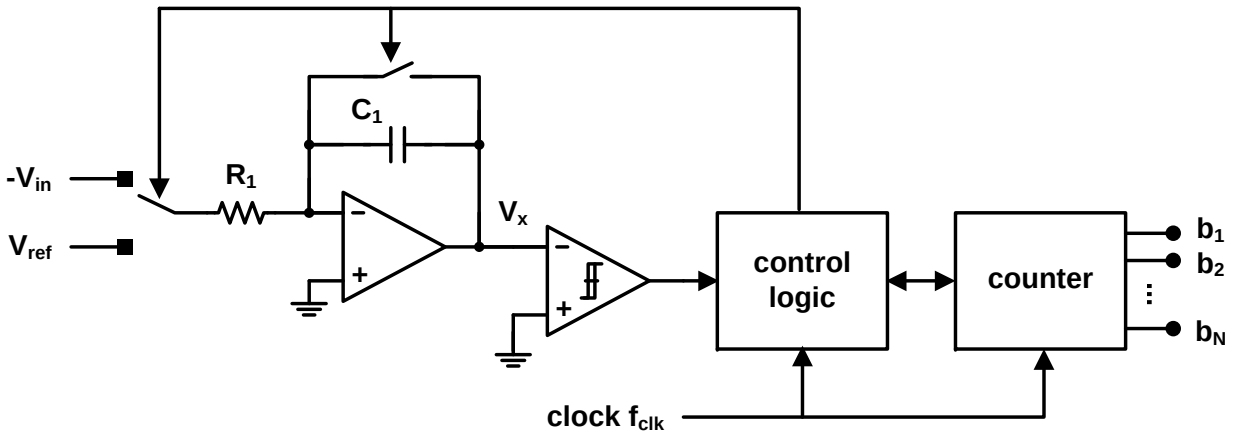
$$y_{INT}(t) = \alpha V_{REF} \cdot T_{DATA} = V_{IN} \rightarrow T_{DATA} = \frac{V_{IN}}{\alpha V_{REF}}$$

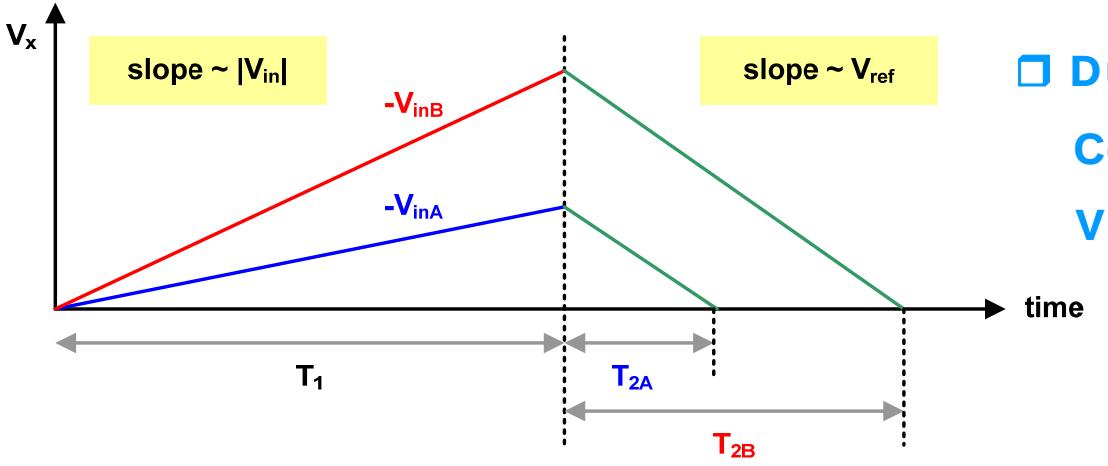
- Measurement Done by Counter : T_{DATA} ➔ D_{OUT}

Problems

- Integrator Usually Made by Active-RC Integrator : α ~ 1/RC

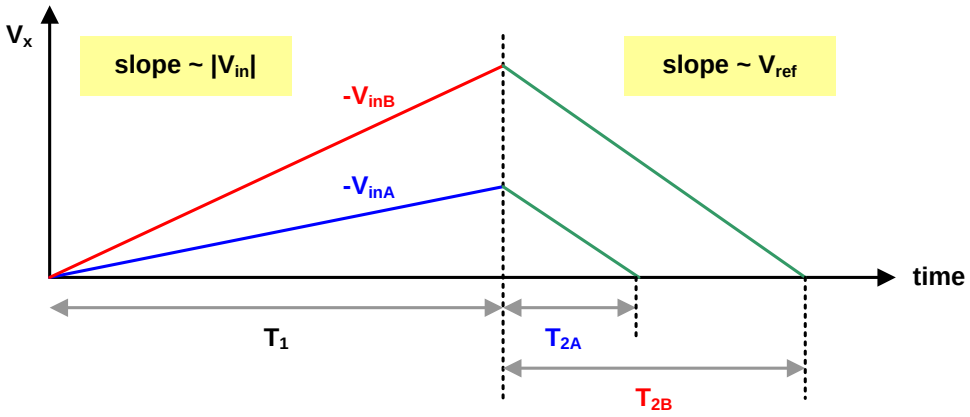
Dual-Slope Integrating ADC – 1





❒ Dual Integration for Compensating RC Variations

Dual-Slope Integrating ADC – 2



- During T_1

$$y_{INT1} = \frac{1}{RC}\int V_{IN}dt = \frac{1}{RC}V_{INA}T_1$$

- During T_{2A}

$$y_{INT2} = \frac{1}{RC}\int V_{REF}dt = \frac{1}{RC}V_{REF}T_{2A}$$

- When Conversion Completed, $y_{INT1} = y_{INT2}$

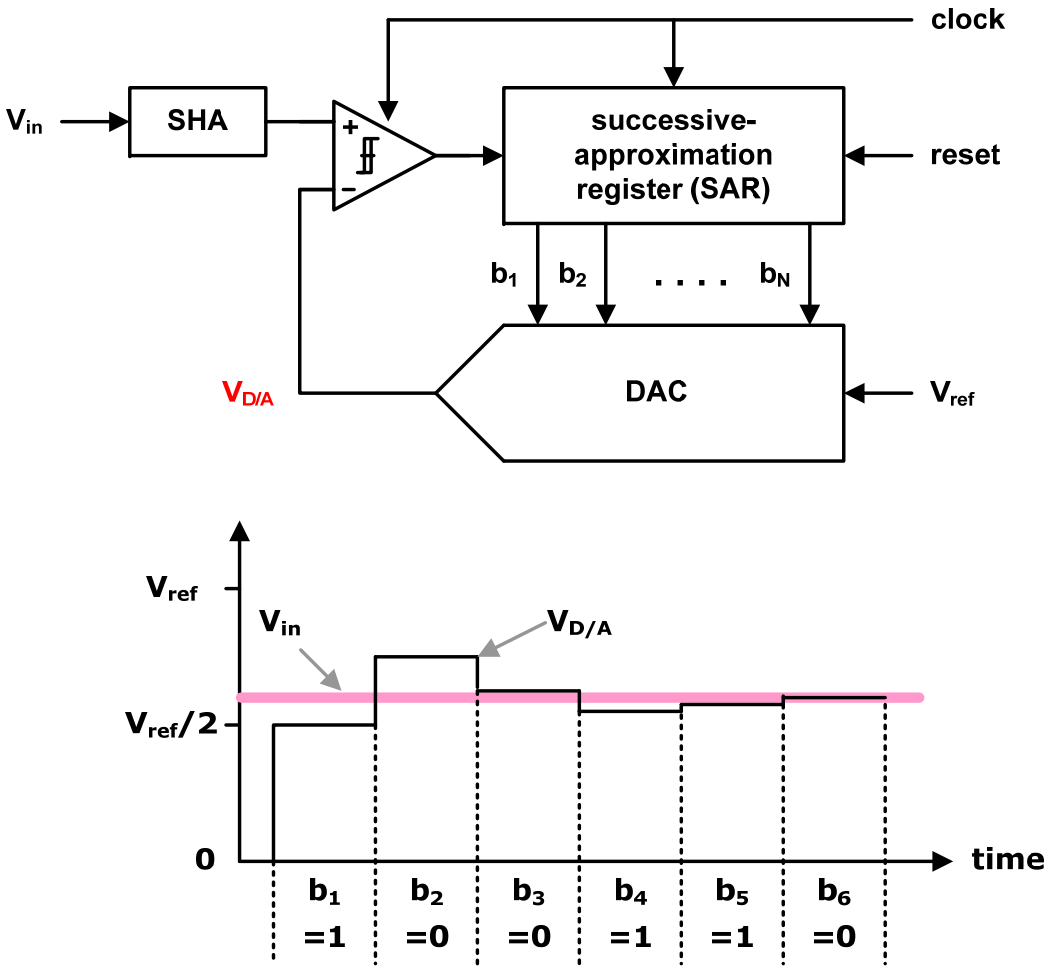
$$T_{I2A} = \frac{V_{IN}}{V_{REF}}T_1$$

- Simple Hardware & Low Power Dissipation
- Conversion Cycles ~ $2 \cdot 2^N$

Medium-Speed ADC

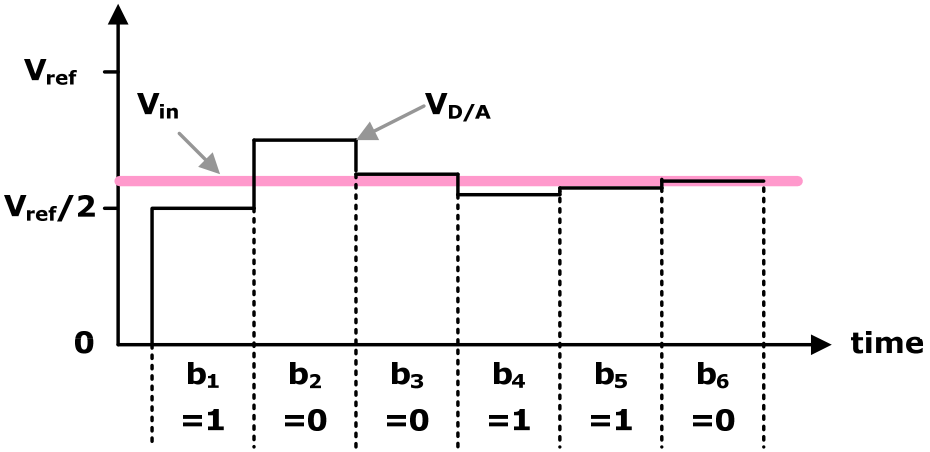
- ☑ SAR ADC
- ☑ Cyclic (Algorithmic) ADC

SAR ADC – 1



❒ Successive Approximation Register (SAR) Control Logic

SAR ADC – 2



$$V_{D/A}(1) = V_{ref}/2$$

$$V_{D/A}(i) = V_{D/A}(i-1) - (-1)^{b_{i-1}} 2^{-i} V_{ref}$$

$$V_{in} > V_{D/A}(i) \Rightarrow b_i = 1$$

- DAC Output $V_{D/A}$ ➔ V_{IN}
- DAC Implementation
  (Ex. Charge-Redistribution DAC)
- SAR Control Logic Circuit
- Conversion Cycles ~ N

❒ V_{IN} = 38.1 (V_{REF}=64)

❶ $V_{D/A(1)}$ = 32 ➔ b_1=1

❷ $V_{D/A(2)}$ = 32+16 ➔ b_2=0

❸ $V_{D/A(3)}$ = 48-8 ➔ b_3=0

❹ $V_{D/A(4)}$ = 40-4 ➔ b_4=1

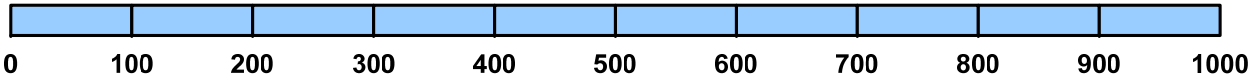
❺ $V_{D/A(5)}$ = 36+2 ➔ b_5=1

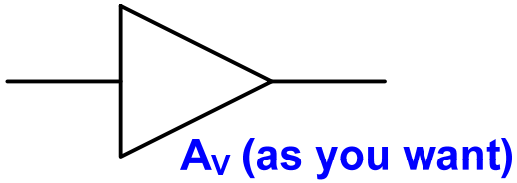
❻ $V_{D/A(6)}$ = 38+1 ➔ b_6=0

Cyclic ADC – 1

❒ **Residue : V_{IN} – (V_{ADC}→V_{DAC})**

If You ONLY Have as Follows,





How Can You Measure the Value of 548?

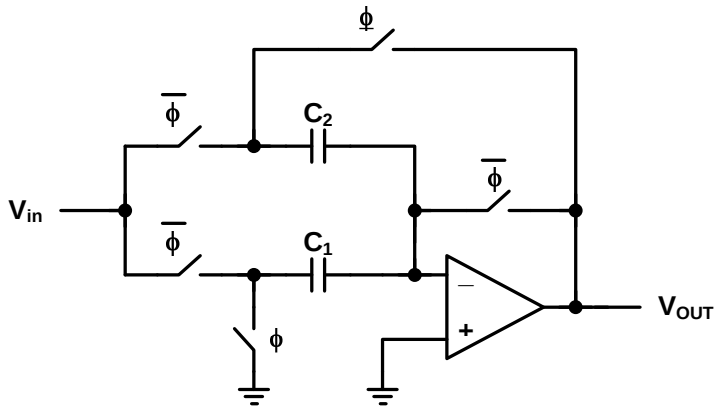
548

Cyclic ADC – 2

- Operations

$$V_{S/H}(1) = V_{in}$$
$$V_{S/H}(i) = 2V_{S/H}(i-1) + (-1)^{b_{i-1}} V_{ref}$$
$$V_{S/H}(i) > 0 \Rightarrow b_i = 1$$

- x2 Amplifier



$$\frac{V_{OUT}}{V_{IN}} = \frac{C_1 + C_2}{C_2}$$

- Conversion Cycles ~ N

❒ V_{IN} = +25.2 ($\pm V_{REF} = \pm 32$)

❶ $V_{S/H(1)}$ = +25.2 ➔ $b_1 = 1$

❷ $V_{S/H(2)}$ = 50.4-32 ➔ $b_2 = 1$

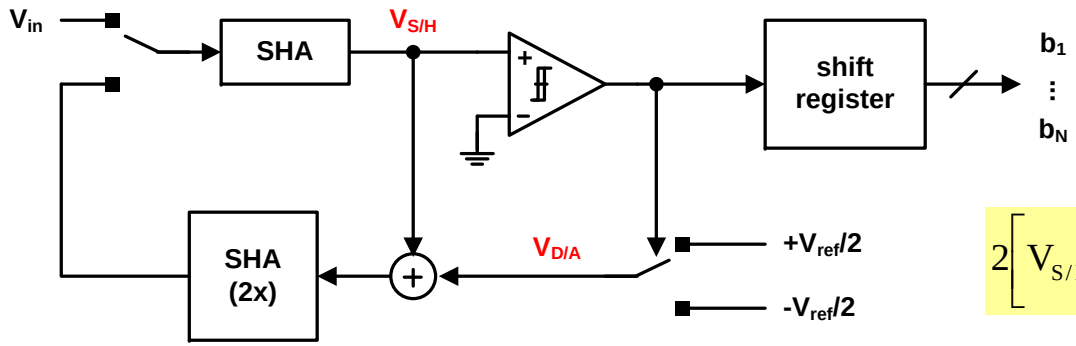
❸ $V_{S/H(3)}$ = 36.8-32 ➔ $b_3 = 1$

❹ $V_{S/H(4)}$ = 9.6-32 ➔ $b_4 = 0$

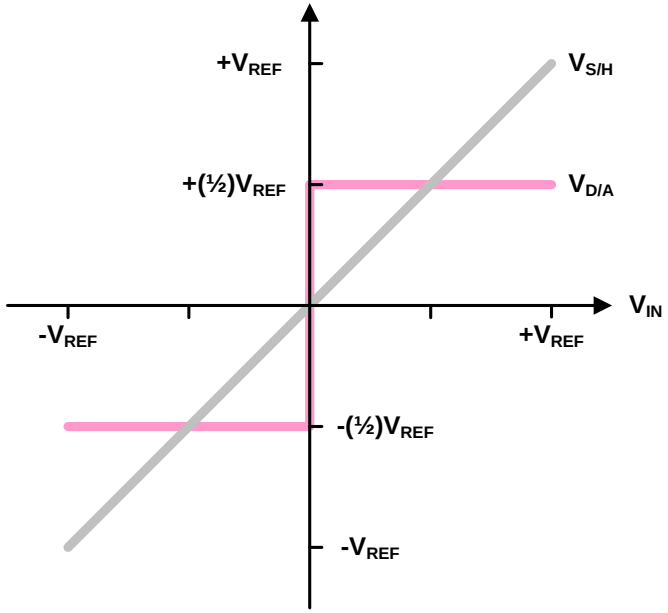
❺ $V_{D/A(5)}$ = -44.8+32 ➔ $b_5 = 0$

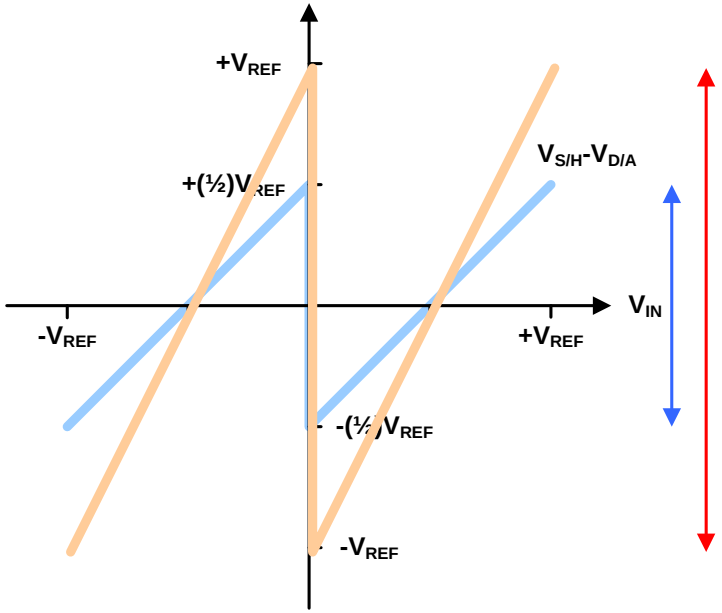
❻ $V_{D/A(6)}$ = -25.6+32 ➔ $b_6 = 1$

Cyclic ADC – 3



$$2\left[V_{S/H} \pm \frac{V_{REF}}{2}\right] = 2V_{S/H} \pm V_{REF}$$

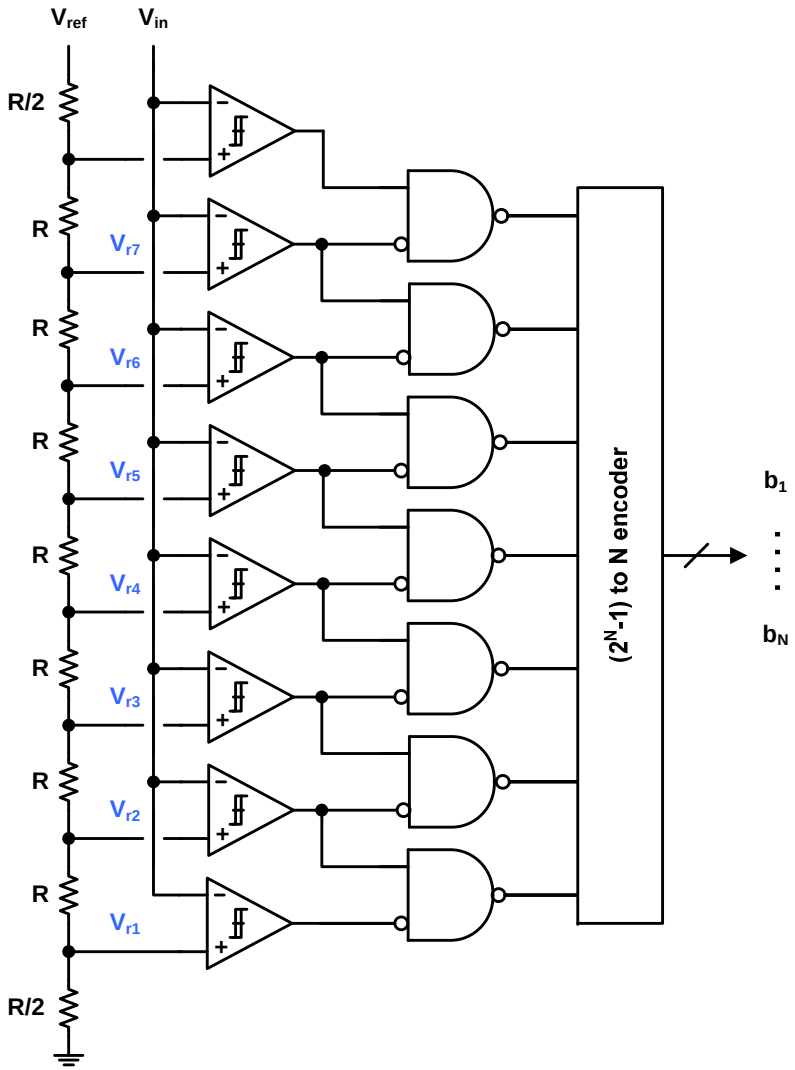




High-Speed ADC

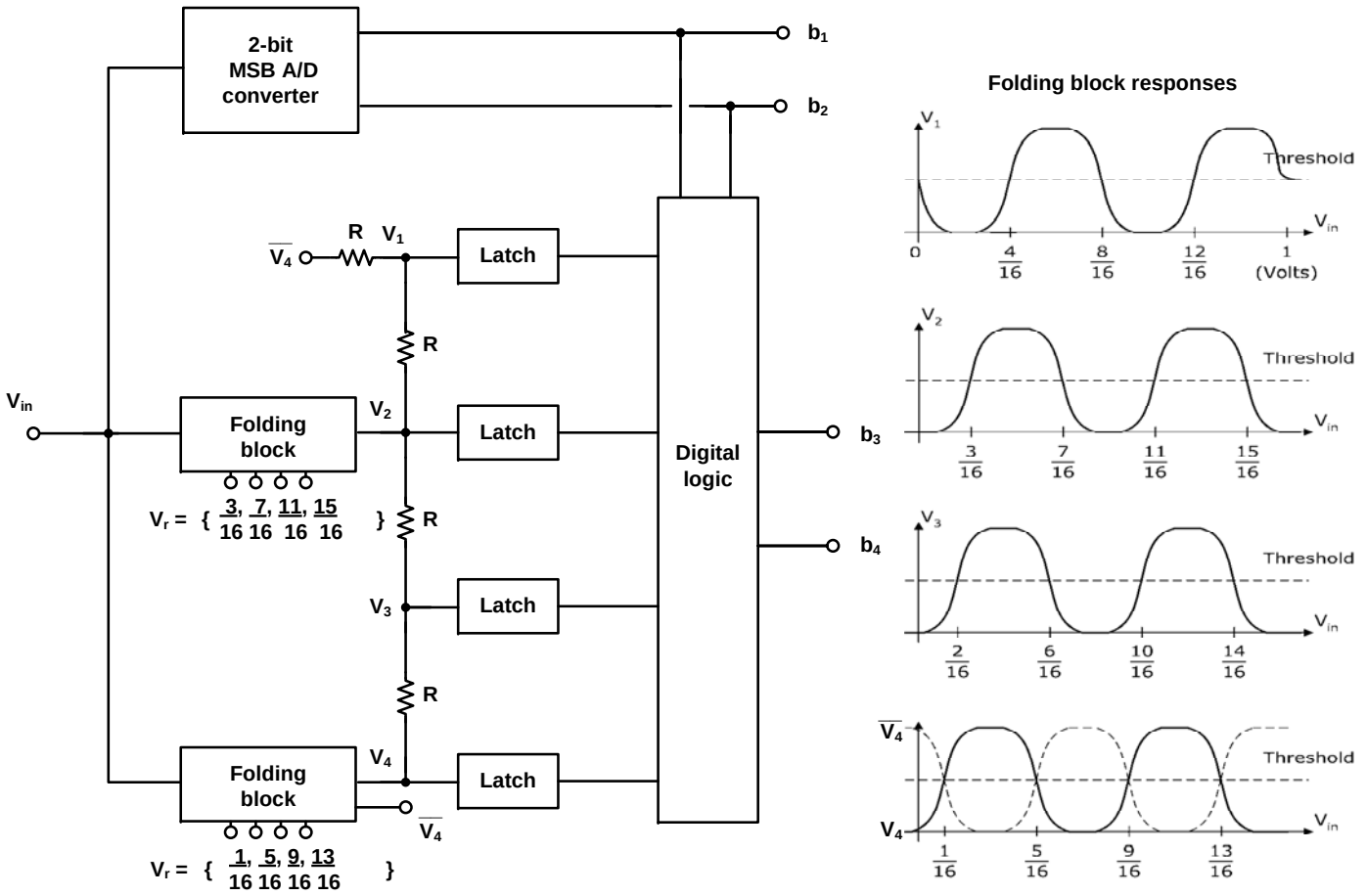
- ☑ Flash ADC
- ☑ Interpolating ADC
- ☑ Folding ADC
- ☑ Pipeline ADC
- ☑ Time-Interleaved ADC

Flash ADC



- Full Utilization of Parallelism
- Large Hardware ~ $O(2^N)$
- Conversion Cycle ~ 1

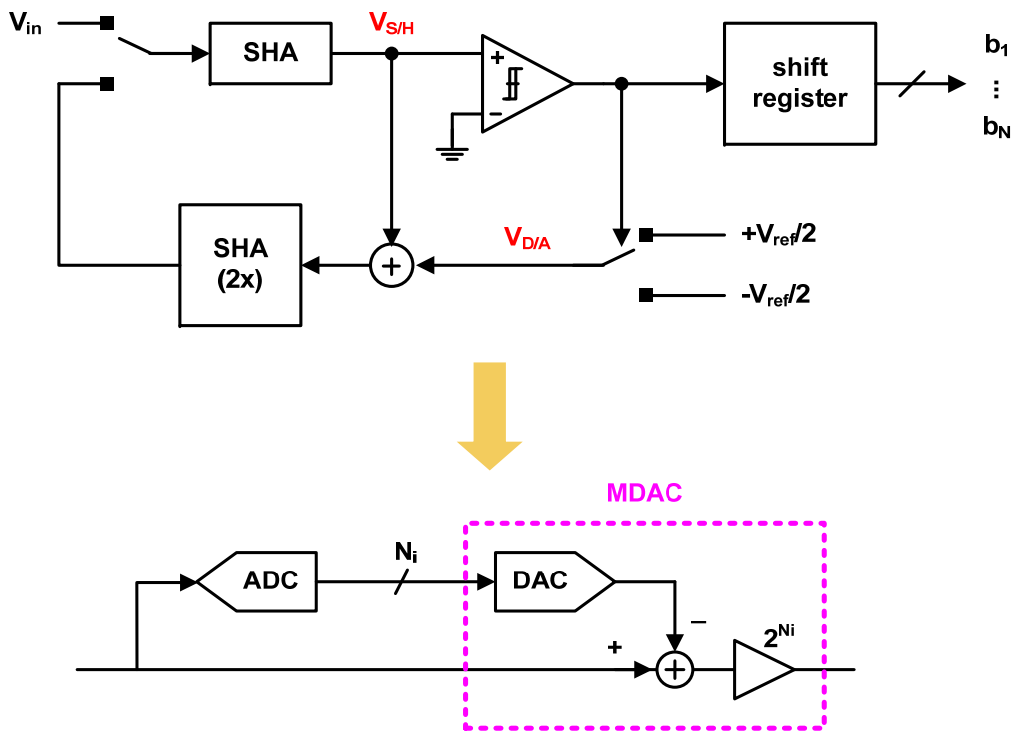
Folding / Interpolating ADC



- Number of Folding Blocks Reduced by Interpolation Technique

Pipeline ADC – 1

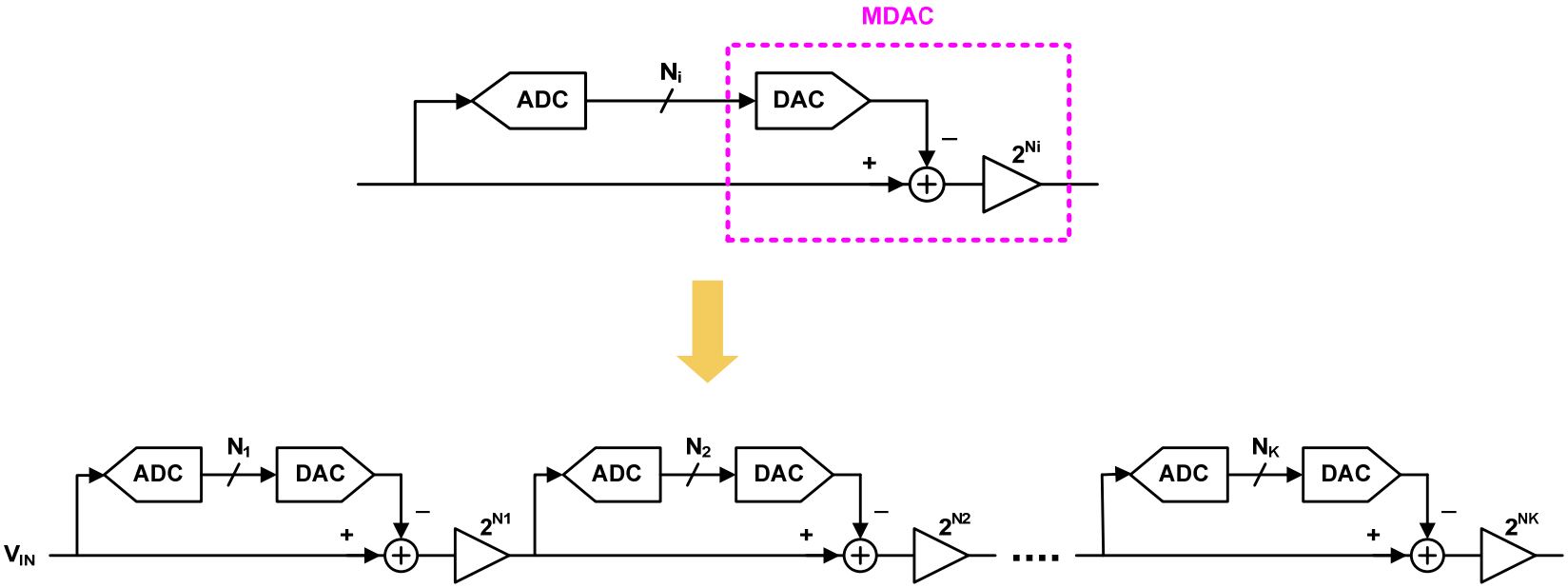
Generalizing Residue Signal Processing From Cyclic ADC



- Residue = V_{ADC} - V_{DAC}
- Amplification for Processing w/ Reduced-Resolution Blocks

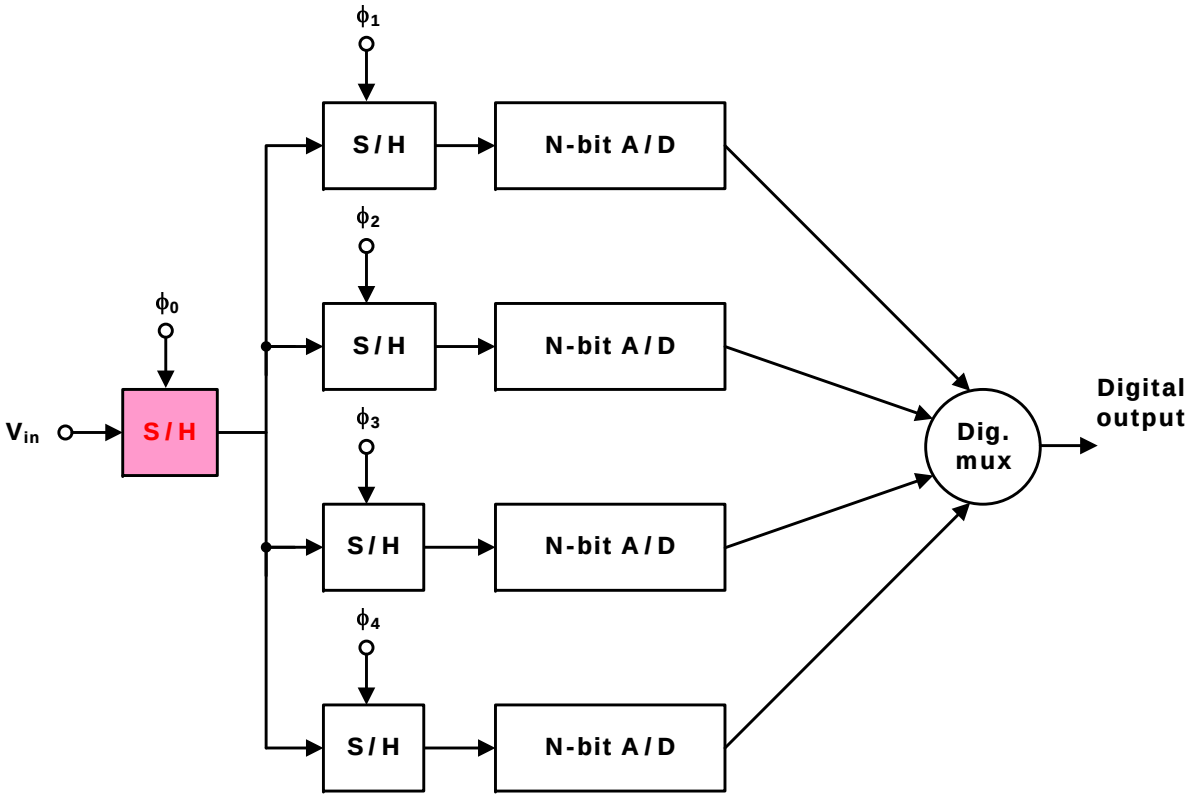
Pipeline ADC – 2

To Increase Conversion Speed : Serial ➔ Pipeline



- Total Number of Bits N = $N_1+N_2+\ldots+N_K$
- Latency ~ K Cycles (Number of Stages)
- $T_{CONVERSION}$ ~ 1 Cycle

Time-Interleaved ADC



- Used for VERY High-Speed ADC Implementation
- Input SHA Critical : $\phi_0 = 4 \times \phi_i$
- Mismatch Problems to be Resolved Between Channels

Q & A