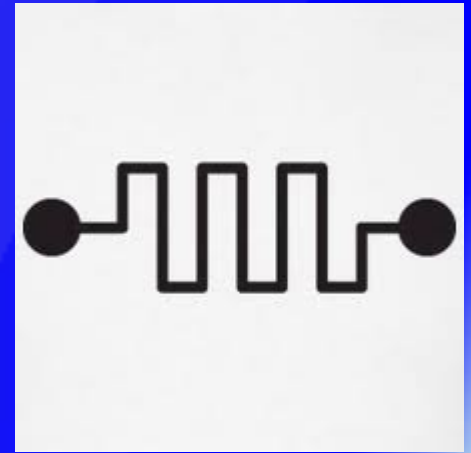


Mentriston

- finding missing links -



School of Electrical & Electronics engineering.

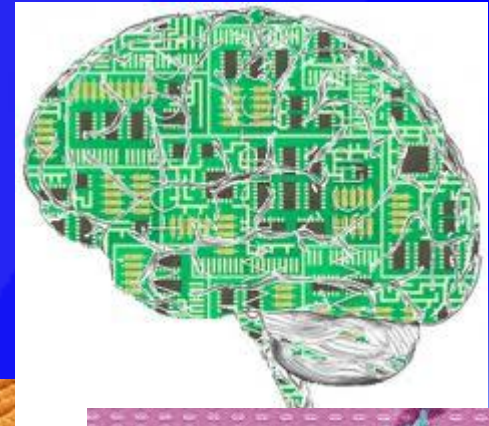
Yonsei University.

Undergraduate 8th semester

Ki Joon, Chang

CONTENTS

1. Getting started
2. What's the meaning of missing links?
3. The properties of Memristance
4. Characteristics
5. TiOx based Memristor
6. Future of Memristor
7. Question session



Part 1. Getting Started

Getting Started



Have you seen this picture before?



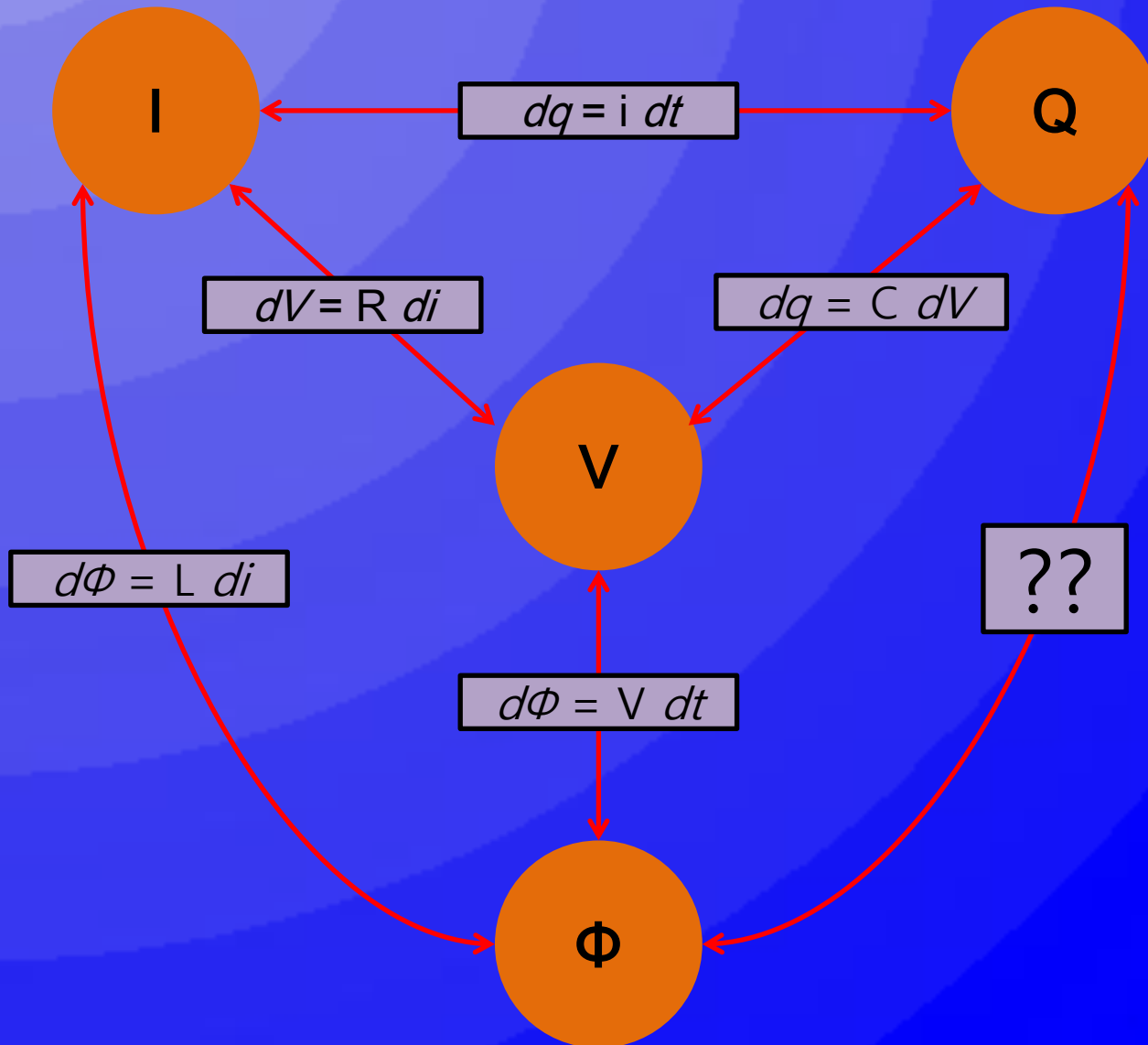
Sung-Mo "Steve" Kang
Chancellor / Professor, School of Engineering, UC Merced

Research Area

- * Low power/large-scale integration design
- * Mixed-signal, mixed-technology integrated systems
- * Modeling and simulation of semiconductor devices and circuits
- * High-speed optoelectronic circuits and optical network systems
- * Nanoelectronics

Part 2. What's the meaning of missing link?

What's the meaning of missing link?

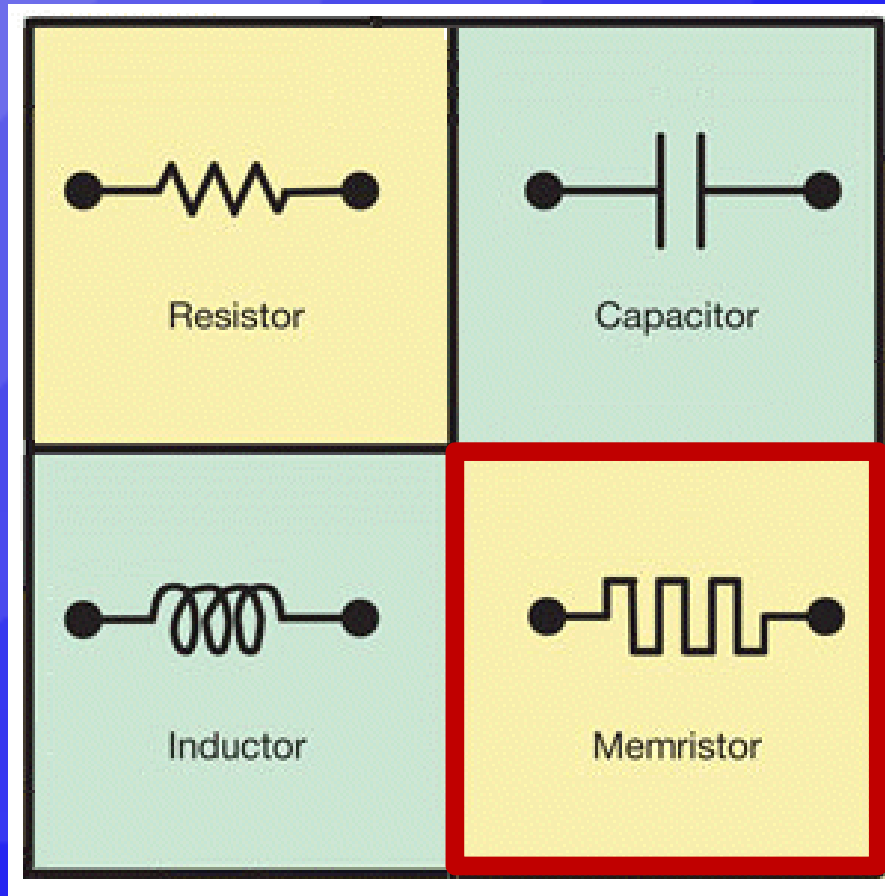


New property!

Memristance (M),
Memory + resistance
 $d\Phi = M dq$

What's the meaning of missing link?

Ohm
(1827)



Von Kleist
(1745)

Faraday
(1831)

L. Chua
(1971)

Part 3. The properties of Memristance

The properties of Memristance

- a. Memristor theory was formulated by Leon Chua in a 1971 paper.
- b. 'Φ' means magnetic flux leakage (not magnetic field!)

$$M(q) = d\Phi / dq$$
$$M(q(t)) = d\Phi/dt / dq/dt = V / I \quad (\text{Ohm's Law})$$

- c. By this derivation, the new property 'M' stands for '**charge dependent resistance**'.
- d. Operation as a switch (similar operation to CMOS)

$$P_{switch}(t) = I(t)^2 M(q(t)) = V^2 \int_{Q_{off}}^{Q_{on}} \frac{dt}{M(q(t))} =$$
$$V^2 \int_{Q_{off}}^{Q_{on}} \frac{dq}{I(q)M(q)} = V^2 \int_{Q_{off}}^{Q_{on}} \frac{dq}{V(q)} = V\Delta Q = V(Q_{on} - Q_{off})$$

- e. Unlike the transistor, the final state of the Memristor in terms of charge **does not depend on bias voltage**. (Non-volatile characteristic)

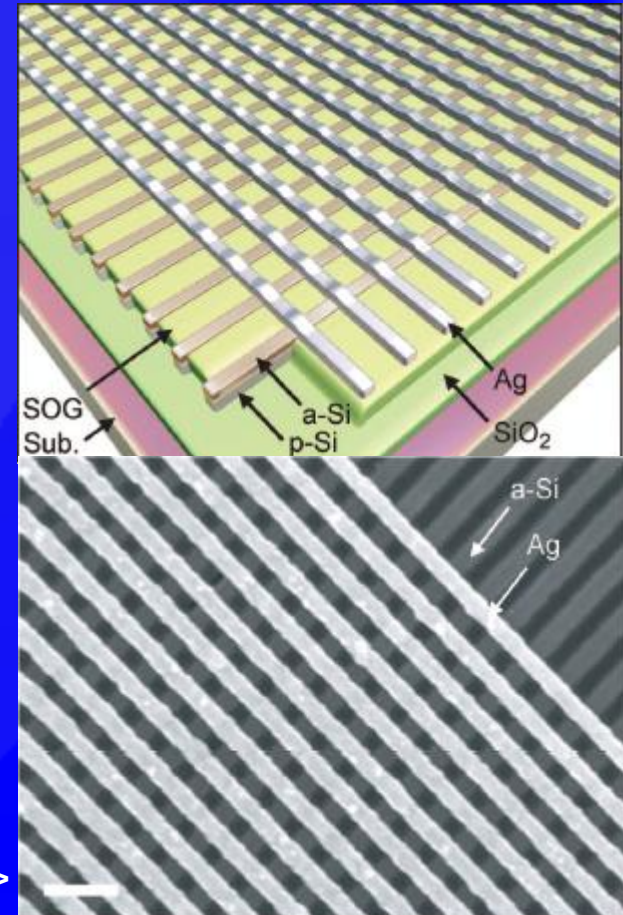
Part 4. Characteristics

- a. Candidates for universal memory
- b. Migration to the “Non-volatile architecture”
 - Reduce power consumption from Flip-Flops (FFs) and registers
 - Reduce transmission power loss
 - Reduce static power – in idle mode (no need to refresh)
- c. Memristor can resolve conventional limitations of the past NV architecture.
 - Block access requirements
 - Long read/write times
 - Access penalty for multilevel cell
- d. Many experts expect that Memristive devices will be rival against 20-nm CMOS technology.
- e. TiO_x (Titanium Oxide) or Amorphous-Si are most famous.

Characteristics

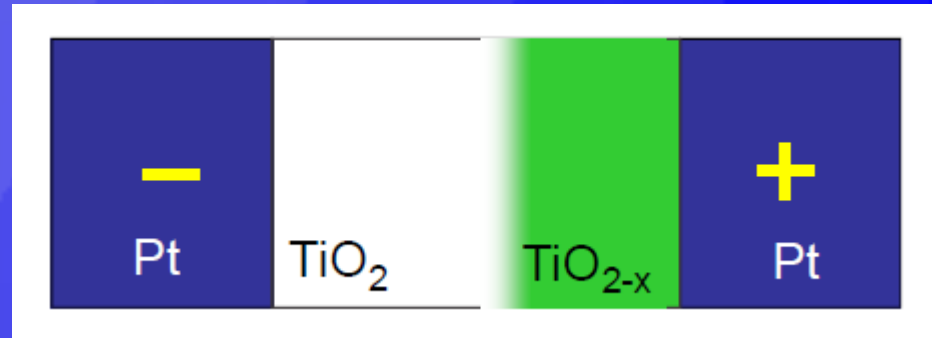
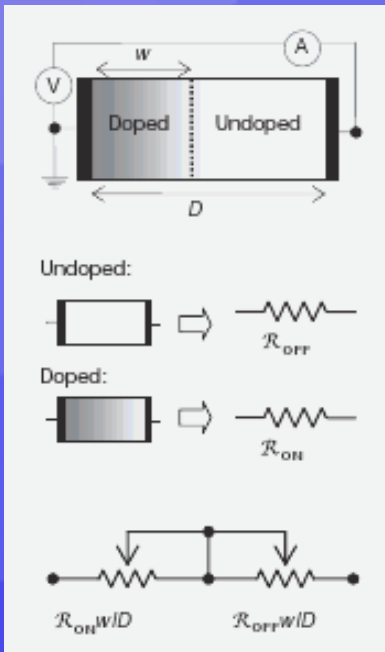
- Less Write/Erase/Read speed (less than 10ns)
- Data holding time is approximately, 7 year
NV characteristic, Resistive RAM
- ON/OFF ratio (>1000000)
In CMOS case, on/off ratio is less than 1000,
better characteristic!
- Scaling potential = less than 30nm
- Endurance >100000 cycles

200nm p-Si Memristor nanowire, Crossbar junctions >>

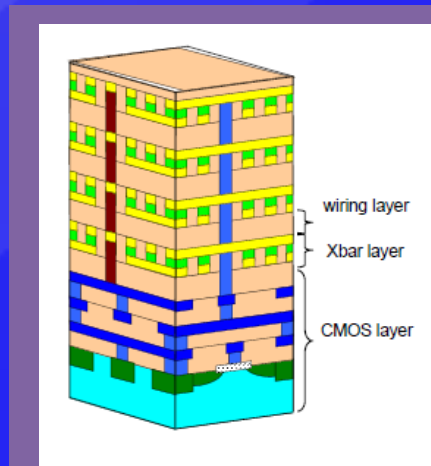
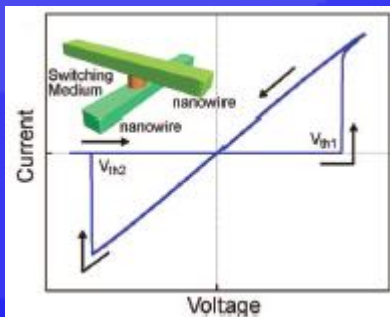


Part 5. TiO_x based Memristor

TiOx based Memristor



When a positive bias voltage is applied to electrode 2, the positively charged O vacancies drift to the left, which narrows the tunneling gap.



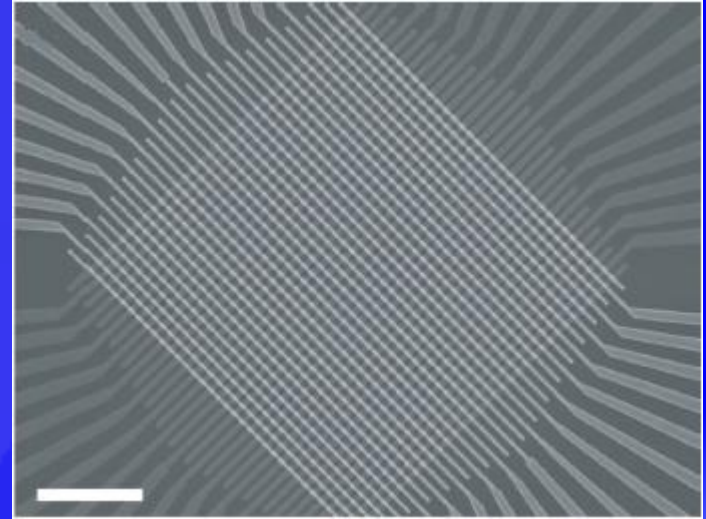
See this Video,
(brief explanation)

Figure. Stacked structure of TiOx Memristor

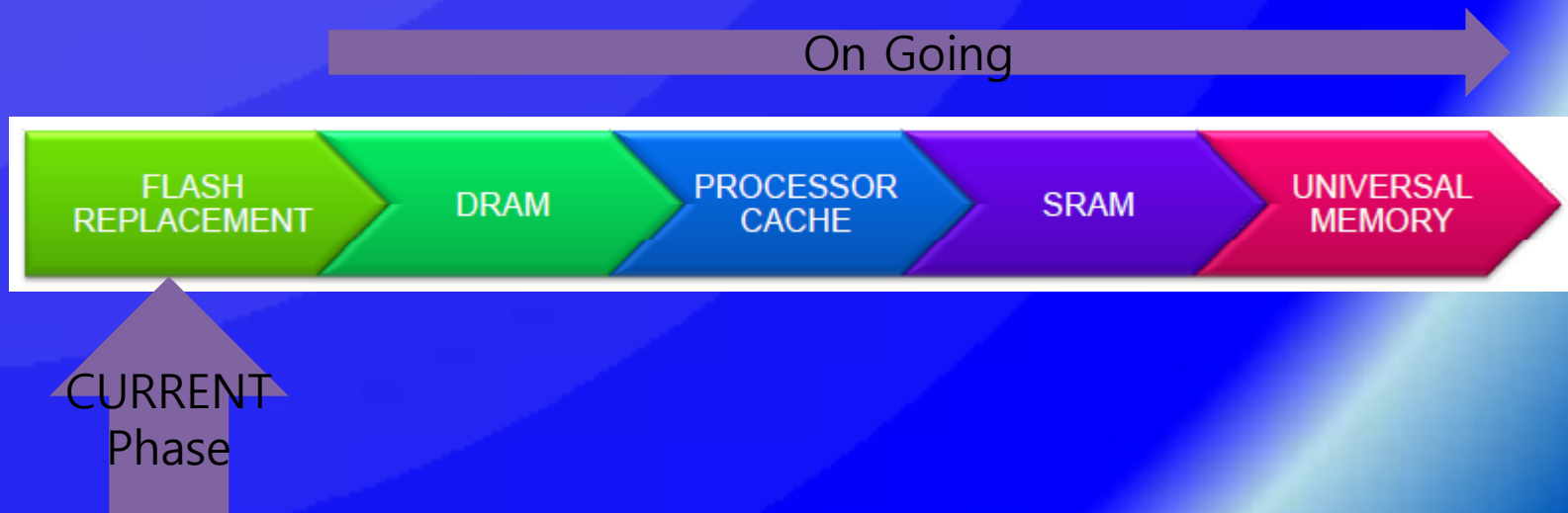
Part 6. Future of the Memristor

Future of the Memristor

- Migration to other phase
- CMOS - Memristor Hybrid circuit
- Another application (Neuromorphic etc.)



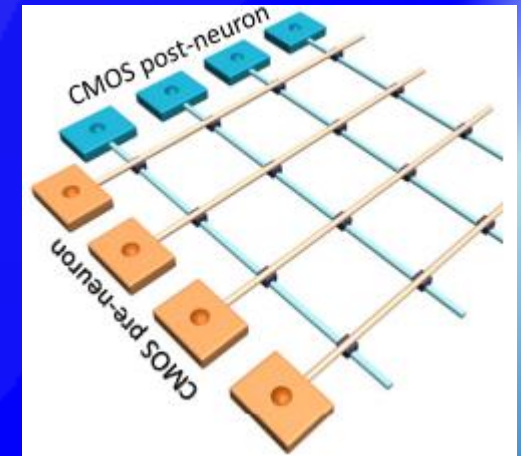
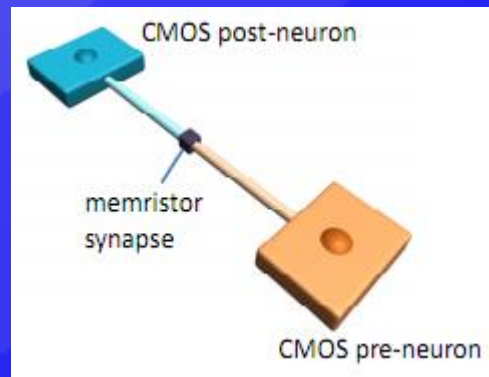
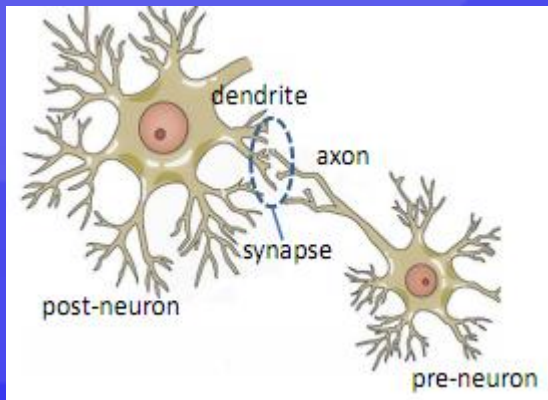
<SEM image of a 1 kb crossbar array, based on the Ag/a-Si/Ni Memristor structure. Scale bar: 2 μm >



Future of the Memristor

a. Bio-inspired super-computing systems : DARPA SyNAPSE project (2008)

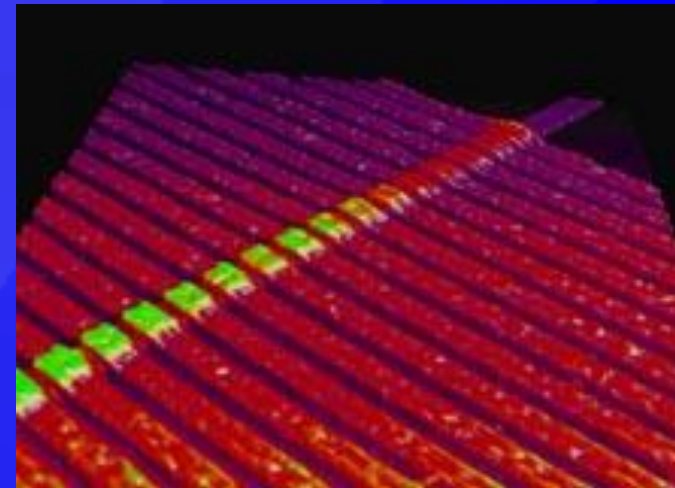
b. A synapse is essentially a two-terminal device and bears striking resemblance to the memristor.



<Schematic of a Hybrid CMOS neuron/memristor synapse circuit approach for neuromorphic systems>

Future of the Memristor

c. HP(Hewlett – Peckard) collaborate with Hynix Semiconductor to bring in the first commercial Memristive device to the market.(31 Aug, 2010, until 2013)



<This colorized atomic-force microscopy image shows 17 TiO_x memristors. The circuit elements, shown in green, are formed at the crossroads of metal nanowires. - HP>

Part 7. Q & A session

Thank you!
Any Questions?