Challenges in Nanoscale Devices and Breakthroughs

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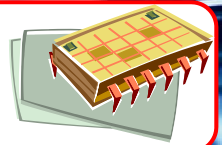
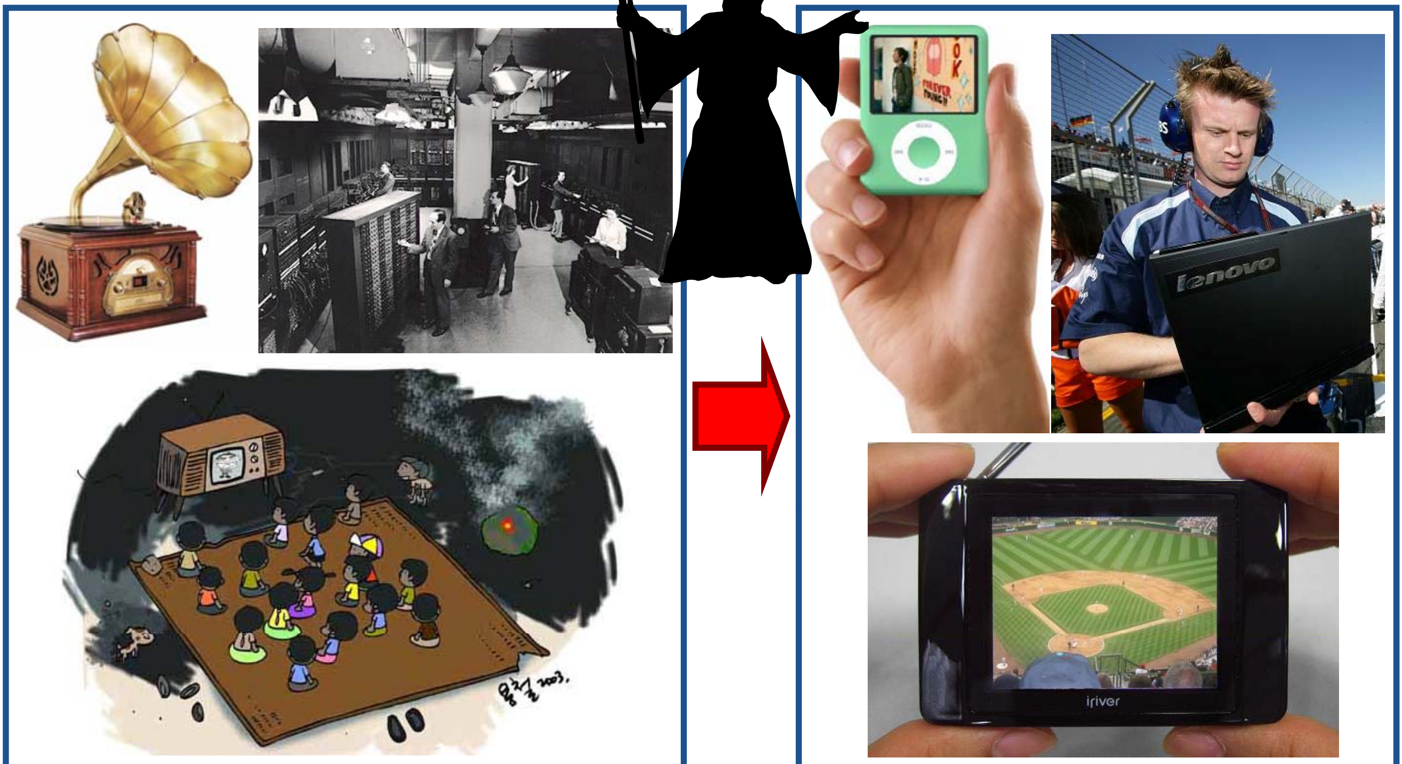
From 1965 to 2011



Semiconductor as an enabler !



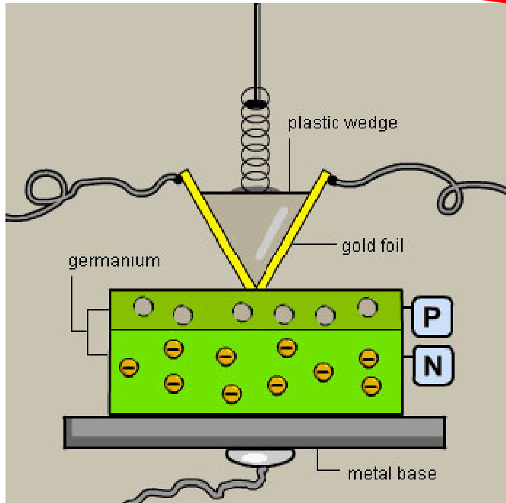
IC History

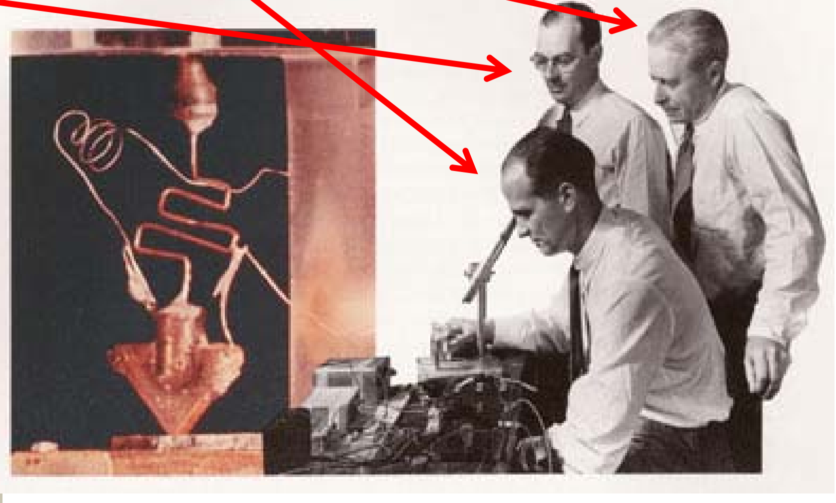
- 1947 The first transistor (Bell Telephone Laboratories)
- 1958 The first integrated circuit available as a monolithic chip (flip-flop) (Texas Instruments)
- 1959 The first bipolar planar transistor (Fairchild)
- 1960 The first MOSFET (Bell Telephone Laboratories)
- 1965 The first op-amp
- 1971 The first 4bit microprocessor (Intel 4004)
- 1972 The first 8bit microprocessor (Intel 8008)
- 1981 The first IBM PC

Genesis of Transistors

- When: 1947
- Affiliations: Bell Telephone Laboratories
- Inventors: William Shockley (leader), John Bardeen(theorist), Walter Brattain (experimenter)

They received the Nobel Prize in Physics in 1956!

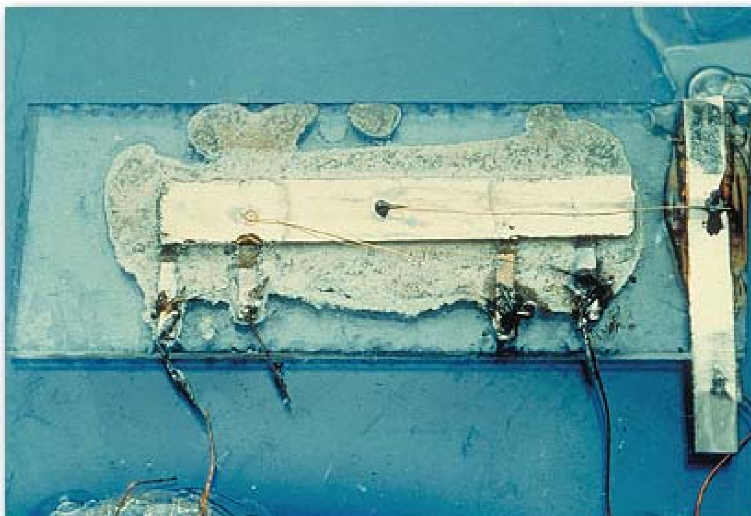


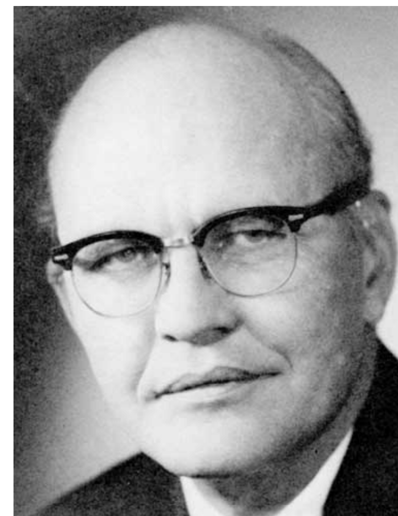


First IC

- When: 1958
- Affiliations: Texas Instruments
- Inventors: Jack Kilby
- Patent Application on Feb. 6, 1959 (Rejected)

He also received the Nobel Prize in Physics in 2000!



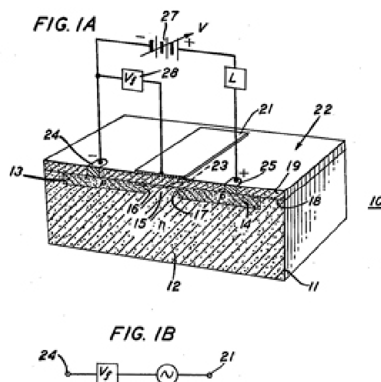


Another First IC ?

- When: 1959
- Affiliations: Fairchild
- Inventors: Robert Noyce
- Patent Application on July 30, 1959 (approved)
- After a long dispute, they became co-inventors.

First MOSFET

- When: 1960
- Affiliations: Bell Telephone Laboratories
- Inventors: Dawon Kahng, M. M. Attala



Aug. 27, 1963 DAWON KAHNG 3,102,230

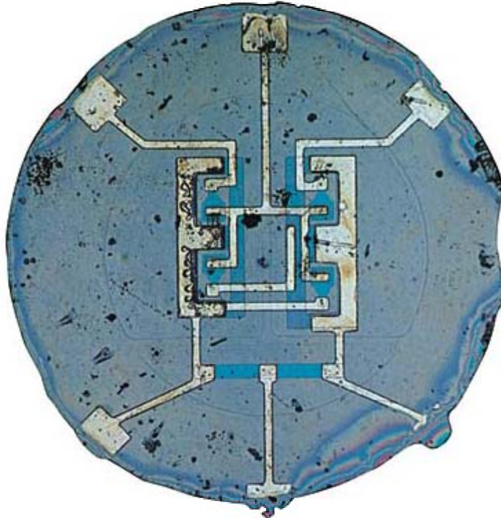
ELECTRIC FIELD CONTROLLED SEMICONDUCTOR DEVICE

Filed May 31, 1960

First Silicon IC

- When: 1961
- Affiliations: Fairchild
- Inventors: Robert Noyce
- The first commercially available IC.

He is one of the Intel's cofounders!



Fairchild (or Traitorous) Eight

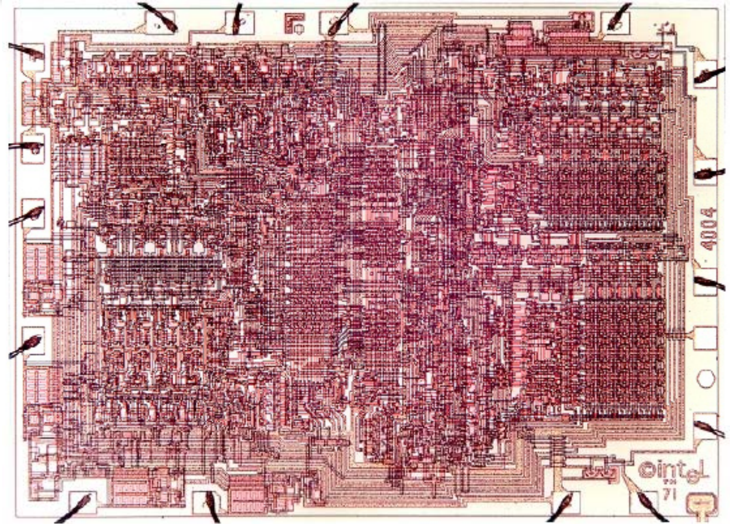
- William Shockley, who left Bell Labs in 1954 to start its own company in Palo Alto, CA. --> Silicon Valley
- Young people, such as Robert Noyce, joined Shockley Company.
- The "traitorous eight" including Robert Noyce, as Shockley came to call them, set up in 1957 Fairchild
- Fairchild: in 1959 new planar technology

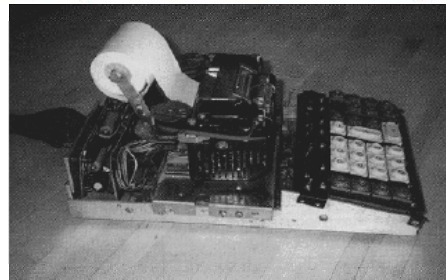
William Shockley's employees drink a toast to him on the day in 1956 when he was awarded the Nobel Prize in Physics for inventing the transistor. Eight of the crew shown here, went off on their own the next year and founded Fairchild Semiconductor Corporation.

From left: Gordon Moore, Sheldon Roberts, Eugene Kleiner, Robert Noyce, Victor Grinich, Julius Blank, Jean Hoerni, and Jay Last.

First Microprocessor

- When: 1971
- Affiliations: Intel
- Name: Intel 4004
- 2,300 Transistors
- The Intel 4004 was originally designed for use in a Busicom scientific calculator (Japan), but Intel engineers realized the design of the chip afforded multi-purpose use - thus the microprocessor was born.

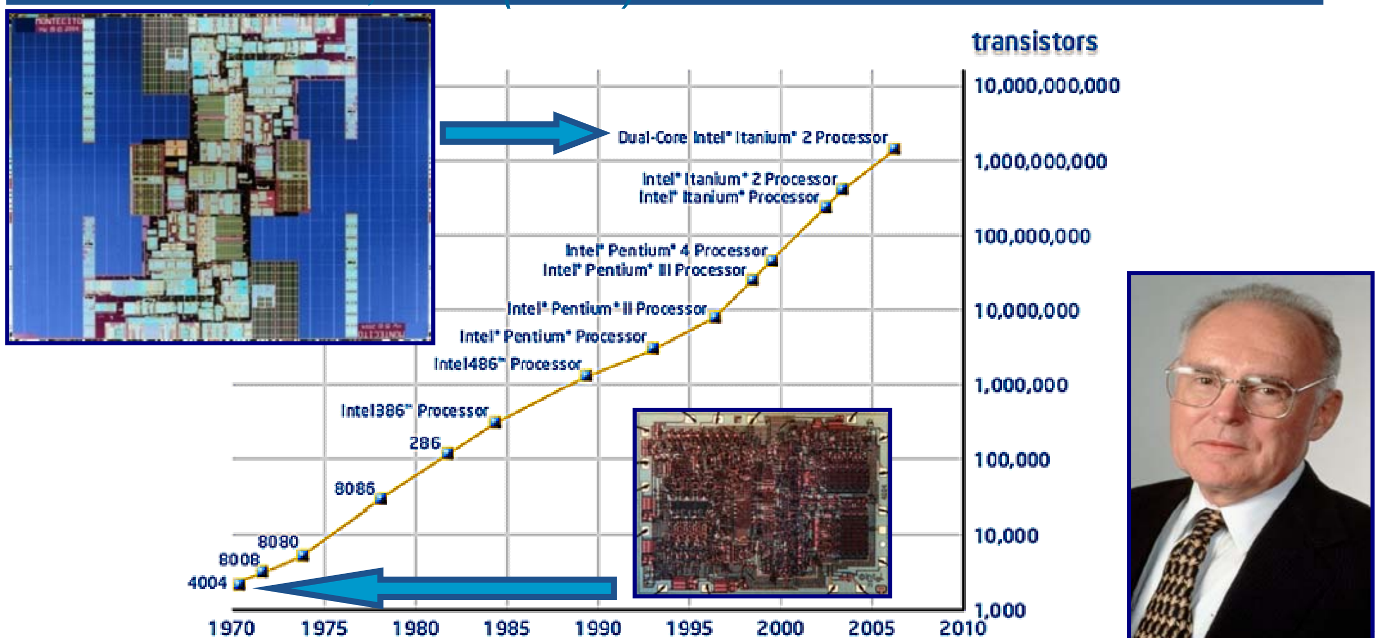




Moore's Law

"The number of transistors incorporated in a chip will approximately double every 18 or 24 months."

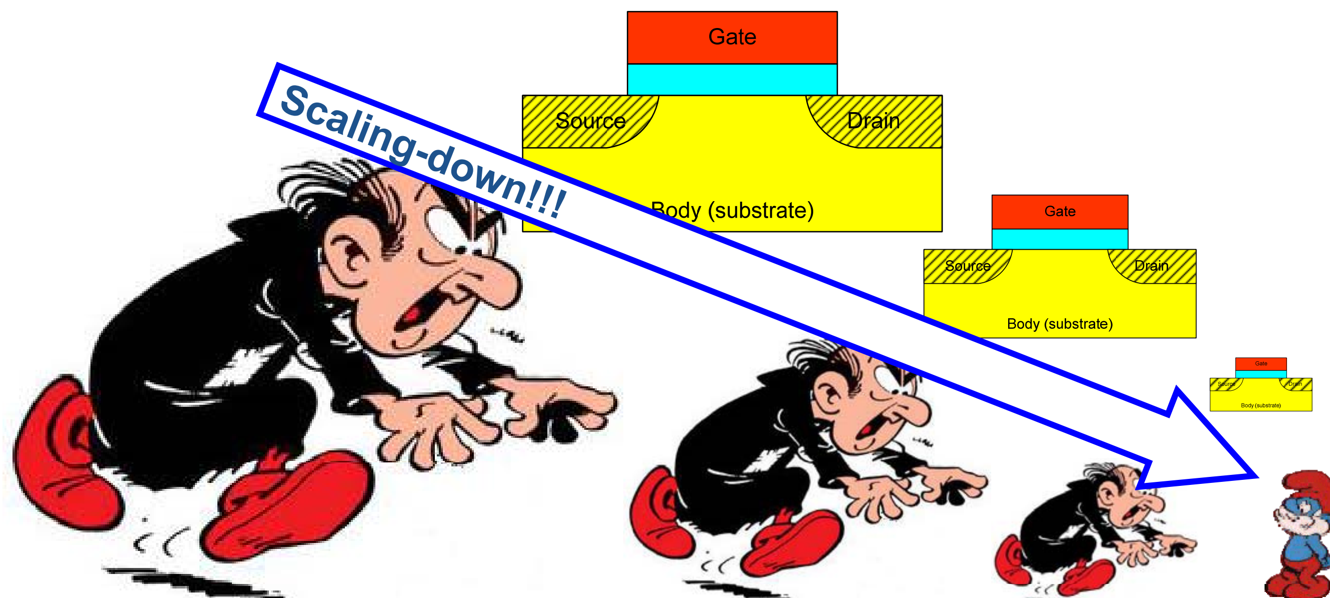
- Gordon Moore, Intel (1965)



CMOS Scaling (1)

❖ Definition of MOSFET scaling(-down)

- The reduction of lateral and vertical geometric dimensions of MOSFETs



CMOS Scaling (2)

❖ Difference between MOSFETs and Gagamel

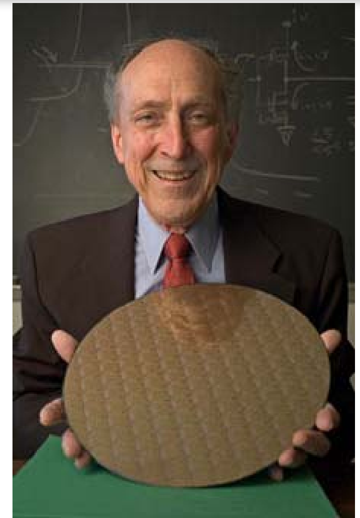
- Gagamel: the smaller, the weaker. No advantages over Smurfs.
- MOSFET: the smaller, the stronger!

❖ What's the meaning of "stronger"?

- More devices at the same area (cheaper price per device)
- Higher performance (higher speed)
- Lower power consumption

That's why semiconductor manufacturers are desperate to scale down devices.

How to Scale Down



❖ Constant-field scaling
- Proposed by Robert Dennard *et al*. (1974)
- Ideal scaling-down way
- Scaling the device voltages and the device dimensions (both horizontal and vertical) by the same factor(κ), so that the electric field remains unchanged.

❖ Constant-voltage scaling

❖ Generalized scaling

Constant-Field Scaling (1)

Objective:

Maintain a constant electric field as dimensions are scaled down.

$$L,\ W,\ t_{ox},\ x_j \rightarrow L/\kappa,\ W/\kappa,\ t_{ox}/\kappa,\ x_j/\kappa$$

$$N_a \rightarrow \kappa N_a$$

$$V_{dd} \rightarrow V_{dd}/\kappa$$

Constant-Field Scaling (2)

Quantity	Scaled quantity
$\mathcal{E}$	$\mathcal{E}$
$v = \mu\mathcal{E}$ or (v_{sat})	v
$W_d = \sqrt{\frac{2\varepsilon_{Si}}{qN_a}(\psi_{bi} + V_{dd})}$	$\sim W_d / \kappa$
$C = \frac{\varepsilon A}{t}$	C / κ

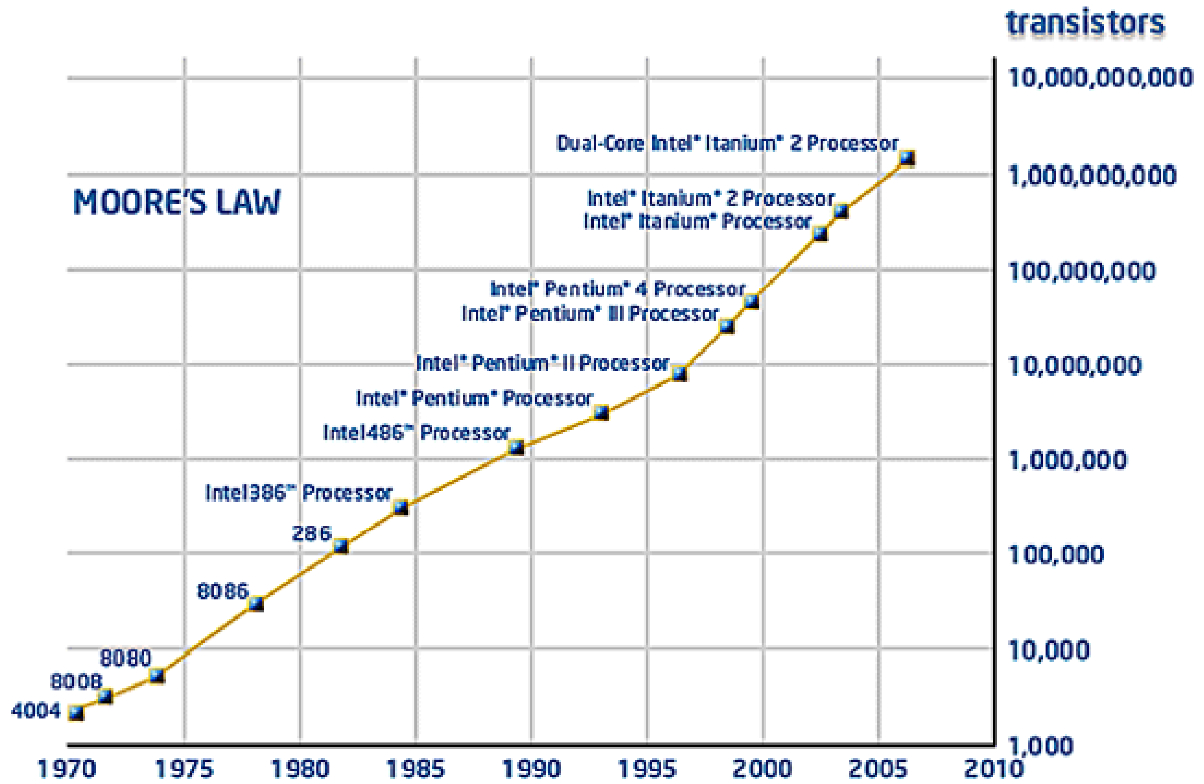
Constant-Field Scaling (3)

Quantity	Scaled quantity
$Q_i = C_{ox}(V_{gs} - V_t)$	Q_i
$I_{ds} = WQ_i v$	I_{ds} / κ
$R_{ch} = \frac{V_{ds}}{I_{ds}} = \frac{L}{W\mu_{eff}Q_i}$	R_{ch}
$V_t = V_{fb} + 2\psi_B + \frac{\sqrt{2q\varepsilon_{Si}N_a(2\psi_B)}}{C_{ox}}$	$> V_t / \sqrt{\kappa}$

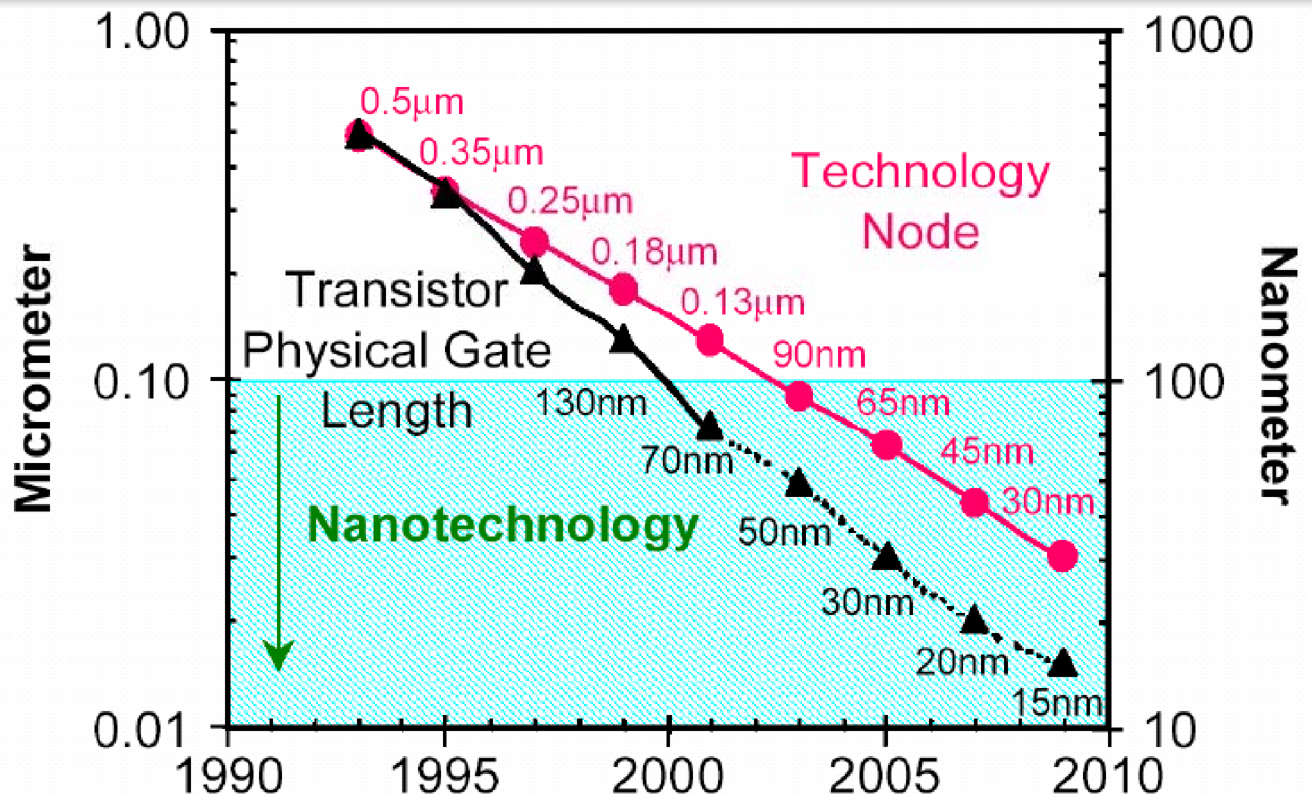
V_t → Nonscaling factor

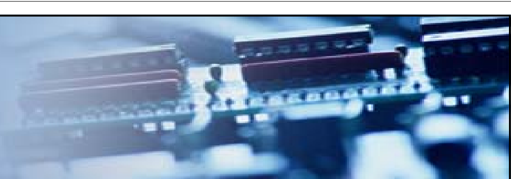
need V_t / κ

Moore's Law Is Still Alive (1)

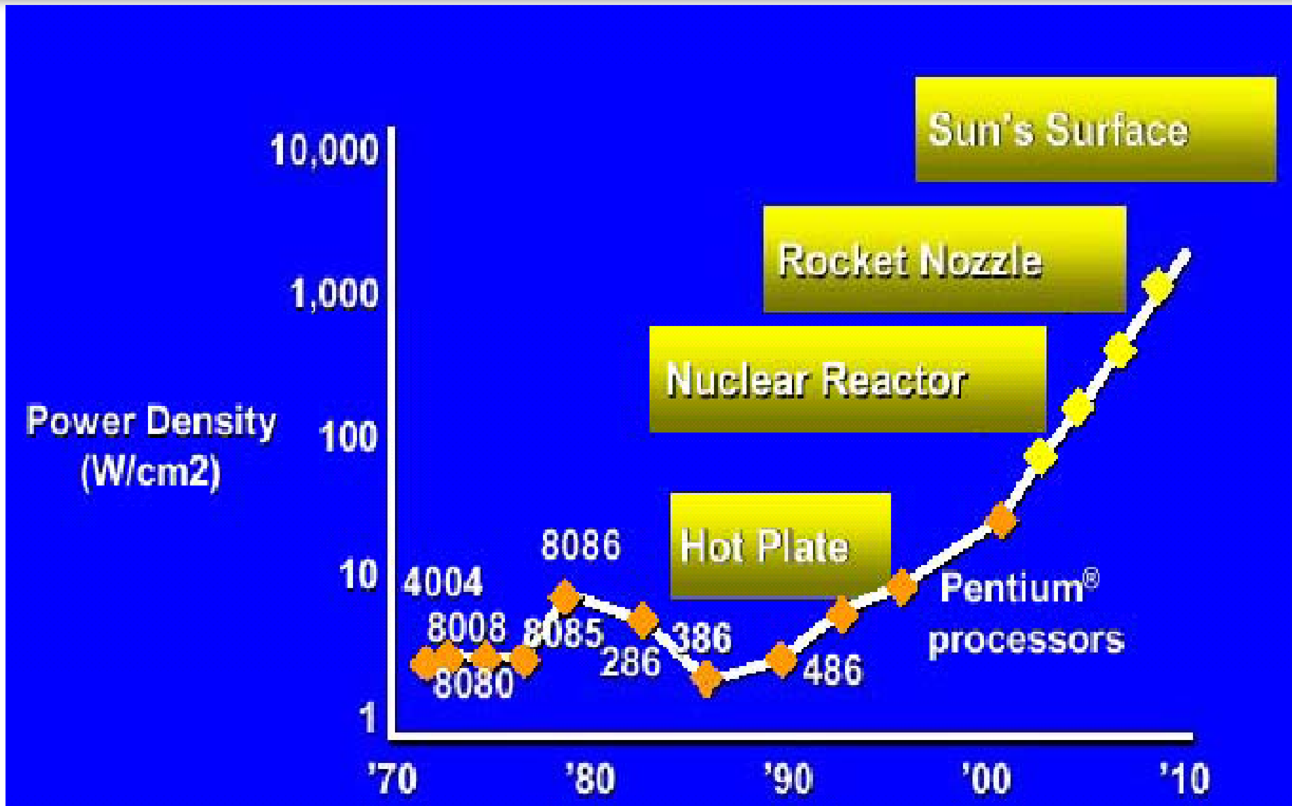


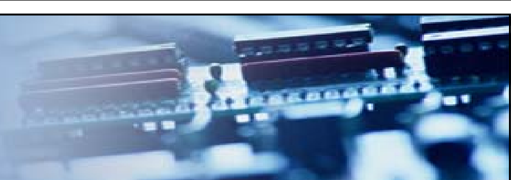
Moore's Law Is Still Alive (2)





CMOS Power Consumption





Accelerated Scaling-Down

"The number of transistors incorporated in a chip will approximately double every 18 or 24 months."

- Gordon Moore, Intel (1965)

"The paradigm shift in the memory industry requires a new memory growth model: a twofold increase per year in memory density."

- Chang-Gyu Hwang, Samsung (2002)

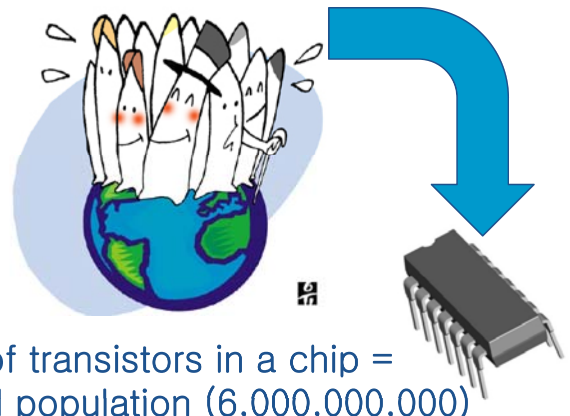
Where Are We Now?

- **Scaling-down is still the driver in semiconductor business competition.**
- **Technology node**
  - 32 nm in production
  - 22 nm in development
  - 15 nm in research
  - Next generations (10 …… nm) remain undefined in many technical aspects.

Challenges

- **CMOS scaling is expected to stop in the year 2022 according to the ITRS 2009.**
- **Technology barriers**
  - Transistor scaling (L_G, t_{ox}, x_j, etc.)
  - Interconnect scaling
  - Statistical variation
  - Cost

Channel length = 1/3000 of the diameter of a hair (100um)

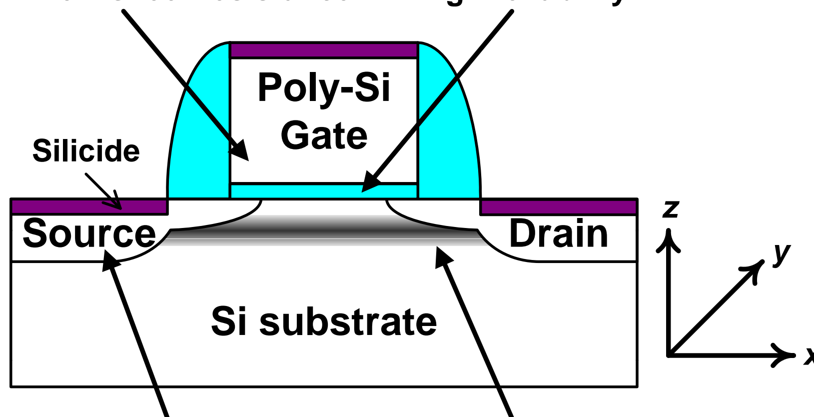


No. of transistors in a chip = world population (6,000,000,000)

Conventional Approach (1)

Gate Material
- No polydepletion
- No boron penetration
- Dual workfunction
- Low sheet resistance

Gate Dielectric
- Thin effective oxide thickness
- Low tunneling current
- Low defect density
- High reliability



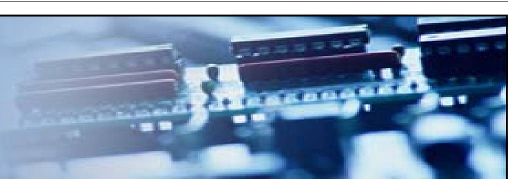
Source/Drain
- Ultra-shallow junction
- Low sheet resistance

Channel
- Low junction leakage
- Low junction capacitance
- Super steep halo or retrograde doping

Conventional Approach (2)

❖ Limitations

- Gate length (L_G) has scaled thanks to the scaling of gate oxide thickness (t_{ox}), source/drain junction depth (x_j), substrate doping concentration (N_{sub}), and operating voltage (V_{DD}).
- N_{sub} increases at the cost of channel mobility, which leads to performance degradation.
- Nevertheless, performance is enhanced by lowering V_{TH}, thinning t_{ox}, slowing V_{DD} scaling.
- So, performance improvement and static power consumption are inevitable.



How to Overcome Crisis

Same Structure and Same Materials

FD-SOI MOSFETs
UTB MOSFETs
Strained silicon engineering

New Structure but Same Materials

Double-gate MOSFETs
Triple-gate MOSFETs
Gate-All-Around MOSFETs

Next-Generation Device

Same Structure but New Materials

Metal gate
High-k dielectric gate insulator

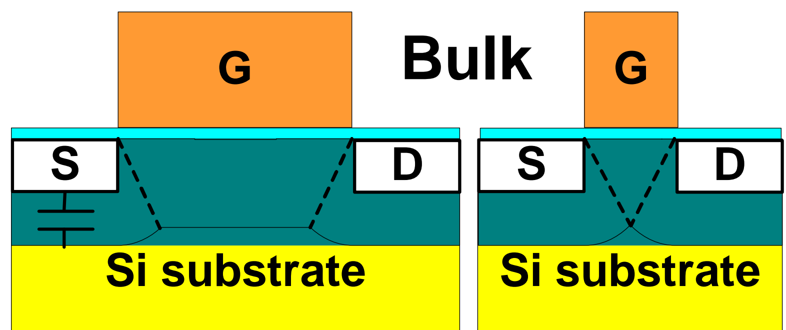
Novel Device Concepts

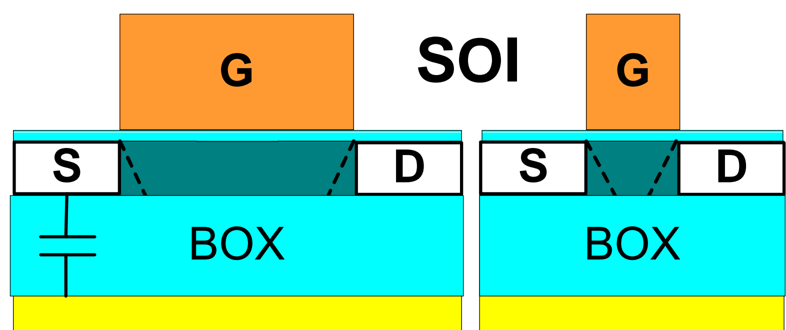
SETs, FITETs
TFETs, I-MOS devices

Same Structure and Same Materials (1)

FD-SOI MOSFETs

- Short channel effect suppression
- High channel mobility
- Subthreshold swing reduction
- Low junction leakage
- Low junction capacitance





Same Structure and Same Materials (2)

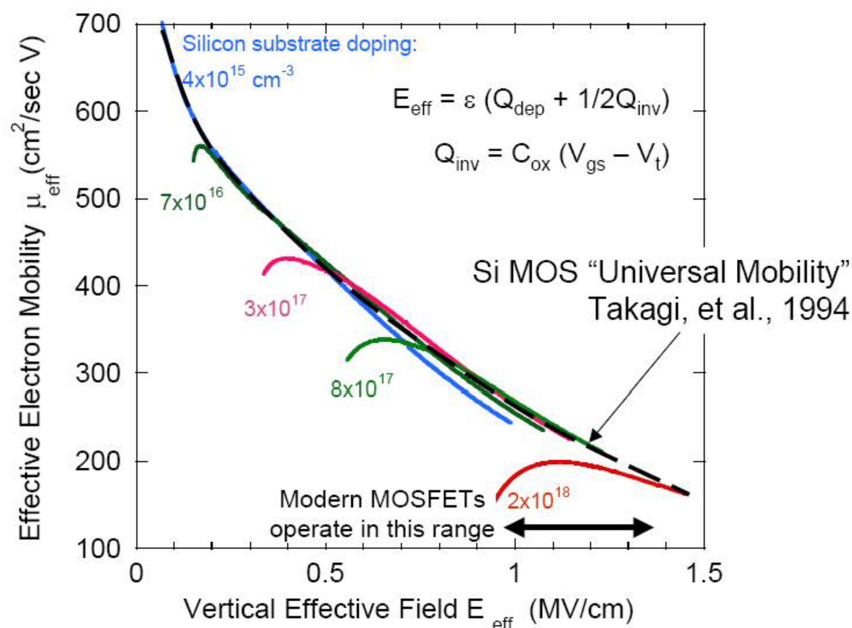
❖ Strained silicon engineering (1)

- To minimize gate delay (increase speed), drain current should be increased.
- Increase of drain current
  - L_G reduction
  - t_{ox} reduction
  - Carrier mobility enhancement – no side effect if possible

$$I_{DS,sat} = \mu_{eff} \frac{\varepsilon_{ox}}{t_{ox}} \frac{W}{L_G} \frac{(V_G - V_T)^2}{2}$$

Same Structure and Same Materials (3)

❖ Strained silicon engineering (2)



Same Structure and Same Materials (4)

❖ Strained silicon engineering (3)

- Desired types of uniaxial stress

	nMOSFET	*pMOSFET*
X	Tensile	Compressive
Y	Tensile	Tensile
Z	Compressive	Tensile

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Same Structure but New Materials

High-k dielectric gate insulator
Metal gate

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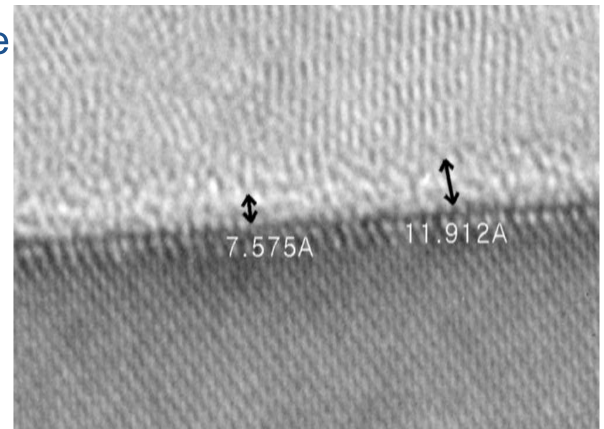
SETs, FITETs
TFETs, I-MOS devices

Same Structure but New Materials (1)

❖ High-k dielectric (1)

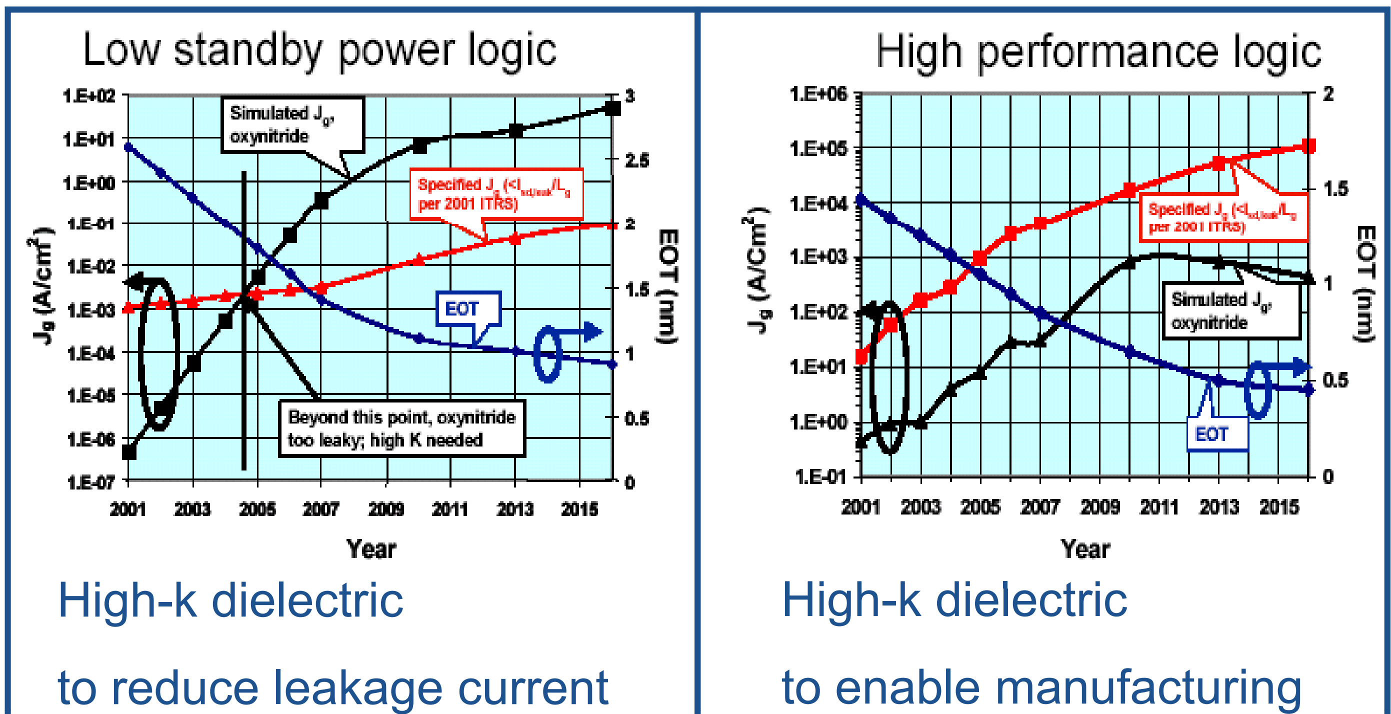
- The success of CMOS technology is greatly owed to the excellent properties of SiO_2.
- Properties of SiO_2
  - Electrically neutralized Interface states
  - Easy to grow on silicon substrate
  - Easy to integrate in a process
  - High energy bandgap
  - Stability
  - Scalability



However, gate oxide thickness has reached its limit.

Same Structure but New Materials (2)

❖ High-k dielectric (2)



Same Structure but New Materials (3)

❖ High-k dielectric (3)

- Requirements
  - High dielectric constant
  - Interface quality
  - Barrier height
  - Gate material compatibility
  - Morphology
  - Thermal stability
- Deposited, not grown by
  - PVD (Physical Vapor Deposition)
  - CVD (Chemical Vapor Deposition)
  - ALD (Atomic Layer Deposition)

Same Structure but New Materials (4)

❖ High-k dielectric (4)

- Candidates

	Dielectric const.	*Bandgap (eV)*
HfO_2	24	5.7
Al_2O_3	9	8.7
Ta_2O_5	26	4.5
ZrO2	25	7.8
SiO_2 (reference)	3.9	8.9

Same Structure but New Materials (5)

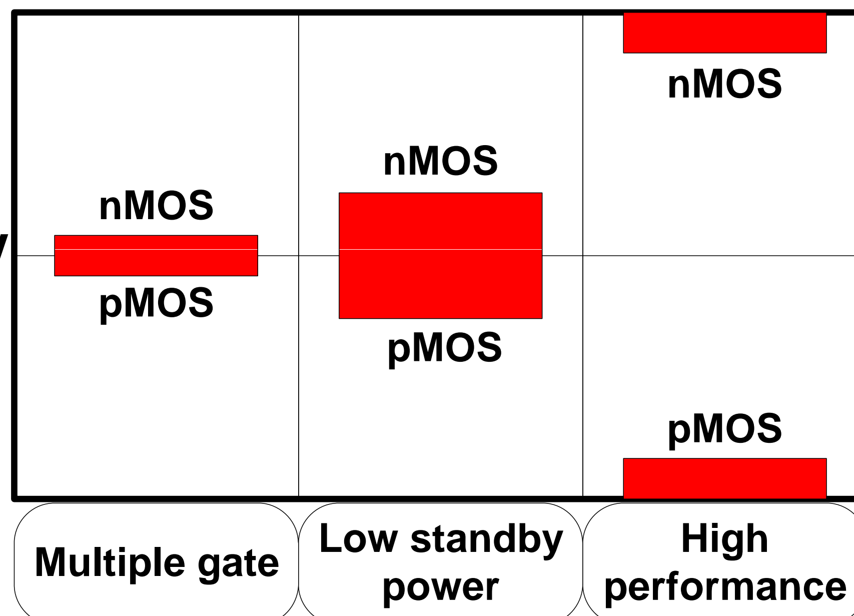
❖ Metal gate (1)

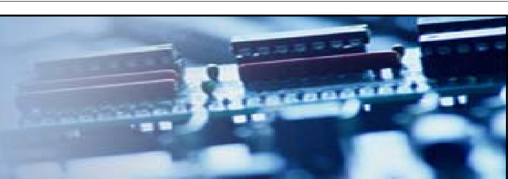
- Advantages
  - No polydepletion effect -> EOT reduction
  - Low resistivity
- Requirements
  - Appropriate work function
  - Low resistivity
  - Good interface with gate dielectric
  - Easy to deposit and etch
  - Thermal stability

Same Structure but New Materials (6)

❖ Metal gate (2)

- Work function requirements





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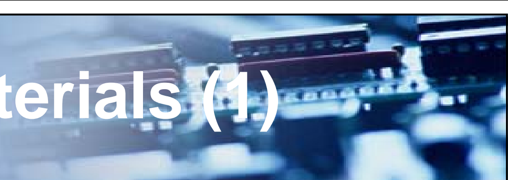
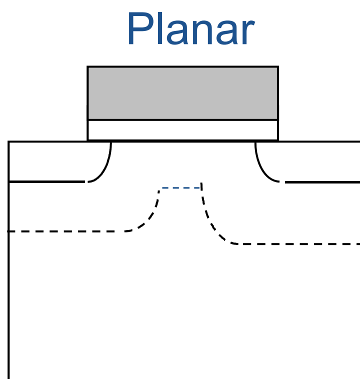


New Structure but Same Materials (1)

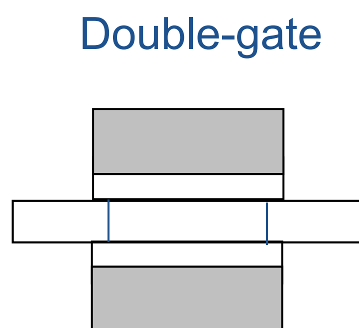
❖ Advantage of double-gate MOSFETs

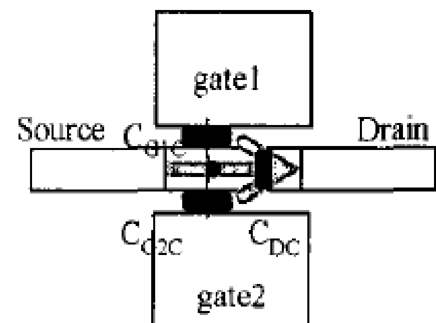
- Gate controllability ↑
- Short channel effect ↓
- Drive current ↑
- Gate oxide thickness ↑

Planar



Double-gate





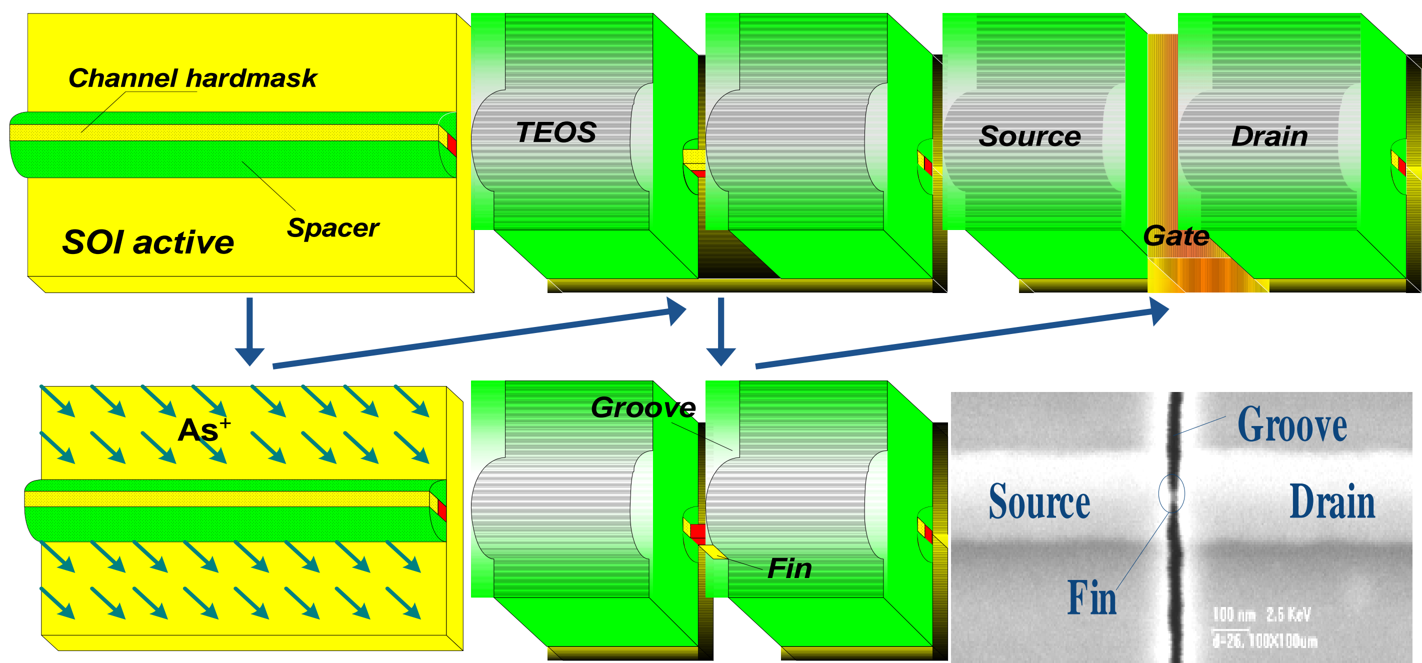
New Structure but Same Materials (2)

❖ Issues related to FinFETs

- Channel doping
  - High current drivability ← Low channel doping
  - Dopant fluctuation problem
- Gate stack material
  - negative threshold voltage problem
  - Gate material work-function control : metal gate, FUSI
- Fin width
  - UTB : $T_{si} \le L_G/3$
  - Double gate MOSFET : $W_{fin} \le 2 \times L_G/3$
- Source/drain resistance
  - As L_G scales down, W_{fin} must decrease and parasitic resistance increases.

New Structure but Same Materials (3)

❖ FinFETs with low S/D resistance



<D. S. Woo *et al.*, *IEEE Trans. Nanotech.*, 2002.>

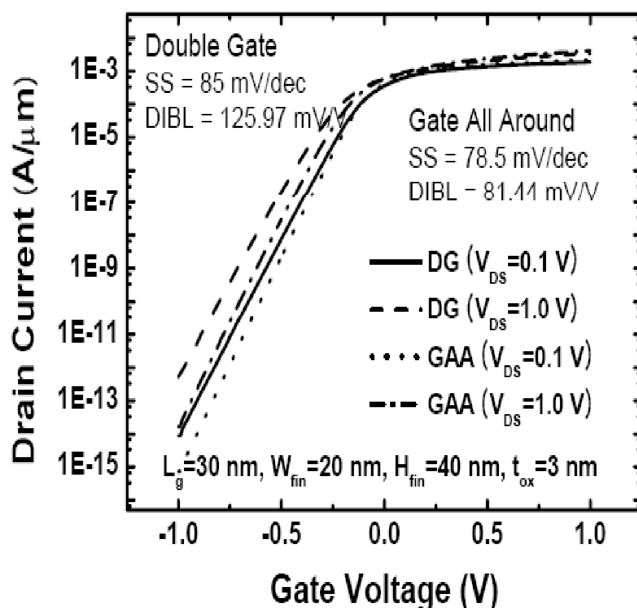
New Structure but Same Materials (4)

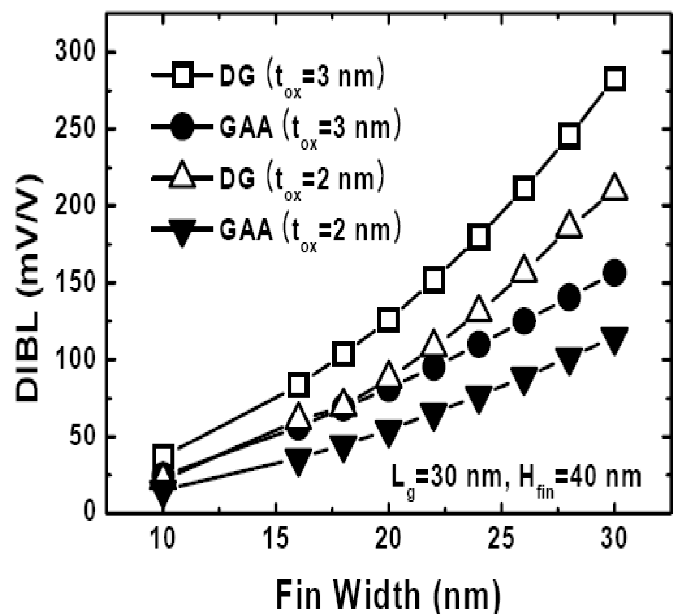
❖ Why triple or GAA MOSFETs?

- The more, the better.
- More gates provide additional capacitances, which have an effect on the channel.
- SCE immunity ↑
- Current drivability ↑
- Gate oxide thickness ↑
- Gate leakage current ↓
- The ratio of the fin width to the gate length ↑

New Structure but Same Materials (5)

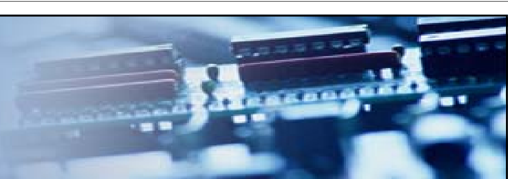
❖ Double-gate vs. GAA MOSFETs





<J. Y. Song *et al.*, *IEEE Silicon Nanoelec. Workshop*, 2005.>

How to Overcome Crisis



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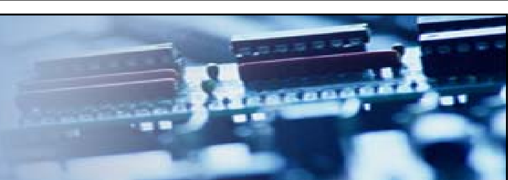
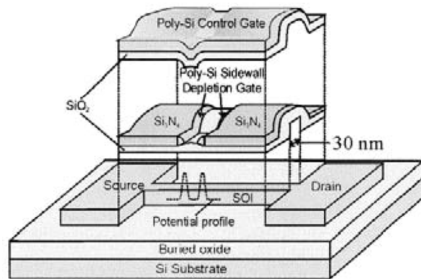
Novel Device Concepts (1)



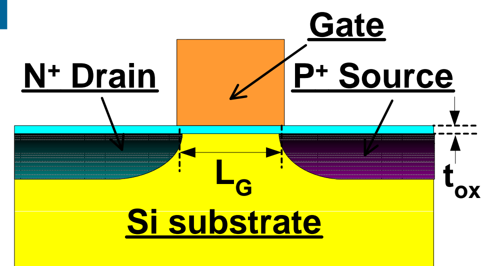
❖ Various kinds of novel devices

SET



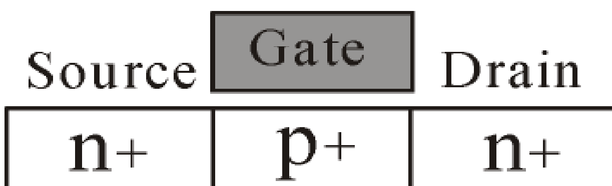
<D. H. Kim *et al.*, *IEDM*, 2001.>

TFET



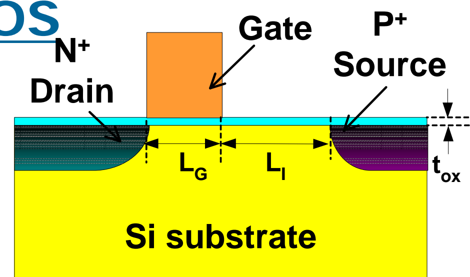
<W. Y. Choi *et al.*, *IEDM*, 2005.>

FITET



<K. R. Kim *et al.*, *IEEE EDL*, 2004.>

I-MOS

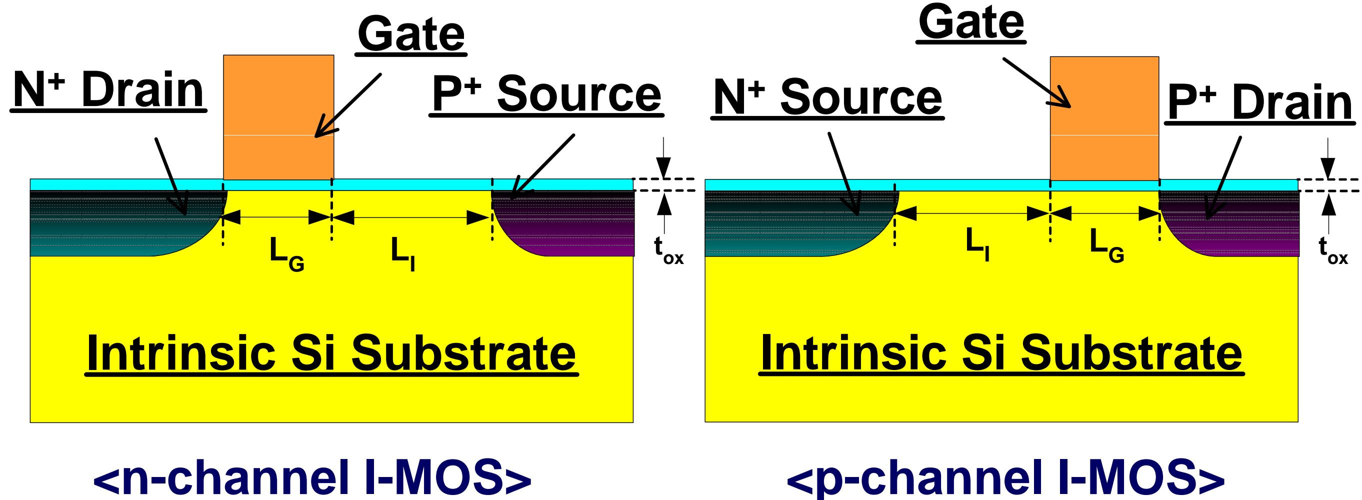


<W. Y. Choi *et al.*, *IEDM*, 2004.>

Novel Device Concepts (5)

❖ I-MOS (1)

- It uses modulation of avalanche breakdown voltage of a gated p-i-n diode.
- Subthreshold swing less than 60 mV/dec at room temp.



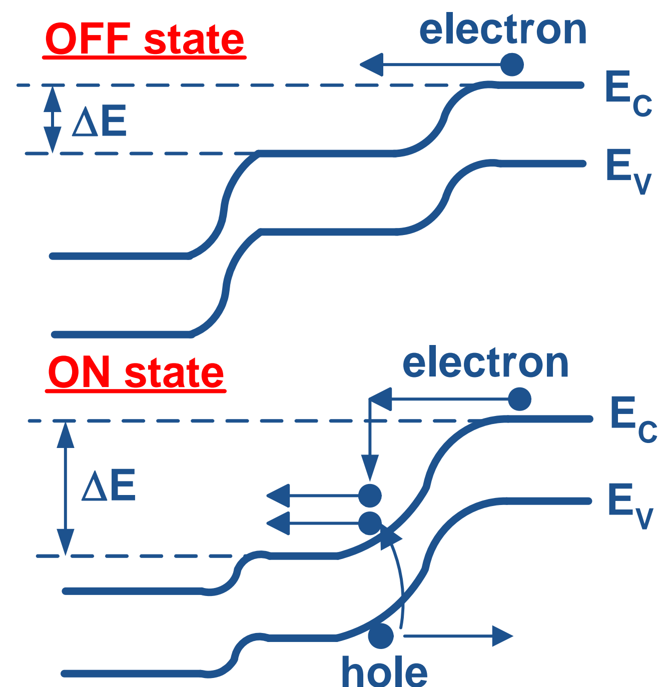
<n-channel I-MOS> <p-channel I-MOS>

3D Integration and Device Lab. (http://tidlab.sogang.ac.kr)

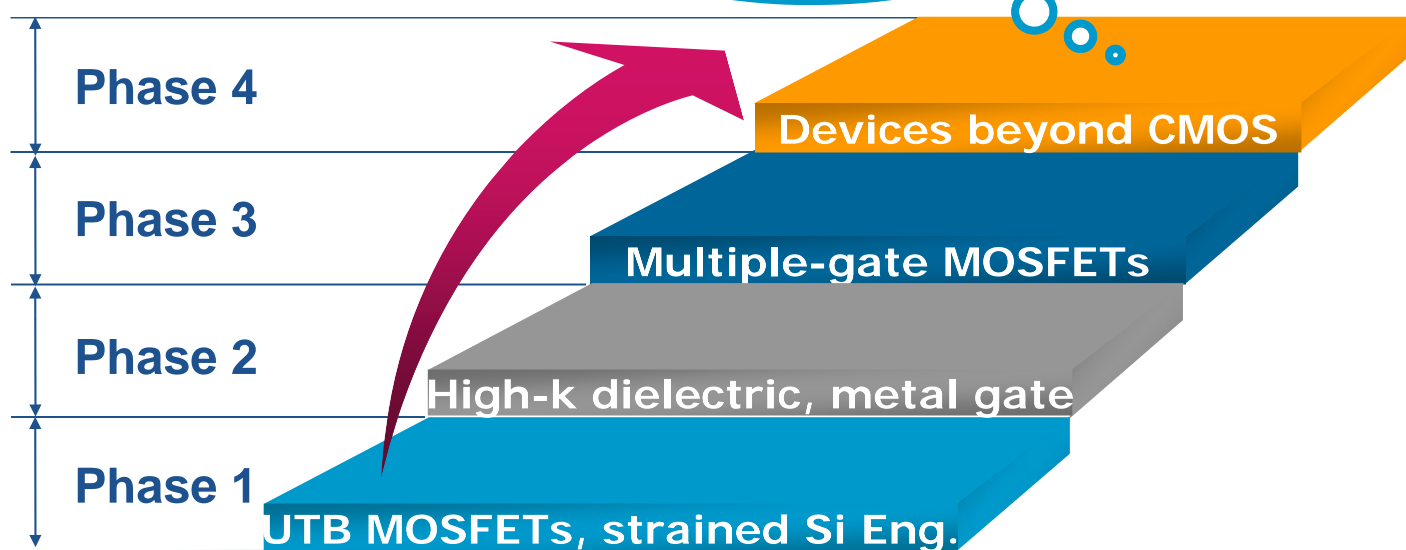
Novel Device Concepts (6)

❖ I-MOS (2) – basic operation principle

- ***OFF state*** ($V_G < V_{TH}$): The energy between the channel and the source is not enough to induce avalanche breakdown.
- ***ON state*** ($V_G > V_{TH}$): The energy between the channel and the source is enough to induce avalanche breakdown.



What Will Happen in the Future?



Conclusions

- Some technical challenges and breakthroughs have been reviewed.
- In order to surpass 32-nm technology node, various novel technology elements and interdisciplinary collaboration are strongly required.

Crisis is a chance. Use your imagination.