

High speed silicon Mach-Zehnder modulator

Ling Liao, Dean Samara-Rubio, Michael Morse, Ansheng Liu, Dexter Hodge

Intel Corporation, SC12-326, 2200 Mission College Blvd., Santa Clara, CA 95054
ling.liao@intel.com

Doron Rubin

Intel Corporation, S. B. I. Park Har Hotzvim, Jerusalem, 91031, Israel

Ulrich D. Keil and Thorkild Franck

Intel Copenhagen, Mileparken 22, Skovlunde DK-2740, Denmark

Abstract: We demonstrate a silicon modulator with an intrinsic bandwidth of 10 GHz and data transmission from 6 Gbps to 10 Gbps. Such unprecedented bandwidth performance in silicon is achieved through improvements in material quality, device design, and driver circuitry.

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1. Introduction

It is challenging to achieve high speed optical intensity modulation in silicon (Si) because the material does not exhibit any appreciable electro-optic effect [1]. In [2,3] we presented our first device design based on the free-carrier plasma dispersion effect wherein the phase shifting elements of a Mach Zehnder interferometer (MZI) are metal-oxide-semiconductor (MOS) capacitors embedded in Si rib waveguides. An applied voltage induces an accumulation of charges near the gate dielectric of the capacitor, which, in turn, modify the refractive index profile of the waveguide and ultimately the optical phase of light passing through it. The MOS capacitor is operated exclusively in accumulation bias so that the device bandwidth is not limited by carrier recombination in Si. In [2,3], this first version of the MOS-capacitor device was shown to have 2.5 GHz small-signal bandwidth and a demonstrated capacity to transmit data at 1 Gbps. Through the design of customized drive circuitry, the 2.5 GHz device has achieved 4 Gbps data transmission [4], though with an extinction ratio (ER) of only 1.3 dB due to the relatively low phase modulation efficiency of this first device. Significant changes to the Si waveguide design and processing have been made to further improve modulator bandwidth and ER without increasing the optical loss of the critical phase-shifting regions. This new version of the modulator demonstrates data transmission up to 10 Gbps with 3.8 dB ER and ~ 10 dB of on-chip loss.

2. Device design

Figure 1 shows a scanning electron microscope (SEM) cross-sectional image of this new Si waveguide-based MOS capacitor phase shifter. It comprises a 1.0 μm n-type doped crystalline Si (the Si layer of the SOI wafer) on the bottom and a 0.55 μm p-type doped crystalline Si on the top with a 10.5 nm gate dielectric, a multi-layer stack of silicon dioxide and nitride, sandwiched between them. In the first version of the device, the waveguide cross-section was 2.5 μm x 2.3 μm and the top Si layer was actually poly-silicon (poly-Si), which is significantly more lossy than crystalline Si due to defects in the material lattice [5]. Here, a process called epitaxial lateral overgrowth (ELO) is used to grow the crystalline Si on top of the gate dielectric to improve device transmission [6]. To target high bandwidth performance, the doping concentrations of both the Si slab and ELO-Si rib of the new device are significantly higher than those of the previous poly-Si based modulators [2,3]. The doping level here is $2 \times 10^{17} / \text{cm}^3$ for the Si slab and $1 \times 10^{18} / \text{cm}^3$ for the ELO-Si rib. It should be noted that these doping levels are not optimized in that the device resistance is likely limited by the Si slab resistance. As a result, the ELO-Si doping concentration may be reduced without significant impact to device speed.

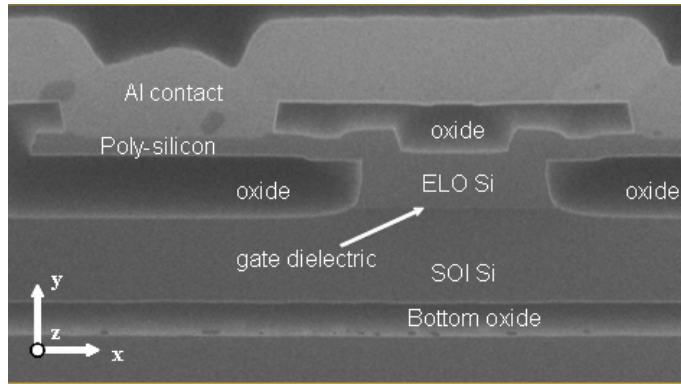


Fig. 1. SEM cross-section of the new phase shifter with ELO-Si rib.

To form the rib waveguide, the ELO-Si, gate dielectric, and $\sim 0.1 \mu\text{m}$ of the SOI Si are etched. As a result, the waveguide rib height is $0.65 \mu\text{m}$ and the waveguide slab thickness is $0.9 \mu\text{m}$. The rib width is $1.6 \mu\text{m}$ (measured at the mid-point of the rib), and because the sidewalls of the waveguide rib are not entirely vertical, the gate dielectric width is $1.9 \mu\text{m}$. In order to minimize the metal contact loss, we designed two $\sim 3 \mu\text{m}$ wide poly-Si pieces to slightly overlap the top corners of the ELO-Si rib. Aluminum contacts are deposited on top of this poly-Si layer as shown in Fig. 1. The oxide regions underneath the poly-Si pieces and on both side of the rib maintain optical confinement and prevent optical field from penetrating into the contact areas. All waveguide dimensions here are smaller than the first version of the device; as a result, the optical mode is more tightly confined and interacts more strongly with the charges. This effect is illustrated in Fig. 2, which compares line-cuts (in the y -direction) of modeled mode profiles of the two devices. Note that the new design has significantly stronger optical field in the vicinity of the gate where the charges accumulate.

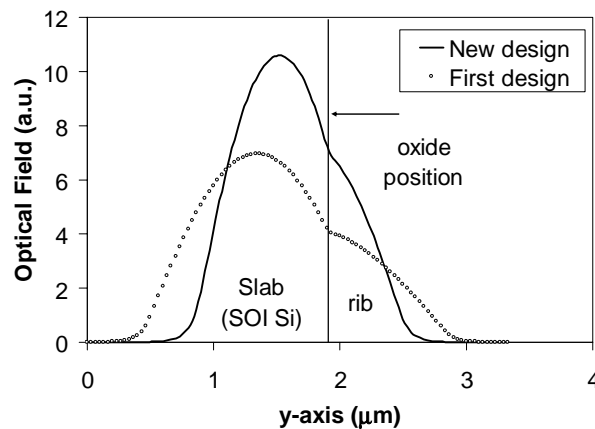


Fig. 2. Vertical line-cuts of the modeled mode profiles of the new device depicted in Fig. 1 and the first version of the device presented in [2,3]. The optical field intensity at the gate is higher for the new device which allows the gate charges to more strongly influence n_{eff} .

The overall length of the MZI modulator is 15 mm , which includes input and output waveguides, 3dB splitters, and two arms of nominally equal length (13 mm). A schematic of the device is shown in Fig. 3. Each arm comprises a 3.45 mm long high-doping, high-speed RF MOS capacitor phase shifter and two $\sim 4.75 \text{ mm}$ long lightly-doped, low-speed phase

shifters that are driven with DC voltages to electrically bias the MZI at quadrature. High speed operation requires the use of a low impedance drive circuit. A custom IC has been developed and used in all data transmission measurements exceeding 1 Gbps including measurements in [4]. The driver is manufactured using a 70 GHz- F_T SiGe HBT process and employs a push-pull emitter-coupled logic (ECL) output stage which is wire-bonded directly to the RF phase-shifters. As indicated schematically in Fig. 3, the 3.45 mm long RF phase-shifters, each with 26.4 pF capacitance, are divided into eleven equal sections of 315 μm with each section having bond pads for the two differential signals (applied to the p-type ELO-Si of the phase shifters) and the RF return path (connected to the n-type Si slab). The driver operates from a single-ended power supply in the range of 3.3 to 3.9 V and is targeted to deliver up to 1.6 V_{pp} (3.2 V_{pp} differential) into 27 pF phase-shifters when operating at 8 Gbps. A number of control settings are available to trade performance for power dissipation (from 2.7 W to 3.9 W depending on supply voltage, output swing, bit rate, and edge rate). Of this power, approximately 10% is dissipated in the modulator. Improved driver design and improved phase-shifter efficiency will lead to reduced power dissipation.

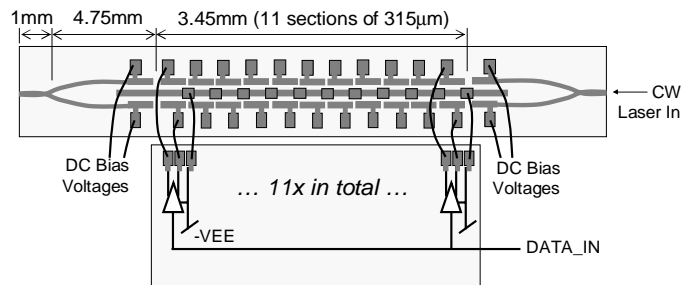


Fig. 3. Schematic of MZI, wire-bonds, and driver IC. Not drawn to scale.

3. Phase-shifter performance

In accumulation, the n-type Si in the MOS capacitor phase shifter is grounded and a positive drive voltage, V_D , is applied to the p-type ELO-Si causing a thin charge layer to accumulate on both sides of the gate dielectric. With a change in free-carrier density, both refractive index (n) and absorption (α) of Si are changed [7]. The change in index of the small amount of Si containing the charge layers (modeled to be 10 nm on both sides of the gate dielectric) is manifest as a change in the effective refractive index of the mode (n_{eff}). The resulting optical phase shift depends on this voltage-induced n_{eff} change, the device length, and the optical wavelength [2,3]. The n_{eff} change therefore critically determines the phase efficiency, and it is governed by design parameters such as the waveguide dimensions and the position of the gate dielectric as they determine how effectively the accumulated charges overlap with the optical mode [8]. As a figure of merit for phase efficiency, the product $V_\pi L_\pi$ can be determined from the measured phase shift, where V_π and L_π are the voltage swing and device length required to achieve π -radian phase shift. The goal is to minimize the $V_\pi L_\pi$ product to lower the required drive and shorten the device length. The phase shifter design of Fig. 1, with reduced waveguide dimensions of 1.6 μm x 1.6 μm compared to the first version of the device (2.5 μm x 2.3 μm), indeed demonstrates stronger mode-charge interaction with more than 50% reduction in $V_\pi L_\pi$: 3.3 V-cm compared to 7.8 V-cm. In addition, we measured waveguide losses of the new device to be 10 dB/cm for the high-speed sections and 2.5 dB/cm for the low-speed sections. If poly-Si were used for the waveguide rib, as has been the case for the first device, reported in [2,3], loss would be 16 dB/cm and 10 dB/cm for the high-speed and low-speed sections, respectively.

To understand the intrinsic bandwidth of the new modulator, the impedance of 315 μm long phase shifter sections is measured. The data is given in Fig. 4. Note that these test structures, with ELO-Si rib and high dopant concentrations, have a capacitance of 2.4 pF and resistance of 6.5 Ω . The RC cutoff frequency, $(2\pi RC)^{-1}$, is therefore in the range of 10 GHz for the new modulator.

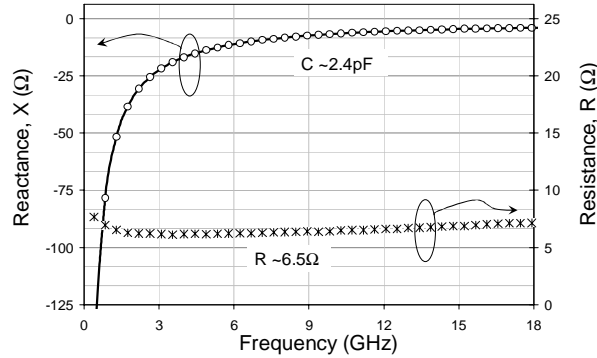


Fig. 4. Impedance of a 315 μm long phase-shift segment from the new ELO-Si device. The reactance is well modeled as a 2.4 pF capacitor, and the resistance is approximately 6.5 Ω , giving an RC cutoff of 10.2 GHz.

4. High speed data transmission

Optical characterization of the MZI modulator discussed in section 2 shows that it has a total insertion loss of 19 dB: 10 dB of on-chip loss and 9 dB of coupling loss. Of the 10 dB on-chip loss, 3.5 dB is due to the high-speed (RF) sections, 2.5 dB is due to the low-speed (bias) sections, and the remaining 4 dB is likely due to a combination of voltage-induced free carrier absorption [8] and un-optimized design of the splitters and bends. Optical coupling to the 1.6 μm x 1.6 μm waveguides is done using lensed single-mode fibers with approximately 3.3 μm spot size. The total coupling loss of 9 dB can be significantly reduced using one of the known waveguide mode converter techniques [9-11]; however, the devices reported here do not include any on-chip mode converter because focus was given to the understanding of the MOS-capacitor based phase shifters.

To characterize data transmission performance, a DC voltage of -3.3V, the lowest voltage potential in the system, is applied to the n-type Si slab. Then a voltage is applied to the ELO-Si rib of the low-speed phase sections to accumulate the MOS capacitors so to bias the MZI at quadrature. An AC voltage swing of 1.4V is applied to the ELO-Si rib of the RF phase shifters; the associated DC bias is chosen such that the entire AC swing is above the flat-band voltage [2]. This voltage swing, based on calculation for device in Fig. 3, should yield 0.15 π -radian phase shift in each MZI arm, enough to give a modulation ER of 4.2 dB. Figure 5(a) shows the measured eye diagram of the device at $\lambda = 1.55 \mu\text{m}$. The data is generated using a 6 Gbps $2^{32}-1$ pseudorandom bit sequence (PRBS) source and collected using an optical plug-in of a digital communications analyzer (DCA). The eye diagram shows 4.5 dB ER and 57 ps rise time (RT), which gives a nominal bit rate, defined as $BR^{\text{nom}} = (3 \times RT)^{-1}$, of 6 Gbps. Even though these ER and data rate represent a significant improvement over the 1.3 dB and 4 Gbps performance achieved using the first version of the modulator [4], 6 Gbps is not limited by the new waveguide modulator itself since the intrinsic bandwidth (RC cutoff) is above 10 GHz. Further analysis reveals two causes for the 6 Gbps bandwidth limit. First, the wirebond inductance (estimated to be 0.7 nH) chokes the high-frequency components of the capacitor charge/discharge current pulses (LC cutoff frequency is ~ 3.9 GHz). Second, the driver circuitry has a limited slew rate and was, in fact, expected to deliver 8 Gbps performance under nominal operating conditions. To test this assertion that the

bandwidth limitation is extrinsic to the modulator, a device with 20% higher intrinsic bandwidth was measured, and it gave identical rise and fall times as those of Fig. 5(a).

The new modulator has also been tested with 10 Gbps PRBS input, and a representative eye diagram is given in Fig. 5(b). The eye is open and only slight degradation in ER is observed compared to the 6 Gbps eye - 3.8 dB ER compared to 4.5dB ER. It is encouraging to note that the edge rates and jitter only change gradually as data rate is increased, which suggest that electronic equalization could be used in the receiver to improve eye margin at 10 Gbps.

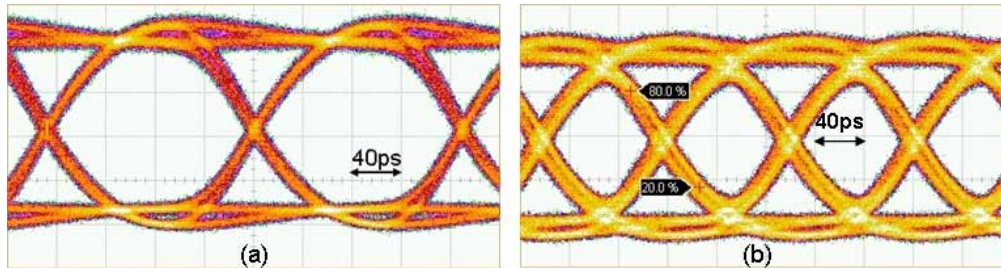


Fig. 5. Optical eye diagrams of modulator co-packaged with driver; both eye diagrams have the same vertical and horizontal scales. (a) 6 Gbps: ER, RT, and FT are 4.5 dB, 57 ps, and 54 ps, respectively. (b) 10 Gbps: ER, RT, and FT are 3.8 dB, 55 ps, and 56 ps, respectively. Measured modulation speed is limited by driver performance.

Although the Si modulator based on the MOS-capacitor design is orders of magnitude faster than any other Si based waveguide modulator [12,13] and it is continuing to show bandwidth improvement, it is still significantly slower than modulators based on either the electro-optic crystal LiNbO₃ [14,15] or III-V semiconductor compounds and multiple quantum wells [16-19]. These devices have shown modulation frequencies in excess of 40 GHz [15,19]. It should be noted, however, that the Si modulator presented in this paper is not fully optimized, and phase efficiency, optical loss, and bandwidth performance can all be improved. A modeling study shows that by further reducing the waveguide dimensions down to 1 μm x 1 μm and thinning the gate dielectric to 6 nm, the phase shifter's $V_{\pi}L_{\pi}$ product is expected to be as low as 0.68 V-cm [20]. Thus, in applications demanding high ER (i.e. 12 dB), the RF phase shifting section in each MZI arm could be < 0.2 cm assuming that the AC drive remains at 1.4 V_{pp} . Alternatively, by sacrificing extinction ratio (i.e., 6 dB), it would be possible to drop the drive voltage requirement below 1 V_{pp} allowing for the use of standard CMOS drive circuits. By optimizing the doping profiles as well as the MZI splitter design, this small cross-section device can achieve 10 GHz modulation bandwidth with >12 dB ER and on-chip loss as little as 2 dB. Of course, even higher bandwidths can be obtained by simply increasing the doping concentrations, though at the expense of higher loss [20].

5. Conclusions

We have demonstrated a waveguide modulator based on a MOS capacitor with unprecedented performance in Si. It exhibits an estimated intrinsic bandwidth (as measured by RC cutoff) of 10 GHz and driver-limited near rail-to-rail data transmission at 10 Gbps with 3.8 dB ER. In addition, we have achieved nearly 2X improvement in device phase efficiency and effectively managed optical loss with a significant materials improvement. Future efforts include optimization of dopant distribution and MZI splitter design to reduce on-chip loss, incorporation of optical tapers to reduce coupling loss, further reduction of waveguide dimensions to scale phase modulation efficiency, and improvement of drive circuitry to realize higher data rate transmission.

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