Silicon Photonic Circuits: On-CMOS Integration, Fiber Optical Coupling, and Packaging

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(Invited Paper)

***Abstract*—Silicon photonics is a new technology that should at least enable electronics and optics to be integrated on the same optoelectronic circuit chip, leading to the production of low-cost devices on silicon wafers by using standard processes from the microelectronics industry. In order to achieve real-low-cost devices, some challenges need to be taken up concerning the integration technological process of optics with electronics and the packaging of the chip. In this paper, we review recent progress in the packaging of silicon photonic circuits from on-CMOS wafer-level integration to the single-chip package and input/output interconnects. We focus on optical fiber-coupling structures comparing edge and surface couplers. In the following, we detail optical alignment tolerances for both coupling architecture, discussing advantages and drawbacks from the packaging process point of view. Finally, we describe some achievements involving advanced-packaging techniques.**

***Index Terms*—Hybrid IC packaging, optical fiber couplers, photonic integration, silicon-on-insulator (SOI).**

I. Introduction

FOR MORE than 30 years, the optical interconnect solutions have been gradually implemented from very long to short distances due to the continuously increasing bandwidth demand. As a result, optical fiber networks have been progressively deployed, in long haul (>10 km) telecommunications links first, down to enterprise LAN, metropolitan, and access networks. Nowadays, because of the intrinsic limitation of copper links in high-data rate servers, Internet switches, and supercomputers, optical links are widespreading also in very short reach (VSR) systems [1]. In these systems, copper cables are typically replaced by active optical cables (AOC) using fiber ribbon, allowing concatenated data rate of 120 Gb/s to be reached over tens of meters of multimode fiber. Compared with the electrical interconnect solutions, optical links exhibit several demonstrated advantages, such as lower signal attenuation, lower dispersion, and crosstalk leading to superior bandwidth by distance products. Another significant advantage of the optical solutions is the immunity of the signals transmission to electromagnetic interference, which makes them very well suited to mobile systems. However, optical links remain more expensive than electrical links. As a result, the next generation of optical components needs to be low cost and compatible with high-volume manufacturing.

An obvious way to achieve this requirement is to increase the integration on optical devices. In spite of many technology developments since the beginning of optical communications, one should admit that the integration level has remained low compared to the microelectronic technology, due to various reasons, particularly the size of integrated optics components and the heterogeneity of photonic materials [2].

Silicon photonics, using highly confined optical modes in silicon waveguide, appears as a unique opportunity to cope with this integration challenge. In addition, it opens the door to simultaneous manufacturing of electronic and optic function on the same chip using CMOS fabrication lines [3], [4] and standard well-mastered microelectronics fabrication process. Thus, it will allow manufacturers to build optical components using the same semiconductor equipments and processes they use for microelectronics ICs. The ultimate goal is to monolithically integrate optical transceivers or circuits into silicon IC chips. Recent developments have already shown an integration of several elementary optical functions into nanophotonic silicon circuits [4] as laser emission, detection, modulation, multiplexing, demultiplexing, and fiber coupling [5].

Such a monolithic implementation fulfills with the so-called "more than Moore" developments leading to integrate more nonmicroelectronic functionalities on a chip, which still keeps decreasing in size. Then, beyond wafer-level heterogeneous optic/electronic layer integration developments, this approach raises new packaging challenges in order to deal mainly with optical coupling and thermal cooling. Indeed, optical fiber is

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still the more relevant medium to transmit optical data, especially as compared with single-mode signals transmitted in tiny silicon wires. Therefore, aligning and connecting one or several fibers to a millimeter-squared-sized silicon photonics chip is a challenge according to the selected fiber-coupling structure.

In this paper, we present results on silicon photonics technology packaging from the very first stage with on-CMOS photonics layer integration to the very last stage with electrical and optical connections. In a first part, we present monolithic integration strategies with a focus on the embedding into the last levels of metallization above the IC layer obtained by photonics wafer to electronics wafer bonding. Then, we present fiber- to silicon-wire-coupling structures comparing their performances and how they can take advantage of the previous photonic layer integration. Finally, the on-CMOS photonics chip packaging is considered with optical alignment tolerances and assembling strategies.

II. On-CMOS Photonic Layer Integration

The ultimate goal of silicon photonics development is to monolithically integrate a photonic layer with optical functions onto silicon IC chips [6]. By cointegrating optics and electronics on the same chip, high-functionality, high-performance, and highly integrated devices can be fabricated. While using well-mastered microelectronics fabrication process lines, it would make CMOS photonics accessible to a broad circle of users in a foundry-like fabless way. In addition, advances in CMOS photonics will move the emphasis from device component to architecture. Industrial and Research and Technology Development efforts could then be focused on new products or new functionalities rather than on technology level.

Concerning the photonic layer, most of the building blocks have already been fabricated using very standard wafer-level process. For instance, detectors, modulators, multiplexers, fiber couplers, and other passive circuits only required standard microelectronics process, such as epitaxy, coating, lithography, and etching. Today, only the laser integration remains rather specific either with an external laser source or with an integrated laser source from III–V material (InP or InGaAs) bonded onto the wafer during the process flow.

Then, we can find three main ways to perform this photonics layer integration (see Fig. 1): embedded into the metal interconnect layers, combined front-end, and backside.

The combined front-end approach (option 2) has been successfully demonstrated by Luxtera Company [7]: both the photonics fabrication and the transistors fabrication are combined at the front-end level. Photonics and electronics structures share the chip footprint leading to moderate integration density. The thermal budget then rules the process steps and is compatible with rather high-temperature process, such as Germanium epitaxy in order to implement high-speed photodetectors. The back-end process is common to electronics and photonics. In this approach, until now, the laser has not been integrated: an external source is flip-chip bonded onto each chip and coupled with silicon wire circuit. The packaging of such a chip is then rather specific in order to deal with its laser assembly.

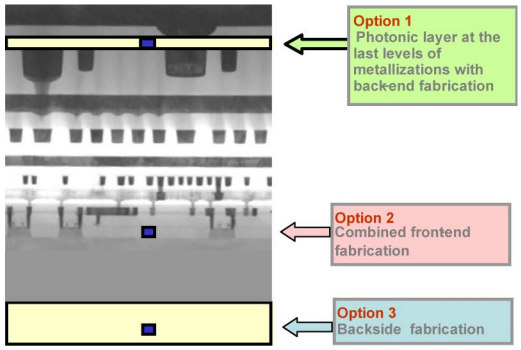

Fig. 1. Photonic layer integration on CMOS options.

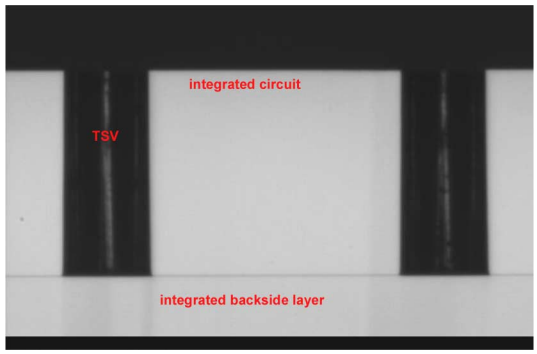

Fig. 2. TSV through silicon for backside integration.

The backside approach (option 3) is developed by Austriamicrosystems within the frame of the pHotonics ELectronics functional Integration on CMOS (HELIOS) European project. This solution takes advantage of the rear side of the electronics wafer. Integration of photonic layers at the backside of the CMOS wafer is performed by bonding and connecting a CMOS wafer and a photonic wafer. First, the CMOS wafer is processed up to the last metal layer and the backside is thinned and fine polished to prime wafer surface quality. The photonic layers are then added by wafer-to-wafer bonding at low temperature. Afterward, electrical interconnects between the CMOS layer and the photonic layer are obtained using through-silicon vias (TSV). Deep silicon etching is performed down to the metal layer of the photonic layers (see Fig. 2). Subsequent TSV isolation and metallization are deposited. Then, the top metal, which connects the TSV with the IC, and the passivation is deposited and structured. Finally, the substrate wafer is removed in order to release the photonic structures. Advantageously, in this approach, the IC and the photonic processings are rather independent and the packaging of such double-side chip is developed for other applications, such as imaging devices. However, double-side thermal management may be an issue.

In this paper, we will focus on the integration approach (option 1) developed at Commissariat à l'Energie Atomique, Laboratoire d'Électronique des Technologies de l'Information (CEA-LETI) and Interuniversity Microelectronics Centre (IMEC), where the photonic layers are embedded into the last levels of metallization above the IC layer (see Fig. 3). Thus, due

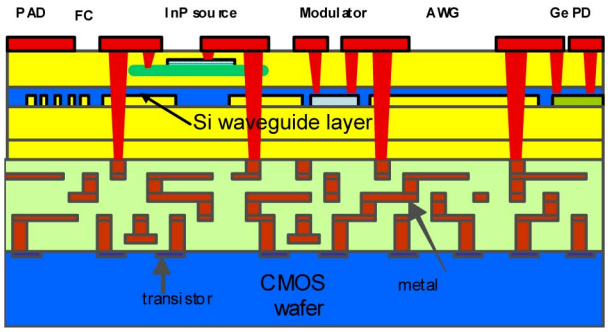

Fig. 3. Illustration of a photonic layer integration at the last levels of metallization above the IC layer.

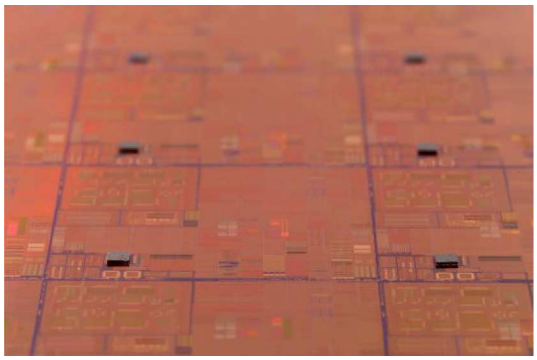

Fig. 4. InP dies bonded onto a CMOS circuit wafer at the metal interconnect layers before next steps processing.

to this 3-D stacking, a high-integration density can be performed and multilevel process for silicon waveguide can be considered.

One of the main advantages of this integration approach is the independence of electronics and photonics layers that avoid any change in the electronics library design. Moreover, any IC technology (e.g., CMOS, SiGe, and analog) can be used: it is open to any standard front-end electronic technologies and full integration of III–V on Si is available.

Depending on the devices to be processed two suboptions are considered. The first consists in building the photonics layer with only low-temperature processes (<400 °C). For example, low-temperature deposition of amorphous layers or die-to-wafer bonding can be used. The second consists in fabricating the photonic functions on a separate wafer and then to bond it on the electronic wafer. The photonic layer is integrated by wafer-to-wafer bonding above the IC layer at the last levels of metallization with back-end fabrication. The substrate initially holding the photonic layer is then removed and the last levels of metallization are processed, including the interconnections between the photonic and the IC layer. In this approach, high-temperature processes can be used for the fabrication of photonic functions (e.g., Si-based modulators and Ge-based photodiodes).

Considering the integration of III–V material for the active parts, these two suboptions may also be combined. Indeed, multiple quantum wells layers on III–V dies can be mounted on top of the waveguides by die-to-wafer bonding (see Fig. 4). The substrate of these dies is then removed by chemical etching and further processing steps are performed, which lead to sources and detectors coupled to the silicon wires and connected to the metallic interconnects of the IC.

The aforementioned IC integration option appears to be very promising in term of integration density and straightforward implementation with the microelectronic process lines as the photonic layer can be treated as any additional metallic layer on the top of the electrical interconnect layers. Moreover, compared with option 3, photonic functions are very close to IC blocks, which is a mandatory condition to reduce the noise signals introduction at high-frequency operations. Nevertheless, this integration approach must consider the final packaging. For instance, the thickness between the optic and the electronic layers can be optimized according to the heat dissipation, which may be performed either at the frontside or the backside of the chip. It will depend on the selected package, which is mainly defined by the number of electrical I/O, the speed of electrical I/O, and the heat to be dissipated. Finally, the fibered optical I/O must be introduced as a new package design parameter depending on the number of fibers to connect and to the optical fiber-coupling structures.

III. Optical Fiber-Coupling Structures

Silicon nanophotonic circuits can exhibit a very high level of functional integration due to the very small cross sections of the silicon waveguides with less than 1 μm mode-field diameter (MFD). However, to be implemented in data optical transmission networks, such circuits still must be interfaced with optical fibers having much larger dimensions with about 10 μm MFD. Due to this mismatch in size, a coupling structure is required in order to minimize the coupling loss that is obtained. This is achieved by computing and maximizing the recovering integral between the two modes. This coupling structure must adapt a wide fiber mode with a narrow silicon wire mode defining the insertion loss. Another issue is the polarization management: in their topology, silicon waveguides are generally highly birefringent, and in the other hand, polarization in fiber-based networks is unpredictable and varies randomly with time.

The insertion loss between an optical fiber and a nanophotonic circuit is definitively a big issue as it directly determines the link performances, such as the link reach, the signaling rate, the receiver sensitivity, etc. Moreover, in order to be compatible with functions for fiber to the home (FTTH) or wavelength-division multiplexing (WDM) applications, for instance, a good coupling structure is also required to be broadband and polarization nonsensitive. Finally, beyond the performance, the selection of the coupling structure is also related to the cost issue by considering the wafer-level testing capability and the packaging requirements with fibers assembling and thermal management.

Experimentally, various solutions have already been implemented, each one having some significant advantages, but also significant drawbacks. In this chapter, we will describe the two structures, which exhibit very complementary performances: edge fiber coupler with adiabatic inverse tapers and surface fiber coupler with gratings. Edge fiber couplers are in-plane spot size converters that increase the MFD to several micrometers in order to match with the optical-fiber-mode diameter. The coupling

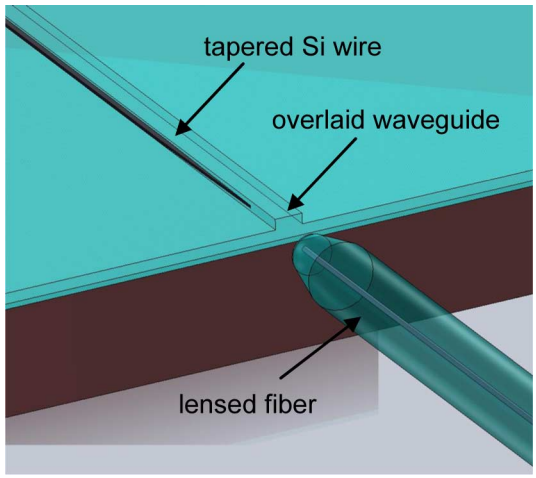

Fig. 5. Illustration of the spot size converter with the Si wire into a larger SiOx rib waveguide in front of a lensed fiber.

is performed at the edge of the chip and the fiber is in the plane of the chip. However, surface fiber couplers are out of plane spot size converters: the beam is first laterally expanded, and then, extracted from the surface to a quasi-perpendicular direction. The coupling is performed anywhere on the chip and the fiber is rather perpendicular to the chip.

A. *Edge Fiber Coupler*

The most efficient edge fiber coupler today is a spot-size converter that gradually transforms a highly confined mode into a wider mode supported by a low-index-contrast waveguide, such as an optical fiber [8]–[12]. Typically, in silicon wire exhibiting a large refractive index contrast with the cladding ($\Delta n \sim 2$), the propagating-mode diameter may be reduced to less than 1 μm, while it is about 10 μm into standard single-mode optical fibers, which are ITU-T G.652.D compliant and used with legacy single-mode networks.

The mode-size converter, we present in this part, is constructed from silicon-on-insulator (SOI) wafers with a 2-D tapered Si wire and an overlaid high-index silicon-rich oxide (SiOx) waveguide [13]. With a fabrication based on microelectronics technology, a silicon strip waveguide having a width of 500 nm and a thickness of 220 nm is laterally tapered down to 80 nm by means of deep ultra-violet (DUV) 193 nm lithography and reactive-ion etching (RIE) techniques. The linear variation of the Si wire width is rather smooth with a length between 200 and 300 μm depending in the structure design. The overlaid waveguide is a 3.5-μm-thick layer of SiOx: the amount of silicon nanocrystals is tailored to obtain a refractive index about 1.6 in order to be very close to that of the single-mode fiber (SMF) core. This thick layer is partially etched (1.5 μm) to form a rib waveguide "the injector" exhibiting a few micrometers mode-field size. This mode size is then compatible for a coupling with state-of-the-art high-performance lensed fiber (see Fig. 5).

The coupling mechanism between the fundamental modes of the Si wire and the SiOx overlaid waveguide is based on a phase-matching condition. The operation principle of the adiabatic

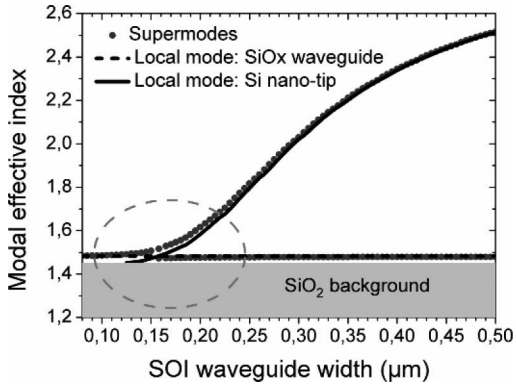

Fig. 6. Modal effective indexes as a function of the Si wire width (TE case). The dashed circle is centered on the phase-matching region.

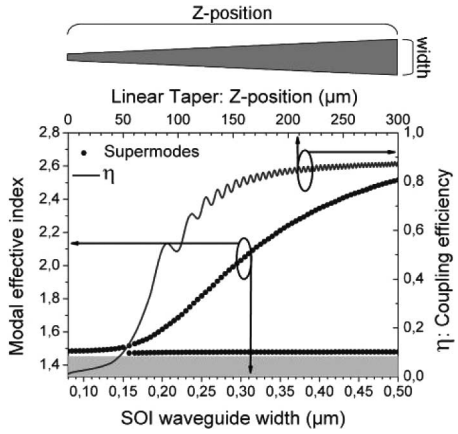

Fig. 7. Modal effective indexes as a function of the SOI waveguide width and coupling efficiency along the taper length. The relative Z-position of the taper is associated with the corresponding SOI nanowire width.

taper structure is shown in Fig. 6, where the effective indexes of the supermodes of the entire structure, as well as the effective indices of the local modes are plotted, which are the modes of the uncoupled waveguides, according to the SOI waveguide width. When the local mode of the SiOx overlaid waveguide excites a supermode, and that this supermode is adiabatically transformed over the phase-matching region, light is coupled into the SOI waveguide. At the Si nanotip, the supermode-field profile is delocalized from the Si wire core. This delocalization of the field profile ensures a strong overlap with the local mode of the SiOx overlaid waveguide.

Using the beam propagation method, simulation results of a fiber coupler with a 300-μm taper length performed at 1.5 μm (TE case) are presented in Fig. 7. The field patterns show how the mode is evanescently coupled from the wide injector waveguide to the narrow SOI waveguide along the taper length (see Fig. 8). Coupling losses below 1 dB were calculated over the 1550–1600 nm wavelength range. Simulation results do not present significant changes of the coupling efficiencies for taper lengths varying between 200 and 300 μm.

For the experimental characterization, a single-mode lensed fiber with a MFD $= 3$ μm was used as an input reference. For each sample, light transmission is measured from input fiber

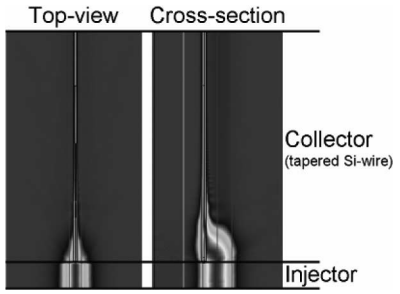

Fig. 8. Electric-field patterns, calculated at 1500 nm, demonstrating the efficient coupling between the wide overlaid waveguide (the injector section) and the narrow tapered Si wire (the collector section).

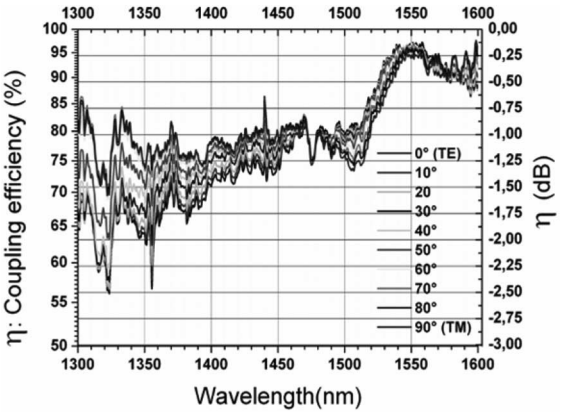

Fig. 9. Coupling efficiency measured as a function of the injection angle.

to output fiber through a waveguide with a coupler at both ends. The transmission characteristic includes then the losses at the facets between the fiber and the SiOx injector, the mode-conversion losses toward the silicon wire, and the waveguide propagation losses, which are negligible in our study. The coupling efficiency of one coupler is extracted from this measurement, assuming that the input and output couplers have identical performances, so as the fibers. Additionally, a tunable polarizer has been implemented in the optical setup to investigate the polarization behavior of the fiber couplers.

The experimental results are reported in Figs. 9 and 10. The coupling efficiency remains high in a broad spectral range: the bandwidth at 1 dB is around 100 nm (>300 nm at 3 dB) for both TE/TM polarization states. We can also notice that less than 0.25 dB coupling losses were measured at 1550 nm.

Three additional samples, selected over the whole 200 mm wafer, were characterized. Similar performances were obtained in the 1500–1600 nm spectral range (variations <0.2 dB). We observed variations of the coupling efficiency close to 0.6 dB at 1400 nm and 1 dB at 1300 nm.

In this paper, we have demonstrated a very efficient spot size converter between Si wire and silica optical fibers. The fiber-to-waveguide insertion loss appears to be lower than 1 dB in the wide 1520–1600 nm spectral range. Moreover, the polarization sensitivity is lower than the measurement accuracy. Such a high-performance level has been obtained due to the resolution of standard CMOS technology on 200 mm SOI wafer to fabricate

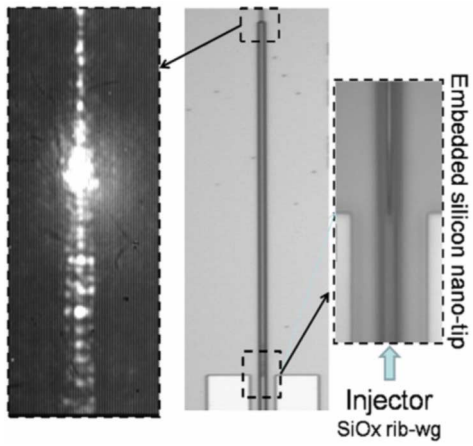

Fig. 10. Top-view images of the couplers (middle, right) associated with an infrared picture taken at 1300 nm (left) showing the end of the coupling transition to the overlaid waveguide (the injector).

silicon features smaller than 100 nm width required for this coupling structure.

Such an edge fiber coupler makes on CMOS photonic chips fully compatible with state-of-the-art planar lightwave circuits (PLC) packaging using actively aligned lensed fibers into metallic or ceramic packages. Nevertheless, further developments are planned on such edge fiber couplers in order to make them compatible directly with standard no-lensed fibers by increasing the overlaid waveguide-mode size. Such an improvement will allow to develop passive fiber alignment approaches in order to reduce the cost of assembling and packaging especially when considering multiple fiber connections. Finally, another point to develop is how to make such edge couplers compatible with wafer-level testing as it is for surface couplers.

B. Surface Fiber Coupler

Grating couplers lead to a vertical or quasi-vertical optical coupling of the light between a fiber and a nanophotonic circuit. This way, they can be located anywhere over the chip and not only at the edge. Therefore, compared with edge-coupling structures, such surface couplers allow light coupling without the need for dicing and polishing the chip edge, which also makes wafer-scale testing of nanophotonic circuits possible. This is the reason why grating coupler may appear to be one of the most relevant fiber-coupling structures for silicon photonics devices today. However, the high sensitivity of these structures to the operating wavelength and to the polarization state may limit the targetable applications. In this part, we present a grating structure that is robust to the integration of the photonic layers onto the electronics layers by wafer-to-wafer bonding. Indeed, the coupling efficiency of such gratings is very sensitive to the layers below.

Physically grating couplers are diffractive structures that are placed at the end of a lateral adiabatic taper. They produce an exiting mode, which may have the same dimensions as a diameter 10 μm SMF making possible a direct butt-coupling between the fiber and the chip. Typically, the grating couplers

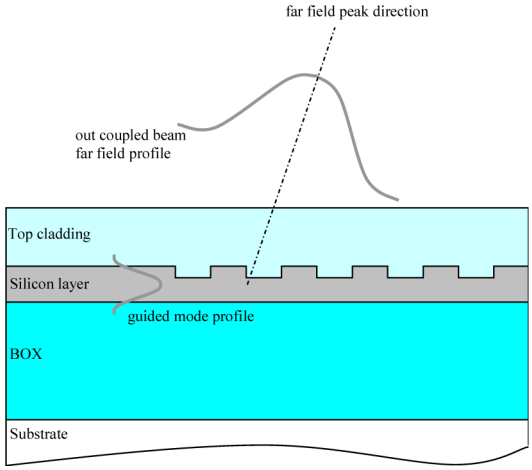

Fig. 11. Illustration of a grating coupler layers with the guided-mode profile and the out-coupled beam from the waveguide toward the fiber through the grating.

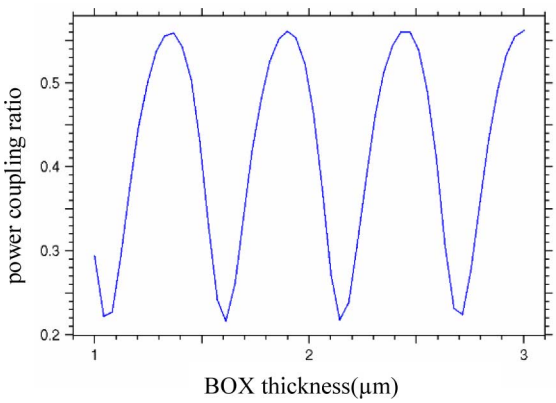

Fig. 12. Illustration of a grating coupler efficiency variation according to the BOX thickness.

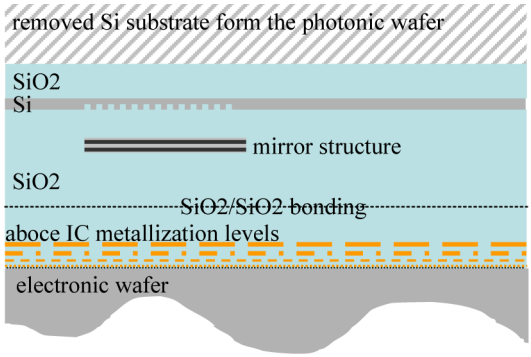

Fig. 13. Illustration of the face-down grating coupler and its mirror below after the photonic layer integration onto the electronic wafer.

are made on a SOI substrate. The silicon structure is sandwiched between a thick SiO_2 buried oxide (BOX) layer and a thinner SiO_2 CVD cladding (see Fig. 11). At the grating level, the silicon layer is partially etched by a RIE process after a DUV 193 nm optical lithography.

If we focus on 1-D grating, some parameters can be given analytically according to the following formula. First, the grating period is optimal for the TE mode coupling at a given wavelength λ and a coupling angle θ with respect to the vertical according to the phase-matching condition

$$k\sin(\theta) + p\frac{2\pi}{\Lambda} = \beta \tag{1}$$

where $k = 2\pi/\lambda$ is the modulus of the out-coupled wave vector, p is the diffraction order, Λ is the grating period, $\beta = (2\pi/\lambda)n_{\text{eff}}$ is the real part of the propagation constant, and n_{eff} is the mean effective index along one grating period.

Using typical photonic SOI wafers with 220-nm-thick silicon layer [14], state-of-the-art of 1-D grating couplers exhibit between 40% to 50% fiber-coupling efficiency [15]. For these optimized designs, the BOX layer thickness is optimized in order to generate constructive reflection from the silicon substrate of the transmitted beam through the grating. This contribution may also be enhanced by increasing the reflection ratio using a bottom mirror, such as a single-metallic layer or a multilayer Bragg mirror [6], [16], [17]. Anyway, the oxide thickness between the silicon grating and the reflective surface underneath appears to be a very sensitive parameter, as a not adapted value may reduce the fiber-coupling efficiency by a factor of more than 2 (see Fig. 12).

We can note as a rule of thumb that 80% of the maximal value is reached for a BOX thickness precision of less than 100 nm from the optimal value. With current SOI fabrication processing, the BOX layer thickness is very accurate with, for instance, 2 μm $\pm$ 50 nm. Such a fabrication tolerance has then no significant effect on the grating performance: it leads to a fiber coupling decreasing of less than 2% and a coupling angle variation of less than 1° [18]. However, when considering the 3-D integration of the photonic layer above a IC layer at the last levels of metallization, neither the oxide thickness nor the substrate reflectivity under the grating coupler can be expected to be optimal (see Fig. 3). This way, the photonic layer integration may strongly reduce the fiber-coupling performance.

In order to overcome this issue, we present a ready to wafer-bonding fiber grating design. In this approach, a grating bottom mirror in made at the photonic layer by anticipating the structure flip. In this approach, the mirror is first made above the encapsulation layer of the fiber grating coupler in order to appear below it after the optical layers integration onto an IC wafer [19]. Indeed, after the substrate removing at the photonic wafer side, the optical structures appear then face down when compared with the initial fabrication (see Fig. 13). This way the thickness between the grating and its bottom mirror, which is a very sensitive parameter, remains under control whatever the wafer-to-wafer bonding process tolerances. Indeed, the bottom mirror reflectivity remain under control whatever the electronic layers or the interconnect layers are below.

The initial grating, we model in 2-D finite-difference time domain (FDTD), is based on a 220-nm-thick silicon core sandwiched between silica layers, the grating period is $\Lambda = 632$ nm and the partial etching depth is 70 nm: the optimal angle at 1550 nm is then 14° in the air with a fiber-coupling ratio of 40% for no layer at all and a nonreflective surface below. The very first structure, we have experimented, is a single 100-nm-thick

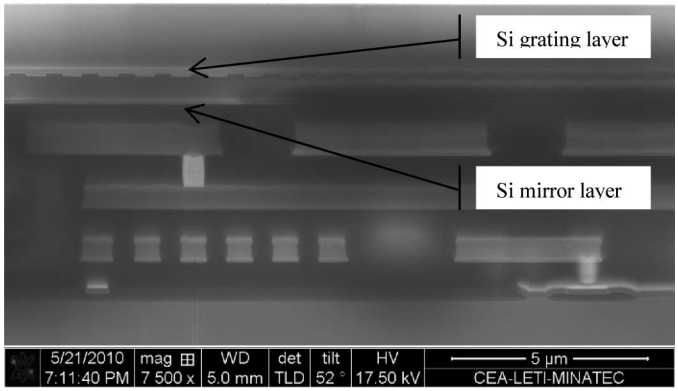

Fig. 14. Picture of a flipped grating coupler with its bottom mirror above several metallic layers.

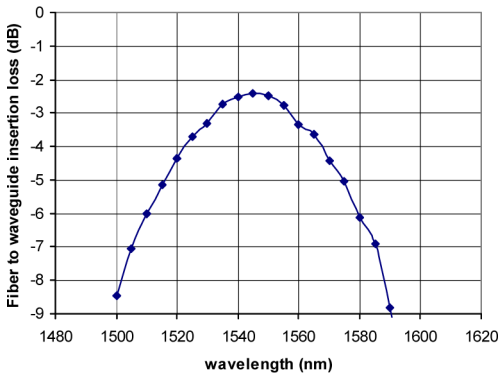

Fig. 15. Measured fiber to waveguide insertion loss of a grating integrated on CMOS with a silicon single-layer bottom mirror.

silicon layer as a bottom mirror below 800 nm of silica below the grating. Below this structure, we can find several metallic layers (see Fig. 14).

In this configuration, the theoretical fiber- to waveguide-coupling ratio increases to 64% corresponding to about 2 dB insertion loss. Experimentally, we have reached less than 2.5 dB insertion loss at 1550 nm in the TE mode (see Fig. 15). This efficiency level value has been extracted from the measurement of the fiber-to-fiber transmission through a circuit with inputand output gratings connected by a $500 \times 220\ \mu m^2$ silicon wire. The measured propagation losses of the silicon wire are 2.2 dB/cm.

We have then demonstrated how to make a grating-based coupler that can anticipate the wafer-to-wafer photonic layers integration in order to be insensitive to metallic levels underneath. Our next developments on this approach will consist in improving the reflectivity of the bottom mirror in order to increase the grating efficiency. For instance, we will consider two kinds of silicon bottom mirrors: multilayer Bragg mirror and grating single-layer mirror.

The multilayer Bragg approach has been efficiently demonstrated by Selvaraja *et al*. [20] with a nonflipped integrated grating reaching experimentally about 69% fiber-coupling efficiency. In our design, considering a quasi-normal incidence at 1550 nm, the quarter wavelength thicknesses of the silicon and silica layers correspond, respectively, to 111 and 269 nm. By optimizing the oxide thickness between the grating and the first Bragg mirror silicon layer to 1.3 μm, we calculate an optimal fiber-coupling ratio of 75% for three silicon layers. It is interesting to observe that this ratio decreases down to 70% for two silicon layers and 64% for one silicon layer to be compared with 40% for no layer at all and a nonreflective surface below.

Even if it should be very efficient, a three-layer mirror may complexify very much the fabrication process as it is a rather thick structure with six silicon and silica layers coating that may require to be removed beyond the grating coupler area. If at normal incidence, the reflection ratio of a single-quarter wavelength thick silicon layer embedded into silica is limited to about 50%, this reflectivity may be increased to almost 100% by implementing a subwavelength grating structure. Theoretically, we find that by implementing a 950-nm period grating in a 130-nm-thick silicon layer as bottom mirror, the optimal fiber-coupling ratio should be again in a range over 75%. It corresponds to the optimum found previously for a three-layer Bragg bottom mirror with a simplified fabrication process flow.

IV. Chip Packaging

Like for nonintegrated optoelectronic devices, packaging of CMOS photonic devices is a keypoint to be considered when designing a component that intend to be connected to an optical fiber network. It is all the more critical than CMOS photonics mainly targets mass production devices. As a result, CMOS photonics devices cannot withstand being packaged at the same cost level as legacy devices (e.g., telecom laser diode modules), for which packaging hold for 80% of the overall cost of the product. The target for CMOS photonics-packaging architecture is to get closer to the microelectronic industry model, i.e., around 20% of the overall cost for packaging [21], [22]. Moreover, additional characteristics should be taken into account: high number of electrical inputs/outputs, good thermal resistance, low-profile geometry (intended to be mounted on an electronic board), compatibility with high-speed data rate up to 40 Gb/s, and finally, high-efficiency optical coupling.

A. Package

In order to achieve these goals, the package itself has to shift from expensive Kovar hermetic packages [23] used for telecom laser diode modules to microelectronic Joint Electron Devices Engineering Council (JEDEC)-style package, like ceramic pin grid array package [24] (see Fig. 16) or leadless chip carrier [25].

Recently, quad flat no leads (QFN) air cavity package (see Fig. 17) has also been implemented in order to package an SOI-based Ge-on-Si high-speed photodetector [26]. This type of package exhibits bandwidth that could enable the packaging of integrated device with high I/O count (32 or more) and high-bandwidth characteristics (20 GHz or more). This is not a hermetic package, as it is assumed that targeted application will not specify reliability level as high as telecommunication standards, and because the structure of CMOS photonic devices itself can withstand to be packaged with low-permeability package, as the active area of the devices are not directly exposed like in InP laser diode modules.

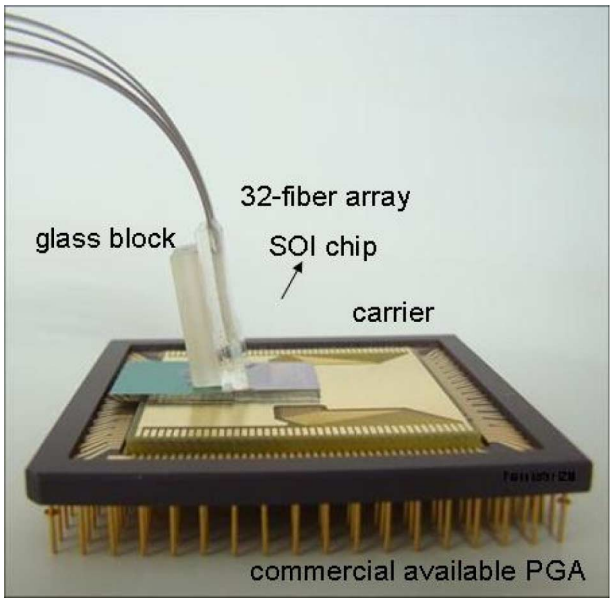

Fig. 16. gPack ceramic pin grid array package.

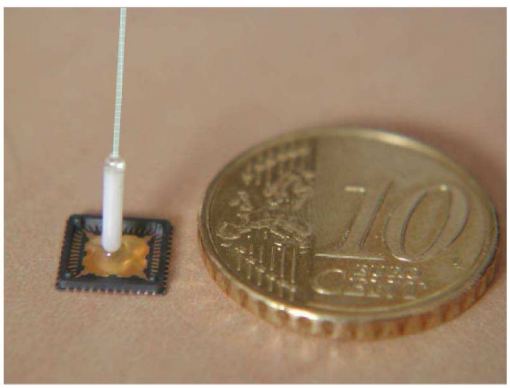

Fig. 17. Pigtailed optical high-speed receiver, embedding a Ge-on-Si photodiode and related electronics in a QFN package multichip module.

B. Optical-Coupling Configurations

Even if demanding in term of high-frequency characteristics, designing the optoelectronic IC (OEIC) case is actually not the most challenging part. Indeed, optical-coupling architecture and assembly definitely remains the key point in order to achieve high-yield low-manufacturing cost components.

This was already the case for legacy telecom laser diode modules, and solutions have been extensively described in the literature [27], [28]. It is well known [29] that two main strategies are used to achieve optical alignment.

1) Active alignment, combined with laser welding, is widespread in the field of telecom laser diode modules, but has also been implemented in InP-based photonic ICs [30]. In this later case, a lensed fiber is aligned and attached at a given working distance from the optical output of an integrated dense WDM (DWDM) transceiver. This kind of process is a noncollective process, time-consuming especially when a multiple fibers have to be connected to an array of output optical ports. However, it has been implemented in various integrated optics devices using a butt-coupling architecture (a flat cleaved optical fiber or a multifiber ferrule is attached to the optical plane using optical adhesive). For example, company Kotura has demonstrated PLC-based devices using this kind of architecture [31].
2) Passive and self-alignment are promising strategies in term of throughput and cost, and multichannel compatibility. However, it leads to lower mean performances because mechanical tolerances statistically combine to get the final distribution of the optical-coupled power. This technology, involving microelectromechanical systems (MEMS) processes, like silicon wet etching, has mainly been implemented for low-cost devices like access and datacom modules [32], including PLC-based diplexers [33].

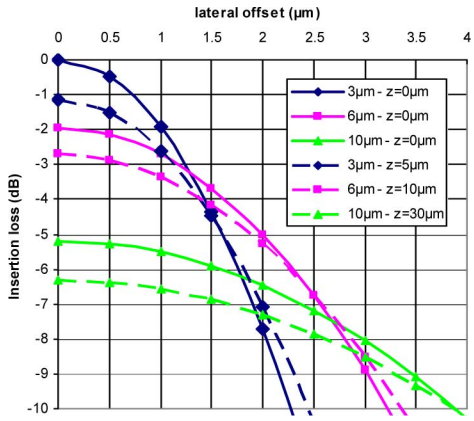

Fig. 18. Insertion loss and alignment tolerances between a diameter 3 μm MFD and a beam with 3 6, or 10 μm MFD.

Whatever the optical-coupling strategy is, alignment tolerances are obtained from the values of the mode-field radii (MFR) in the X- and Y-axes of the optical output coupler and from the mode-field radius of the fiber (e.g., 5.2 μm at 1550 nm for a standard flat cleaved SMF).

One can easily evaluate the theoretical coupling losses and related tolerances using classical formulas, and assuming Gaussian modes. Considering a 3×3 μm MFD in the output plane of the SOI chip (case of a state-of-the-art inverted taper), the optimum coupling ratio is expected to be close to –5 dB when coupled to a flat-cleaved standard SMF, at wavelength 1550 nm, with 1-dB attenuation radial tolerance of ± 1.75 μm. When using a lensed fiber with matched MFR toward the 3×3 μm MFD beam, one can observe (see Fig. 18) that the expected coupling ratio, theoretically, increases to 100% (neglecting Fresnel losses and any misalignment of the lens to the fiber axis), and the alignment tolerances drop to ± 0.75 μm, leading to delicate alignment processes.

Considering an output grating coupler with a MFD is around 10 μm, the expected 1-dB-loss radial tolerance becomes ± 2.5 μm. Figure 19 illustrates various tolerance curves for various gap values between a typical output grating coupler and a standard flat cleaved SMF.

This level of tolerances has been experimentally obtained on gratings (see Fig. 20). Alignment tolerances are usually

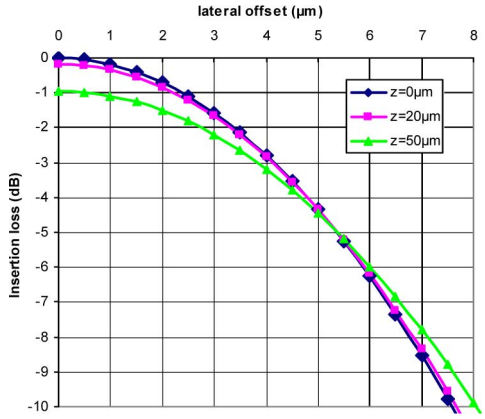

Fig. 19. Insertion loss and alignment tolerances between a diameter 10 μm MFD and a standard SMF.

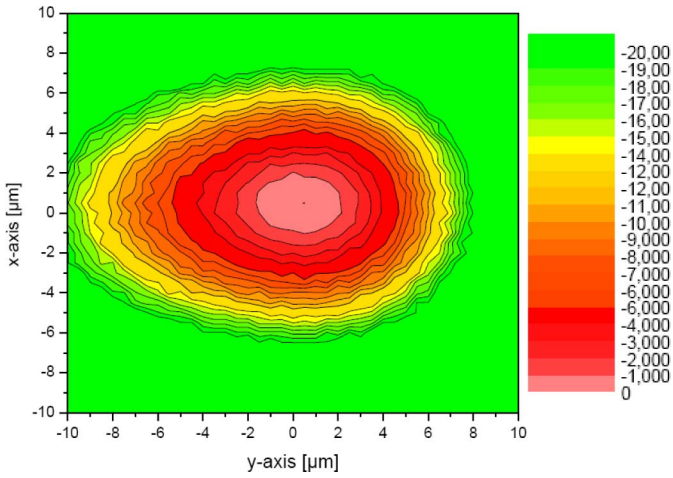

Fig. 20. Measured fiber to waveguide insertion loss (in dB) tolerance through a surface grating coupler.

calculated on the basis of a pure x- or a y-displacement. However, one cannot avoid having misalignment in x-AND in y-direction. Therefore, the tolerances in x- and y-alignment drop by (approximately) a factor of 2. For example, in case a 1 dB drop is observed for a misalignment of 1 μm, one needs an alignment process, which manages better than about 0.5 μm in x-direction and about 0.5 μm in y-direction. This only underlines how easily submicrometer precision is required for a spotsize smaller than SMF.

As a conclusion, coupling architectures relying on inverted tapers (lateral coupling) suffer from two main drawbacks: submicronic alignment tolerance, leading to difficult multichannel alignment and precise preparation of the edge of the die (e.g., by use of optical quality polishing) leading to additional manufacturing costs. On the other hand, grating vertical structures show some benefits, such as good mode matching with SMF, leading to alignment tolerance of ± 1 μm, on-wafer test capability, and capability to be coupled with multichannel fiber arrays [34], [35].

In spite of this advantageous mode-matching property, there are some drawbacks in the use of vertical couplers. First of all, they are limited in term of bandwidth. For a given design based on a nominal wavelength of 1525 nm, expected 1 dB bandwidth is 1500–1550 nm typically [15]. Moreover, 1-D grating are polarization sensitive: they behave as polarization filter. However, 2-D gratings can be used to solve this problem [36].

TABLE I
ADVANTAGES AND DRAWBACKS OF COUPLING ARCHITECTURES.

	Lateral (inverted taper) [12, 13]	Vertical (Grating coupler) [15, 20]
Coupling loss to SMF (flat cleaved fiber, butt coupled)	-7dB (single stage) -1.5 dB (double stage)	-4.5 dB (standard grating) -1 dB (optimized grating)
Coupling loss to SMF (lensed fiber)	-1.5 dB (best) -3 dB (typical)	
1dB tolerance (radial offset)	+/- 0.3 µm (single stage)	+/- 2µm
3 dB bandwidth	Broadband	60 nm
Polarization dependance	Weak	Strong
Suitable for multiple I/O	No	Yes

Pros and cons of these two main architectures are summarized in Table I.

In addition, it may be required to keep the output fiber in the chip's plane, in order to get low-profile components. Thus, if vertical grating are used, an additional optical part needs to be assembled in order to rotate the beam perpendicularly to the grating output axis. This can be done by using a reflector part, e.g., a microferrule including a cleaved optical fiber and a mirror, or a waveguide with a 45° polished tip [37].

C. Advanced Packaging

As mentioned earlier, passive alignment is an alternative way to achieve low-cost mass production compatible assembly processes. It requires accurate mechanical-guiding structures obtained by various MEMS processes, like silicon wet etching or polymer patterns. With the aim to achieve waveguide alignments, we call these techniques "advanced packaging." Such a typical approach has been described in [38]. In this study, an SOI optical chip with waveguide made of silicon (oversized rib waveguide) is considered. The MFD at the output of the chip is close to 10 μm. The SOI chip is passively coupled to a standard SMFs array set in wet-etched v-grooves on a silicon bench. Silicon wet-etched structures (rib–grooves combinations) serve as mechanical standoffs. They are structures on the silicon bench and on the optical chip, the later being the exact negative of the first, allowing the optical chip to be flip-chipped on the silicon bench, with aligned optical axis.

This architecture is made possible for edge-emitting optical chips because MFD allows positioning tolerance of 2 μm, compatible with silicon wet-etch process.

A very similar architecture has been proposed by De Labachelerie *et al.* [39] with "mushroom" structures machined

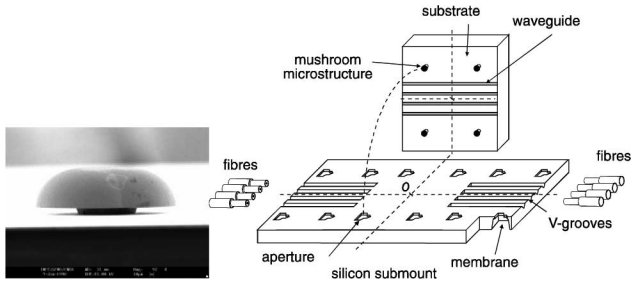

Fig. 21. Principle of the fiber to waveguide coupling by mechanical clip on and flip-chip technique onto a silicon submount, and SEM view of the mushroom structure.

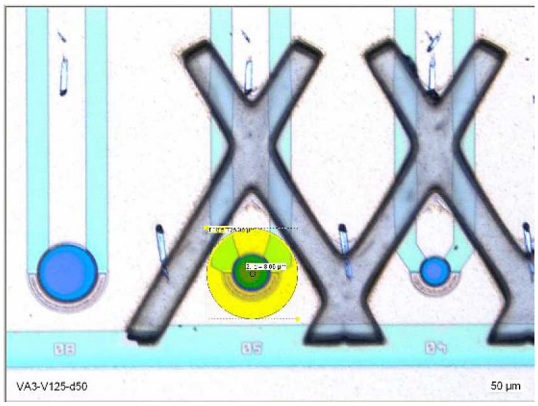

Fig. 22. V-shaped dry film structures processed onto a SOI photonic device (Ge-on-Si photodetector) enabling a fiber to be passively aligned. Yellow circle symbolizes fiber final position.

on the optical chip (see Fig. 21). These mushroom structures can be mechanically inserted into apertures obtained by combining KOH wet etching and RIE of silicon. The alignment accuracy of ± 2 μm has been reported.

It should be noted, however, that these two solutions require some space to be allocated on the optical chip in order for the alignment structures to be built. For CMOS photonics devices, this is a drawback because the area of the chip has to be kept as low as possible, and because complicated processes should be avoided.

In the case, the optical output is vertical, polymer structures obtained by patterning of dry-film photoresist has been applied to SOI optical devices. Total dispersion of such a process has been demonstrated to be ± 2 μm [40], and is thus compatible with fiber alignment with grating, as described in Fig. 22. Fiber is inserted in "v" shaped structures of polymer, for which a 100-μm thickness is sufficient to achieve passive alignment of a fiber or an array of fibers.

V. Conclusion

Recent developments have demonstrated the interest of silicon photonics technology to implement several optical and optoelectronic functions in tiny chips. This footprint reduction and the use of microelectronics fabrication lines make then this approach fully compatible with on-CMOS integration at wafer level. This integration can be considered as the very first level of the packaging technologies of silicon photonic circuits. Then, innovative packaging and integration technologies must be considered in order to jump from photonics- to electronics-packaging ratio cost models.

We have seen how the photonic circuit layers can be integrated at wafer level with electronics circuit layers. Each approach may require different electrical interconnect technologies and may lead to the use of different fiber-coupling structures. However, as they exhibit very complementary performances and alignment tolerances, the targeted application will also contribute to the fiber coupler selection.

Finally, current silicon photonics circuits can, of course, be integrated in current packages that have been developed for planar optical IC. But this photonic packaging that includes optical fibers pigtailling remains very expensive. In order to be compatible with mass production at low cost, advanced-packaging approaches may be developed by integrating MEMS-like features at wafer-level above the photonics layers. Packaging technologies for optoelectronic and nanophotonic at chip level requires integrated technologies at wafer level.

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