CMOS Compatible Integrated Dielectric Optical Waveguide Coupler and Fabrication

Jeong-Min Lee
(minlj@tera.yonsei.ac.kr)

High-Speed Circuits and Systems LAB.
Information

- Name: CMOS Compatible Integrated Dielectric Optical Waveguide Coupler and Fabrication
- Date of Patent: Jun 15, 2010
- Inventors: Solomon Assefa
- Assignee: IBM
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Background of the Invention

- Integrated semiconductor devices that include one or more photonic devices: Photodetectors, Modulators, and Optical switches
  - Require a mechanism to couple optical signals between the optical fibers and the silicon based waveguides

- Coupling from an optical fiber to a photonic device with input and output waveguides often suffers from loss due to index and mode-profile mismatches
  - Polymer couplers
    - Technique used to minimize losses in coupling
    - Provide effective matching

- Optoelectronic circuits (fabricating CMOS) → Fabricating polymer couplers for use → photonic devices need to be encapsulated and annealed as CMOS-compatible processes
Summary of Invention

- This invention provides a method for encapsulation of the devices and the formation of the couplers → Performance is not affected.

- This invention provides a CMOS compatible method:
  - Thermal treatment
  - Electrical activation
  - 3D integration of optical devices

- This invention allows an efficiently manufactured semiconductor device that integrates photonic devices with CMOS circuit devices.
Fabrication Process

1. Accept a semiconductor device with an Integrated Optoelectronic circuit and at least one waveguide (Fig. 1)
2. Depositing a lower SiN layer, an SiON layer, a DLC layer and an upper SiN layer (Fig. 1)
3. Deposit photo-resist layer with an etching area defining an optical wave guide coupler fabrication area (Fig. 1)

4. Etch a portion of the upper SiN layer under the etching area (Fig. 2)
   ✓ DLC: CMP Stop Layer
5. Remove the photo-resist layer and a portion of the diamond like carbon (DLC) layer under the etching area (Fig. 3)
6. Etch the SiO2 layer to at least the lower SiN layer (Fig. 4)
Fabrication Process

7. Depositing an SiON layer onto the semiconductor die (Fig. 5)
8. Perform CMP to remove the SiON layer not within the etching area and the upper SiN layer (Fig. 6)

CMP: Chemical Mechanical Polishing
9. Etch the DLC layer to leave the SiO2 layer and SiON transition layer (Fig. 7)

10. Semiconductor die that has been cleaved along cleave line to expose an exposed face of the SiON coupler (Fig. 8)

11. An optical fiber is attached to the exposed face of the SiON coupler
Conclusion

- This invention provides a method for encapsulation of the devices and the formation of the couplers

- Polymer couplers
  - Low losses in coupling
  - Provide effective matching

- Photonic devices need to be encapsulated and annealed as CMOS-compatible processes
Thank you for listening

Jeong-Min Lee
(minlj@tera.yonsei.ac.kr)

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