SPECIAL TOPICS IN COMPUTER ARCHITECTURE AND VLSI DESIGN:
Overview of Data Converters

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Related Course

- Mixed-Signal VLSI (EEE 6632): Graduate Course
- Covers Data Converters (ADCs and DACs)

Prerequisites
- Microelectronics II, CMOS VLSI
- Analog VLSI or equivalent (e.g. transistor level circuit design including opamp)
- Prior exposure to Spectre or Hspice
Outline of EEE 6632

- Sampling and quantization
- DAC architecture
- Sample and hold
- Switched capacitor circuits
- Comparators
- Nyquist-rate conversion
- Oversampled conversion
- Limits in accuracy
- Calibration, DEM, and DWA
- Test and specification
Motivation

All electronic systems rely on data converters
Motivation

- ADC / DAC: Interface Between Analog Media and DSP System
- Higher Performance of Data Converters Required
- Trends of SoC Implementation
- Main Bottleneck of Design Time and Resources
**System Design Trend**

- VLSI Design & Tech Improvement
  - More Signal Processing Performed in Digital Signal Domain
  - Implementation Trend: A → B
- Partition Criteria Determined Mainly By
  - Available Design Resources of Analog Front End
    Such as ADC/DAC & ASP (Analog Signal Processing)
  - Required Performance Specifications: (B) > (A)
  - Applications & System Requirements
A/D Converter Application Space
Analog IC Market

<table>
<thead>
<tr>
<th>Company</th>
<th>2011 Rank</th>
<th>2011 $M</th>
<th>2011 Share</th>
</tr>
</thead>
<tbody>
<tr>
<td>Texas Instruments</td>
<td>1</td>
<td>6,524</td>
<td>15.4%</td>
</tr>
<tr>
<td>STMicroelectronics</td>
<td>2</td>
<td>4,177</td>
<td>9.9%</td>
</tr>
<tr>
<td>Analog Devices</td>
<td>3</td>
<td>2,584</td>
<td>6.1%</td>
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<tr>
<td>Infineon Technologies</td>
<td>4</td>
<td>2,073</td>
<td>4.9%</td>
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<tr>
<td>Maxim Integrated Products</td>
<td>5</td>
<td>2,034</td>
<td>4.8%</td>
</tr>
<tr>
<td>NXP Semiconductors</td>
<td>6</td>
<td>1,817</td>
<td>4.3%</td>
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<tr>
<td>Skyworks Solutions</td>
<td>7</td>
<td>1,477</td>
<td>3.5%</td>
</tr>
<tr>
<td>Linear Technology</td>
<td>8</td>
<td>1,324</td>
<td>3.1%</td>
</tr>
<tr>
<td>ON Semiconductor</td>
<td>9</td>
<td>1,133</td>
<td>2.7%</td>
</tr>
<tr>
<td>Renesas Electronics</td>
<td>10</td>
<td>1,107</td>
<td>2.6%</td>
</tr>
<tr>
<td>Others</td>
<td></td>
<td>18,088</td>
<td>42.7%</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td></td>
<td><strong>42,338</strong></td>
<td></td>
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</tbody>
</table>

Ref: iSupply (2010)
Example 1

Source: www.apple.com
Example 1
Example 2

- High performance digital oscilloscopes rely on extremely high performance ADCs
  - Example
    - 20 GSamples/s, 8-bit ADC
    - 10 W Power dissipation

[Poulton, ISSCC 2003]
Example 3

**Inside the M2A™ Capsule**

1. Optical dome
2. Lens holder
3. Lens
4. Illuminating LEDs (Light Emitting Diode)
5. CMOS (Complementary Metal Oxide Semiconductor) imager
6. Battery
7. ASIC (Application Specific Integrated Circuit) transmitter
8. Antenna

![Diagram of M2A™ Capsule components](image)
The Data Conversion Problem

- Real world signals
  - Continuous time, continuous amplitude
- Digital abstraction
  - Discrete time, discrete amplitude
- Two problems
  - How to discretize in time and amplitude
    - A/D conversion
  - How to "undescretize" in time and amplitude
    - D/A conversion
Overview

A/D Conversion

- Analog In
- Anti-alias Filtering
- Sampling
- Quantization
- Digital Out
  - 2, 7, 0, 15, ...

D/A Conversion

- Digital In
  - 2, 7, 0, 15, ...
- DAC
- Analog Hold
- Reconstruction Filtering
- Analog Out
Performance metric of Data Converter

- Number of Bits
- Data Conversion Rate
- Power Dissipation / Hardware Area
- Static Parameters
  - Gain & Offset Errors
  - Non-Linearity: DNL (Differential), INL (Integral)
  - Non-Monotonicity, Missing Codes
- Dynamic Parameters
  - SNR (Signal-to-Noise Ratio)
  - THD (Total Harmonic Distortion)
  - SNDR (Signal-to-{Noise+Distortion} Ratio)
  - ENOB (Effective Number of Bits)
  - Signal Bandwidth
Let’s look at Data Sheet

**Features**
- Sample Rate: 250Msps
- 65.4dB SNR
- 78dB SFDR
- 1.2GHz Full Power Bandwidth S/H
- Single 2.5V Supply
- Low Power Dissipation: 740mW
- LVDS, CMOS, or Demultiplexed CMOS Outputs
- Selectable Input Ranges: ±0.5V or ±1V
- No Missing Codes
- Optional Clock Duty Cycle Stabilizer
- Shutdown and Nap Modes
- Data Ready Output Clock

**Description**
The LTC®2242-12 is a 250Msps, sampling 12-bit A/D converter designed for digitizing high frequency, wide dynamic range signals. The LTC2242-12 is perfect for demanding communications applications with AC performance that includes 65.4dB SNR and 78dB SFDR. Ultralow jitter of 95fs RMS allows IF undersampling with excellent noise performance.

DC specs include ±1.0LSB INL (typ), ±0.4LSB DNL (typ) and no missing codes over temperature.

The digital outputs can be either differential LVDS, or single-ended CMOS. There are three format options for
Input/Output Relation

DAC

ADC
Static Errors

Linear Errors: Offset, Gain errors

Non-monotonicity, Missing Codes

→ Non Linear Errors
Static Errors

Differential Non-Linearity (DNL)  Integral Non-Linearity (INL)
Quantization Error (Noise)

Signal Power: \( P_S(f) = \left( \frac{V_{FS}}{2} \right)^2 = \frac{(2^N \Delta)^2}{8} \)

SNR:
\[
\text{SNR} = \frac{P_S(f)}{P_N(f)} = \frac{(2^N \Delta)^2}{8 \Delta^2} = 2^{2N} \cdot \frac{3}{2}
\]

SNR (dB):
\[
\text{SNR (dB)} = 6.02 \cdot N + 1.76
\]

Mathematical expression:
\[
q^2 = \frac{1}{\Delta} \int_{-\Delta/2}^{\Delta/2} x^2 \, dx = \frac{\Delta^2}{12}
\]
Dynamic Errors

\[ SNR = \frac{S}{N} \]
\[ SFDR \quad ENOB = \frac{(SNDR - 1.76)}{6.02} \]

SNDR = \frac{S}{(N + D)}

Amplitude

Dynamic range

Peak SNR

\[ F_s/2 \]
Anti-Alias Filtering

Brick Wall

Attenuation

Ideal AAF

Real AAF
Sampling & AAF

- In order to prevent aliasing, we need 
  \[ f_{\text{sig, max}} < \frac{f_s}{2} \]
- The sampling rate \( f_s = 2f_{\text{sig, max}} \) is called Nyquist rate
- Can tradeoff sampling speed against filter order
- In high speed converters, making \( \frac{f_s}{f_{\text{sig,max}}} > 10 \) is usually impossible, therefore we need fairly high order filters

[v.d. Plassche, p.41]
Classes of Sampling

- Nyquist-rate sampling \((f_s > 2 \cdot f_{\text{sig,max}})\)
  - Nyquist data converters
  - In practice always slightly oversampled

- Oversampling \((f_s \gg 2 \cdot f_{\text{sig,max}})\)
  - Oversampled data converters
  - Anti-alias filtering is often trivial
  - Oversampling also helps reduce "quantization noise"

- Undersampling, subsampling \((f_s < 2 \cdot f_{\text{sig,max}})\)
  - Exploit aliasing to mix RF/IF signals down to baseband
Classification of ADCs

ADC

- Nyquist-rate
  - Flash
  - Two-step
  - Pipeline
  - Successive approximation
  - Algorithmic
  - Dual Slope
  - ...

- Oversampled

- Sigma-delta

  - SC (Switched-Capacitor) implementations
  - CT (Continuous-Time) implementations
Example: Flash ADC

- Fast
  - Speed limited by single comparator plus encoding logic
- High complexity ($2^B-1$ comparators), high input capacitance
  - Typically use for resolution up to 6 bits
Results from Yonsei

- High precision SAR+$\Delta\Sigma$ hybrid ADC
- 20bit resolution, 6ppm INL, 1uV offset, and 6.3uW power
Performance Limits

![SNDR vs BW plot with various data points and trend lines for different years and jitter levels.]
Ideal DAC

- Essentially a digitally controlled voltage, current or charge source
  - Example below is for unipolar DAC
- Ideal DAC does not introduce quantization error!
The Reconstruction Problem

- As long as we sample fast enough, \( x(n) \) contains all information about \( x(t) \)
  - \( f_s > 2 \cdot f_{\text{sig, max}} \)
- How to reconstruct \( x(t) \) from \( x(n) \)?
- Ideal interpolation formula

\[
x(t) = \sum_{n=-\infty}^{\infty} x(n) \cdot g(t - nT_s)
\]

\[
g(t) = \frac{\sin(\pi f_s t)}{\pi f_s t}
\]

- Very hard to build an analog circuit that does this…
Zero-Order Hold Reconstruction

- The most practical way of reconstructing the continuous time signal is to simply "hold" the discrete time values
  - Either for full period $T_s$ or a fraction thereof
- What does this do to the signal spectrum?
- We'll analyze this in two steps
  - First look at infinitely narrow reconstruction pulses
Dirac Pulses

- $x_d(t)$ is zero between pulses
  - Note that $x(n)$ is undefined at these times

$$x_d(t) = x(t) \cdot \sum_{n=-\infty}^{\infty} \delta(t - nT_s)$$

- Multiplication in time means convolution in frequency
  - Resulting spectrum

$$X_d(f) = \frac{1}{T_s} \sum_{n=-\infty}^{\infty} X \left( f - \frac{n}{T_s} \right)$$
Spectrum

- Spectrum of Dirac signal contains replicas of $V_{in}(f)$ at integer multiples of the sampling frequency.
Finite Hold Pulse

- Consider the general case with a rectangular pulse $0 < T_p \leq T_s$
- The time domain signal on the left follows from convolving the Dirac sequence with a rectangular unit pulse
- Spectrum follows from multiplication with Fourier transform of the pulse

\[
H_p(f) = T_p \frac{\sin(\pi f T_p)}{\pi f T_p} e^{-j\pi f T_p}
\]

\[
X_p(f) = \frac{T_p}{T_s} \frac{\sin(\pi f T_s)}{\pi f T_p} e^{-j\pi f T_p} \sum_{n=-\infty}^{\infty} X \left( f - \frac{n}{T_s} \right)
\]

Amplitude Envelope
Envelope with Hold Pulse $T_p = T_s$

\[ \frac{T_p \sin(\pi f T_p)}{T_s \pi f T_p} \]
Example

Spectrum of Continuous Time Pulse Train (Arbitrary Example)

ZOH Transfer Function ("Sinc Distortion")

ZOH output, Spectrum of Staircase Approximation

$\frac{f}{f_s}$
Reconstruction Filter

- Also called smoothing filter
- Same situation as with anti-alias filter
  - A brick wall filter would be nice
  - Oversampling helps reduce filter order
Example: Resistor String DAC

\[ V_{OUT} = \left( \frac{b_0}{2^1} + \frac{b_1}{2^2} + \ldots + \frac{b_{N-1}}{2^N} \right) \cdot V_{REF} = D \cdot V_{REF} \]

- Simple, inherently monotonic
- Small area up to ~8 bits
- Unsuitable for high-resolution, high-speed designs

Resistors: Current Division
Capacitors: Charge Division
Transistors: Current Division
Overview

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