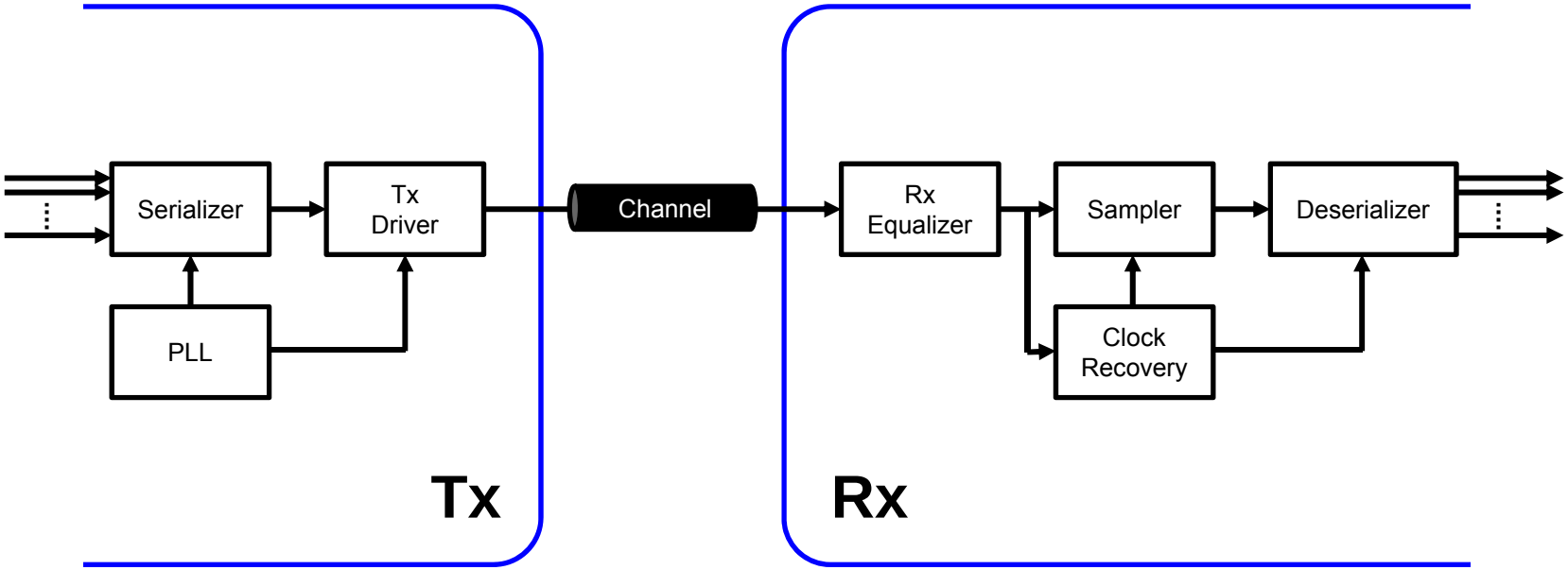
High-speed Serial Interface

Lect. 14 – Clock and Data Recovery (Continuous-mode CDR)

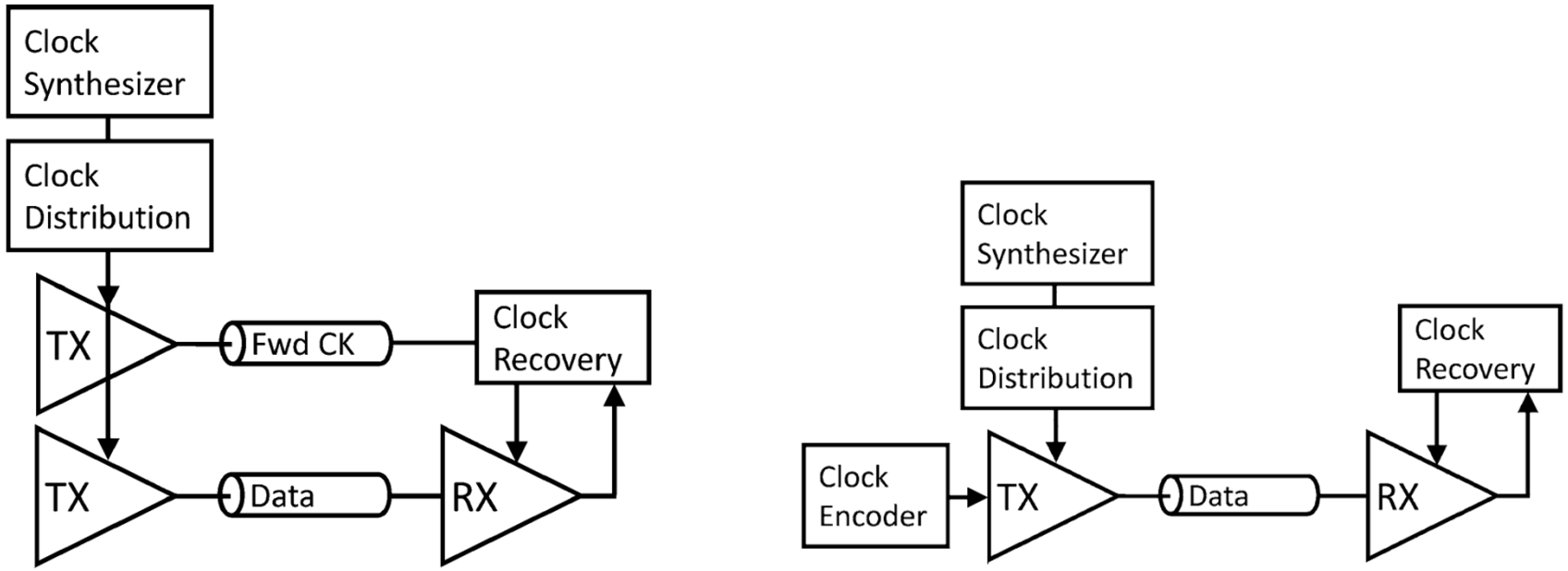
Block diagram

- Where are we today?



Why CDR?

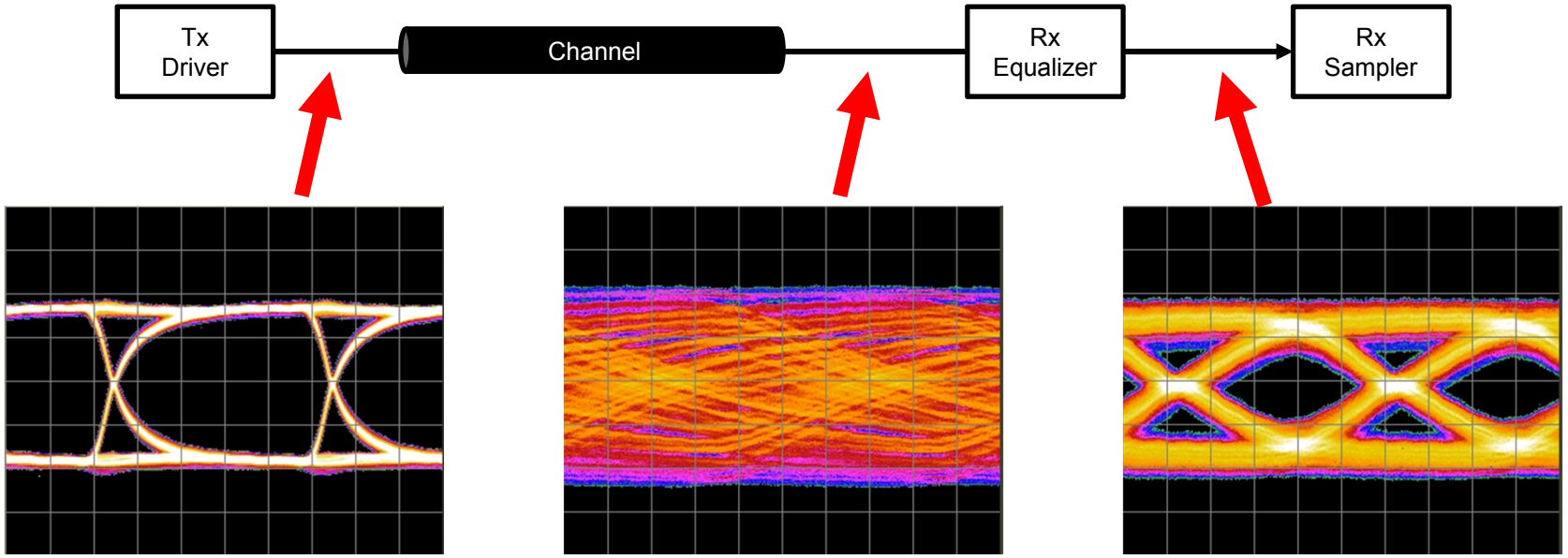
- Clocking architecture for interfaces
  - Forwarded clocking vs. embedded clocking



Bryan Casper - "Clocking Analysis, Implementation and Measurement Techniques for High-Speed Data Links—A Tutorial", 2009 TCAS1

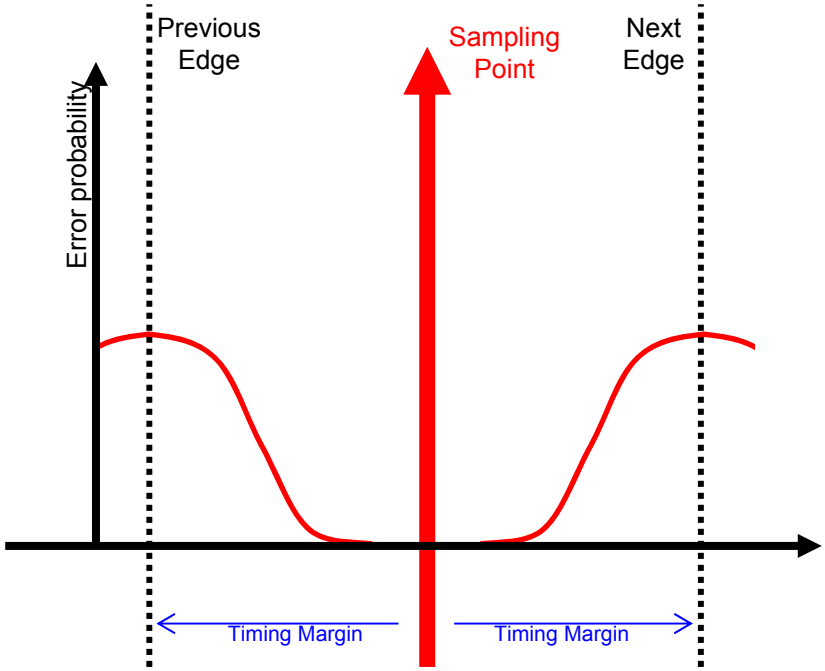
Why CDR?

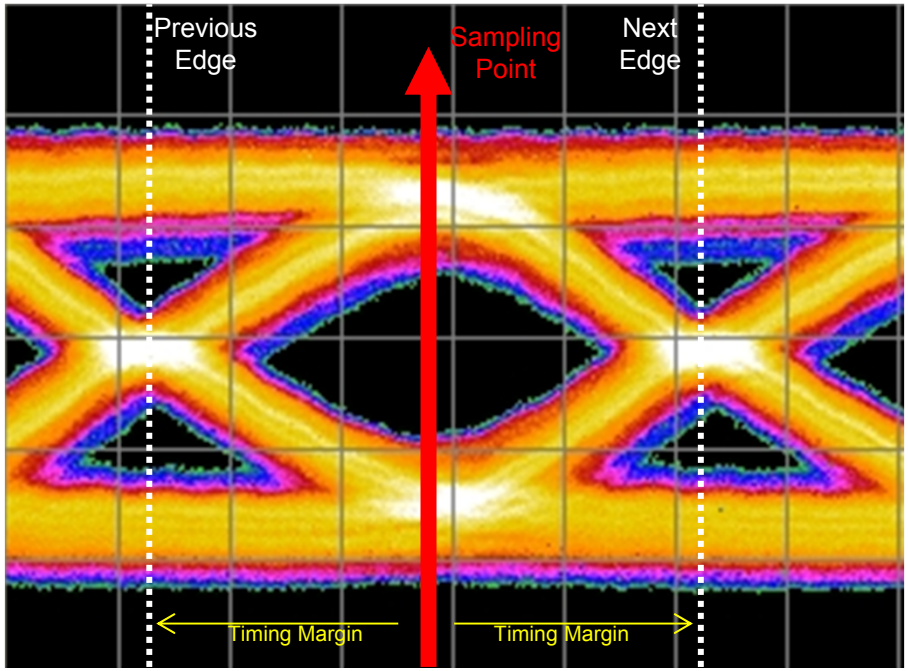
- High-frequency loss in channel causes ISI → closed eye
- Equalizer cannot fully open the eye
- Noises during transmission



Why CDR?

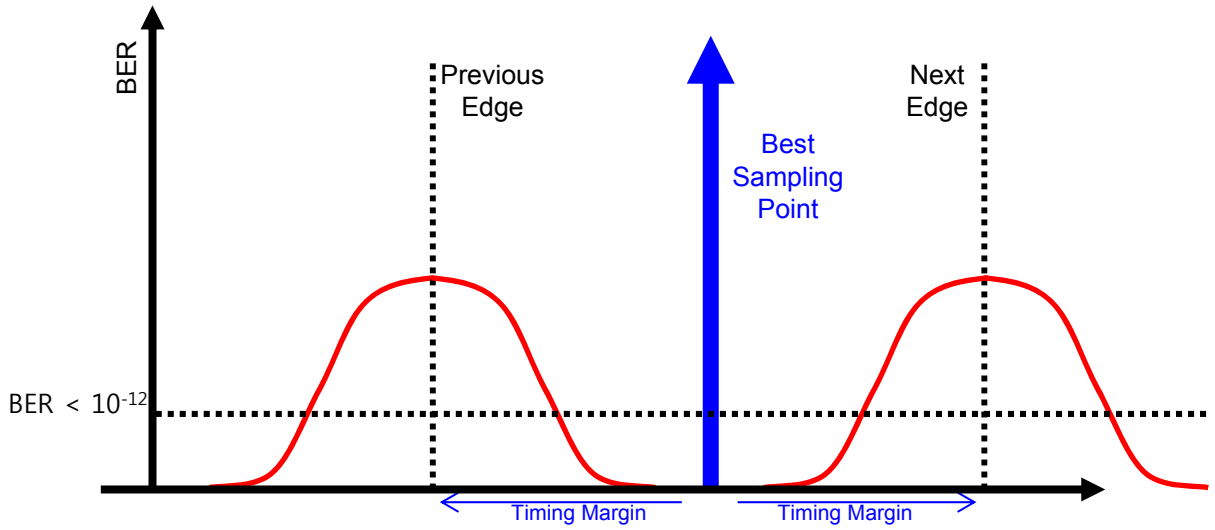
- To find the best sampling point
  - Best sampling point for lowest error probability
  - Depends on noise (jitter) profile





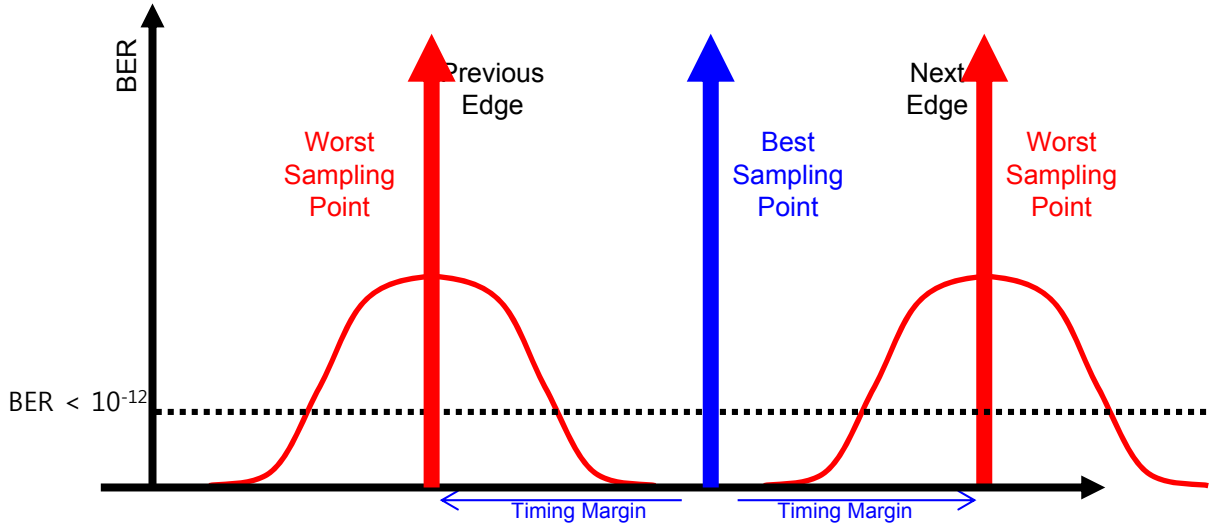
Edge-tracking

- Difficult to find the best sampling point
  - Target BER for HIS: (often) < 10^{-12}
  - BER < 10^{-12} takes long measurement time
    - For 1Gb/s, 1000s > 15min



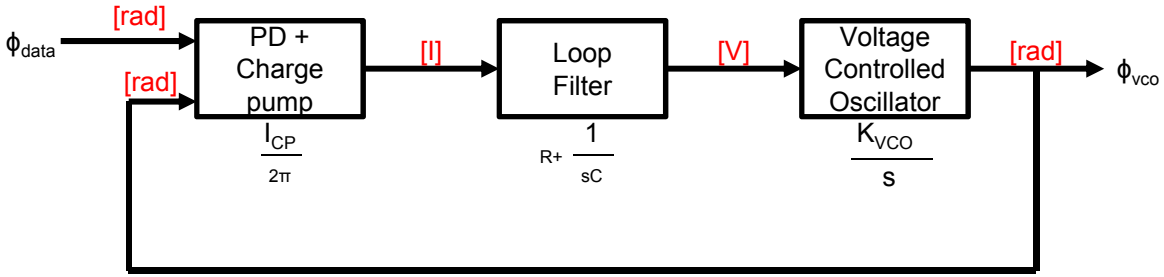
Edge-tracking

- Tracking edges is easier
  - Phase information from transition edges
  - Best sampling point is determined from the edges ➔ middle of two adjacent edges
  - Continuous identical data (CID) sequence affects CDR performance
  - For many applications, balanced coding scheme is employed to guarantee minimum transition
    - For 8b10b coded signaling, probability of transition ~ 50%.



PLL-based CDR

- PLL-based edge-tracking CDR
  - Based on PLL with no divider



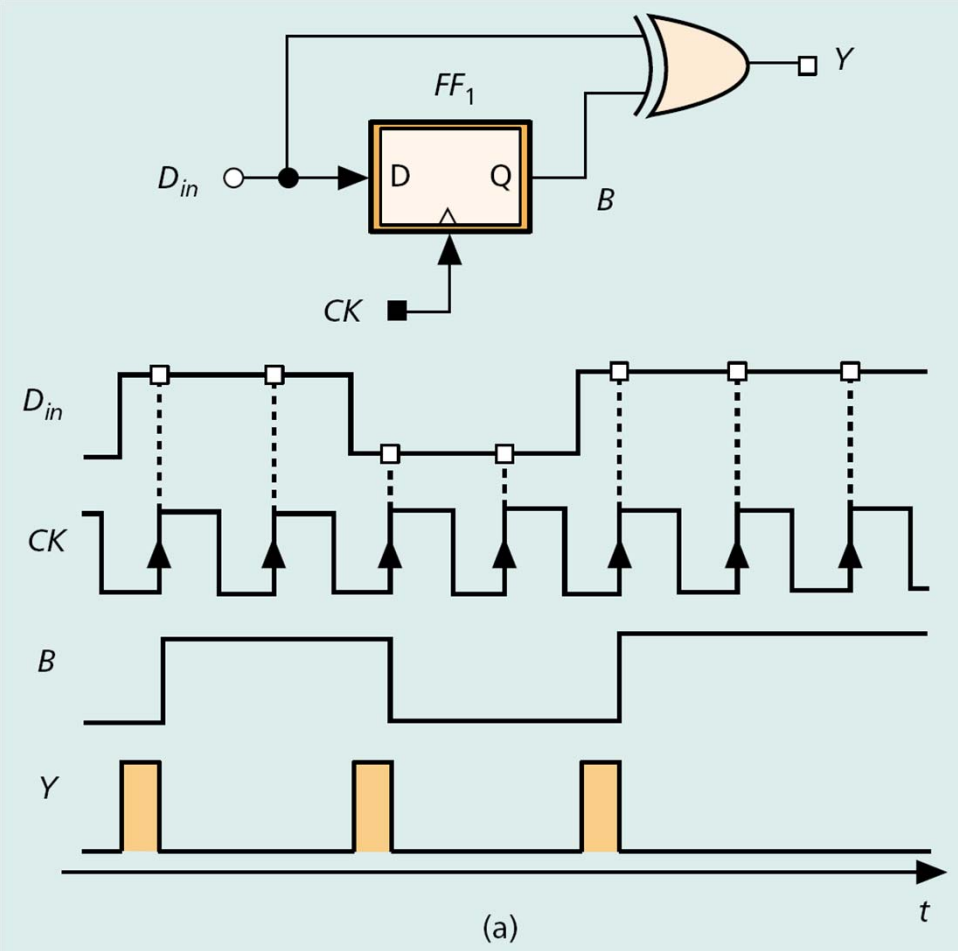
  - Difference in PD
    - PLL: Reference clock
    - CDR: Data
  - PD should detect data transition and phase difference between data and clock

Phase detector

- Linear vs. bang-bang
  - Linear phase detector produces output proportional to phase difference ➔ PLL-like behavior
  - Bang-bang phase detector produces only UP or DN signal corresponding to the sign of phase error.

Phase detector

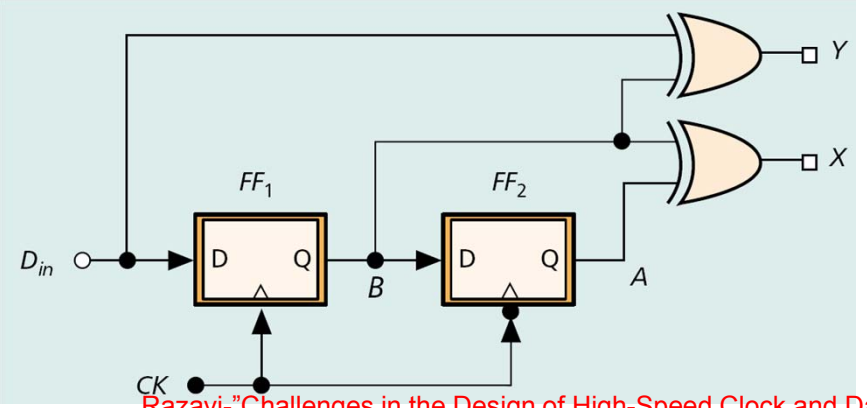
- XOR PD
  - Retimed data (B) compared with input data
  - Phase comparison results produced only when there is data transition
  - Duration of Y: Phase error
  - However, output (Y) shows only positive value
  - Average value of Y depends on transition density
  - Reference pulse with fixed duration when data transition?



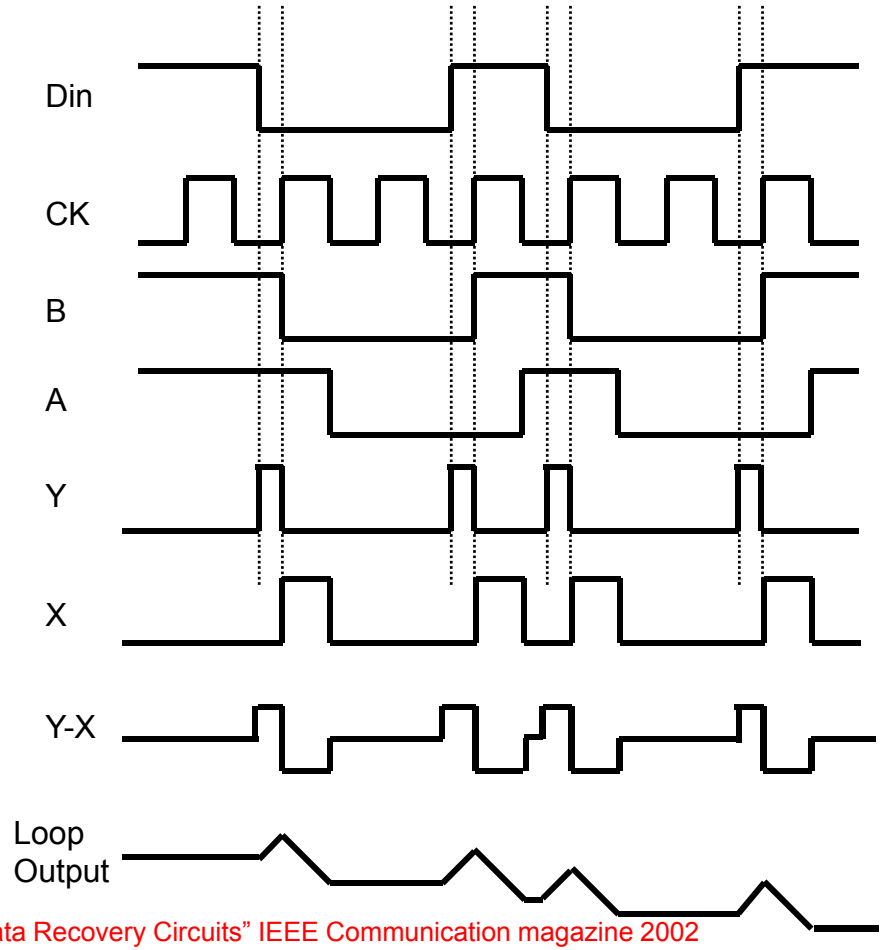
Razavi-"Challenges in the Design of High-Speed Clock and Data Recovery Circuits" IEEE Communication magazine 2002

Phase detector

- Hogge PD
  - Y: Identical to XOR PD output
  - X: Reference signal
    - Duration of half the period when there is data transition
  - Y used as Up and X as Dn for charge pump
  - CK slows down until X and Y have the same duration
  - A, B: Recovered data



Clock earlier than data shown below
Locking achieved when duration of Y equals to duration of X
➔ Clock falling edge is aligned with data edge



Razavi-"Challenges in the Design of High-Speed Clock and Data Recovery Circuits" IEEE Communication magazine 2002

Phase detector

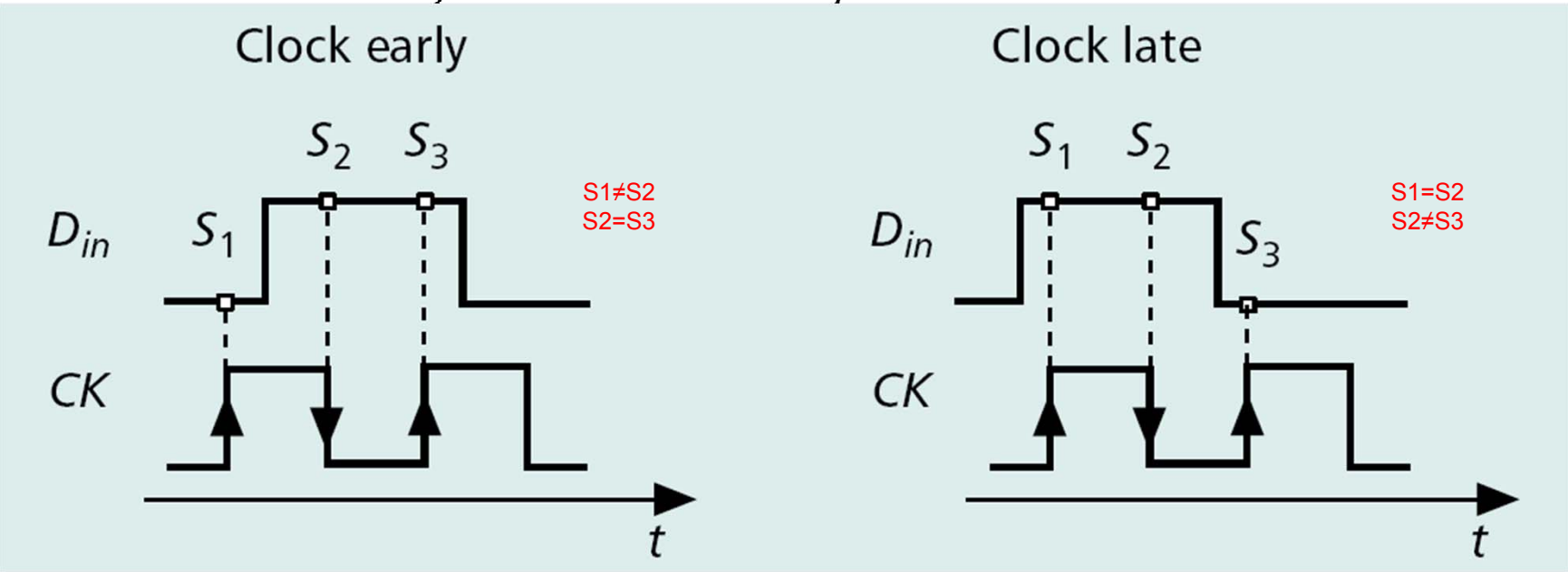
- Limit of linear phase detector
  - Static phase offset
    - Steady-state error in feedback system if open-loop gain is not sufficient
    - Clk-to-Q delay (ΔT) of FF1 results in hardware limited phase offset

    ➔ Y wider by ΔT
  - When locked, charge pump output voltage becomes triangular wave
  - Short pulse generation
    - Pulse width is proportional to phase error.
      - Reference pulse (X) is short (1/2 of data period)
      - With larger phase error, phase error pulse (Y) becomes shorter

      ➔ Distorted pulse shapes in high speed operation

Phase detector

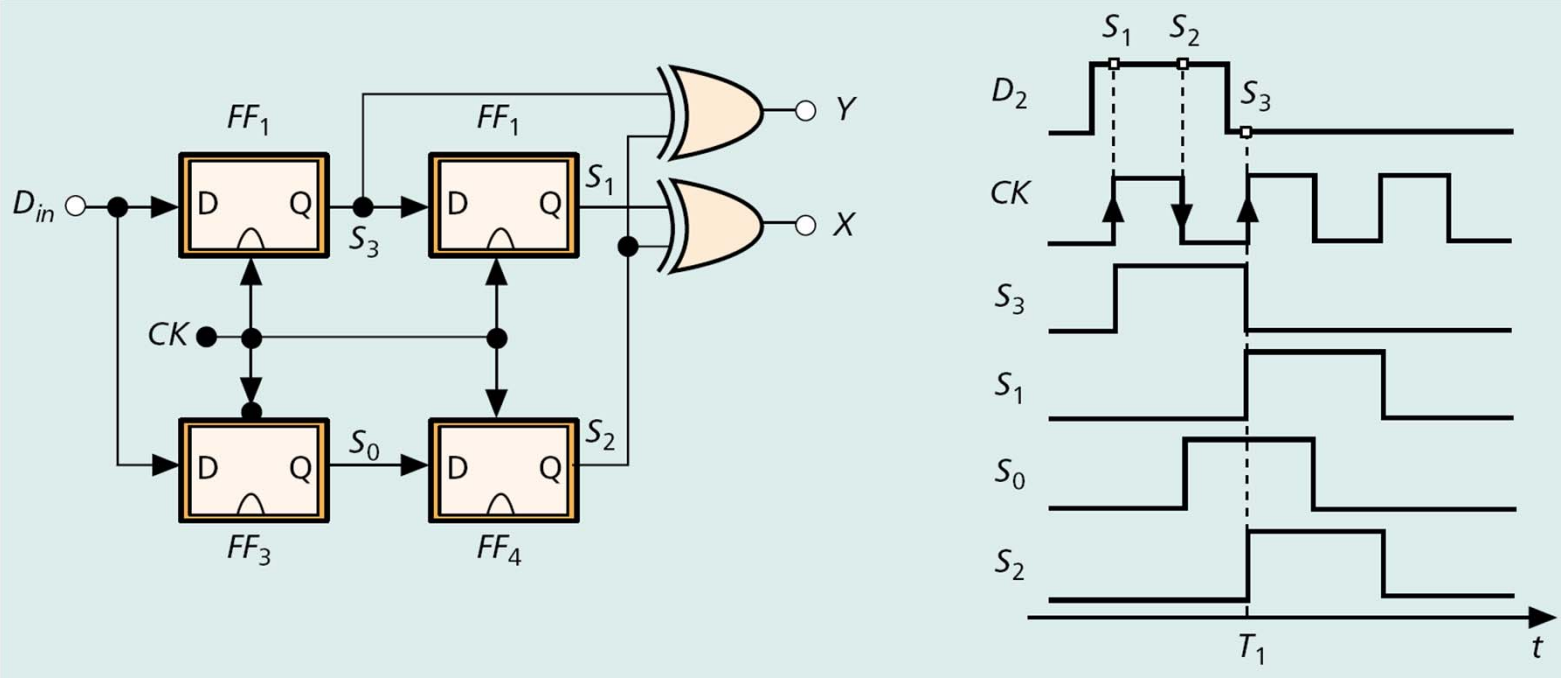
- Bang-bang phase detector
  - Possible to find sign of phase error by 2x-oversampling
    - If two adjacent sampling produces different values, then transition
    - Clock early or late can be easily determined



Razavi-"Challenges in the Design of High-Speed Clock and Data Recovery Circuits" IEEE Communication magazine 2002

Phase detector

- Alexander phase detector
  - FF1 samples at positive edge and FF3 at negative edge



Clock later than data shown above
At T1, Y = S2 XOR S3 ➔ 1
X = S1 XOR S2 ➔ 0
➔ Clock later than data
Y: UP, X: DN

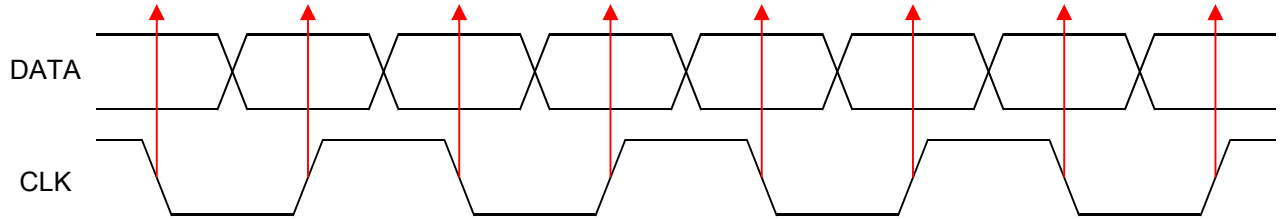
Phase detector

- Advantage of bang-bang phase detector
  - Up or Down pulse width fixed (only when there is data transition)
  - Duration: Two periods
  - PD gain is ideally infinite around $\Delta\phi = 0$
    → no static phase offset in feedback analysis

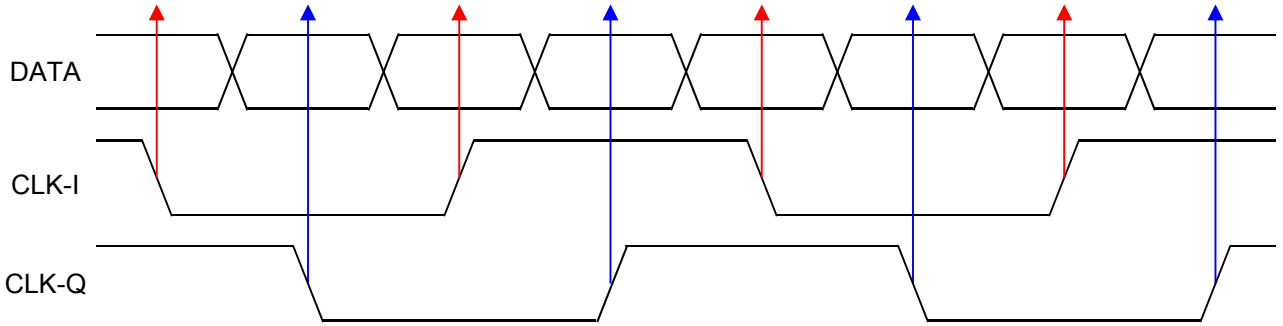
- Disadvantage
  - Simple loop analysis not possible with infinite PD gain
  - In reality, input jitter affects PD gain (SP paper)

Reduced sampling rate

- Reducing sampling rate
  - Half-rate sampling

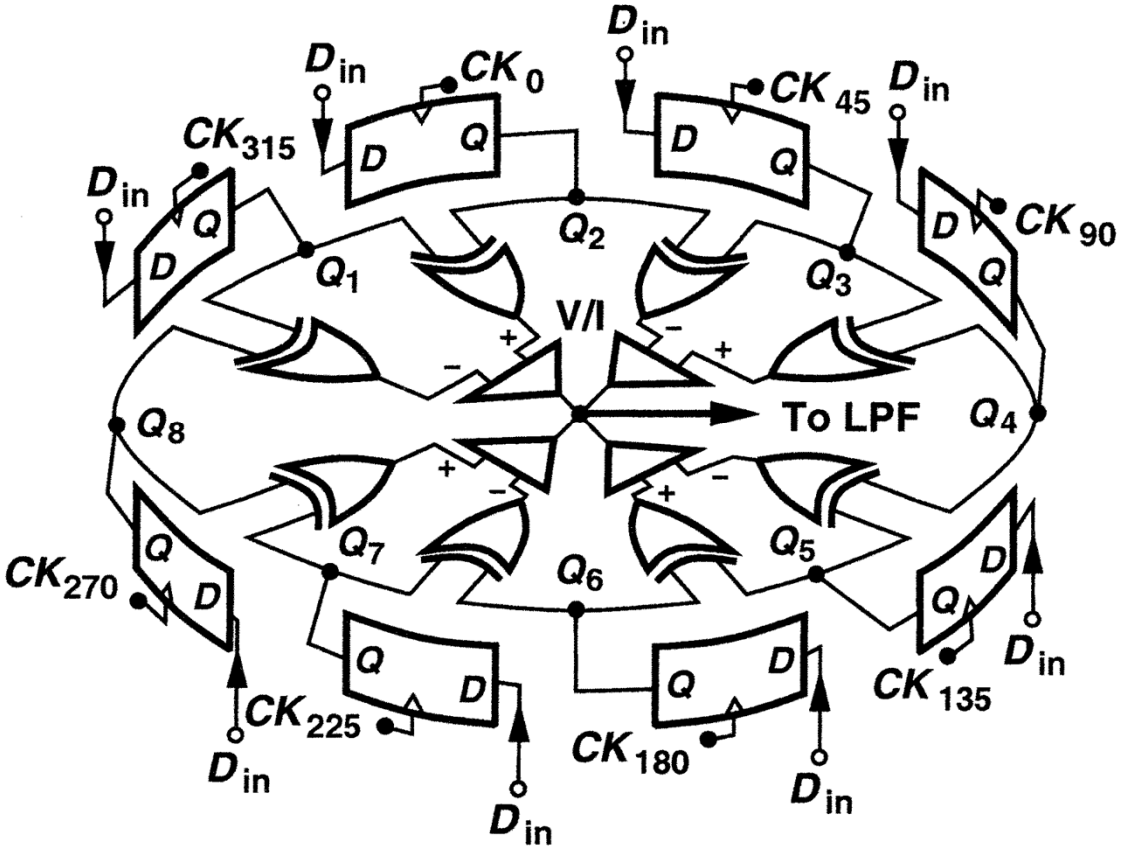


  - Quad-rate sampling



Reduced sampling rate

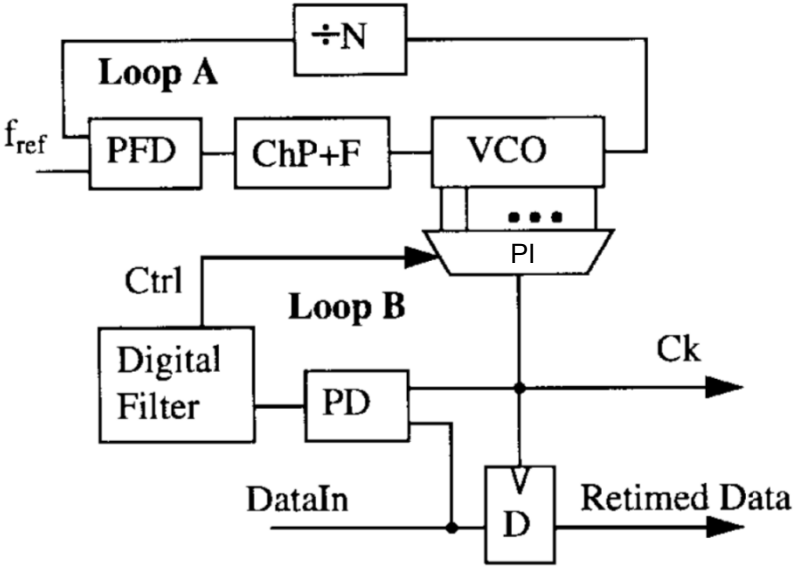
- Quad-rate bang-bang phase detector

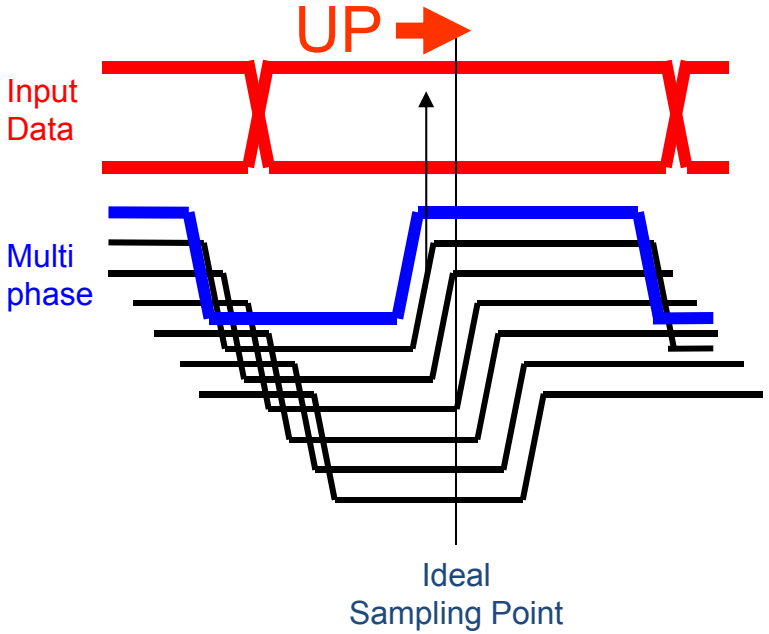


Jri Lee -"A 40-Gb/s Clock and Data Recovery Circuit in 0.18-m CMOS Technology" JSSC 2003 (SP)

PI (Phase Interpolator)-Based CDR

- CDR using PI-based phase controller





-- Generate the correct phase clock signal with several available from VCO

– Large Bandwidth for Loop A → suppress VCO jitter
– Small Bandwidth for Loop B → suppress input jitter

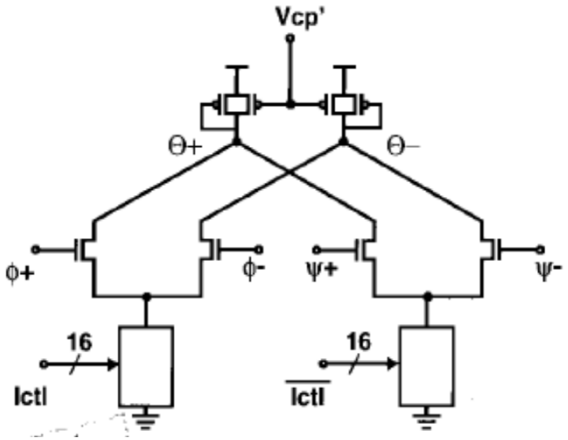
Patrik Larsson-" A 2-1600-MHz CMOS Clock Recovery PLL with Low-Vdd Capability", JSSC 1999

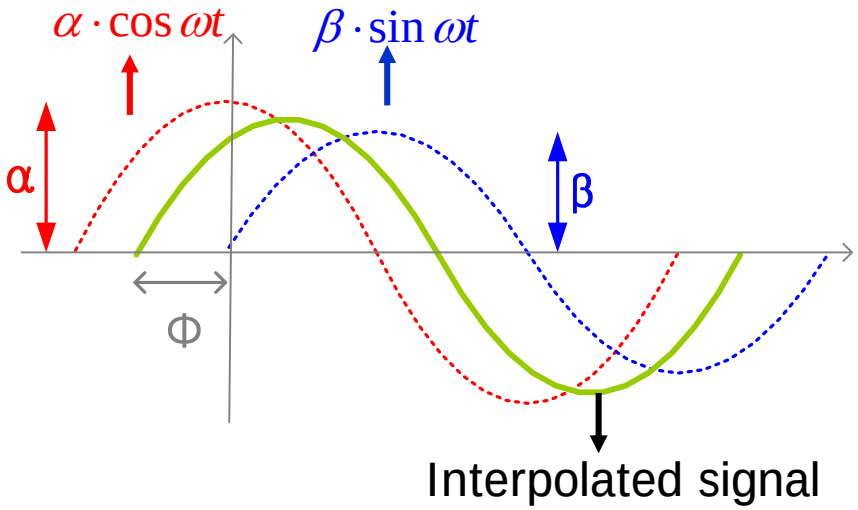
Phase controller

- PI-based phase controller
  - Phase interpolator produces mid-phase between I/Q input clocks
  - Implemented as current-mode summation
  - Possible phase range: 90 degs

$$f(t) = \alpha \cdot \cos\omega t + \beta \cdot \sin\omega t$$
$$= \sqrt{\alpha^2 + \beta^2}\cos(\omega t + \phi)$$

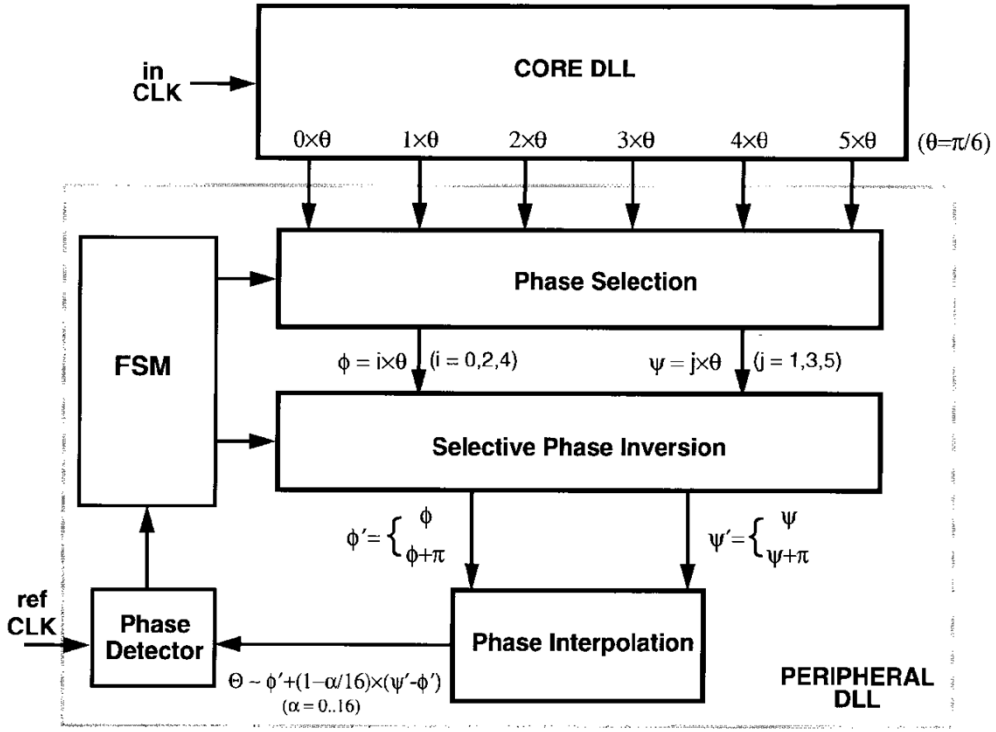
$$\phi = \tan^{-1}(\frac{\beta}{\alpha}), \quad \frac{\beta}{\alpha} = \tan\phi$$





Phase controller

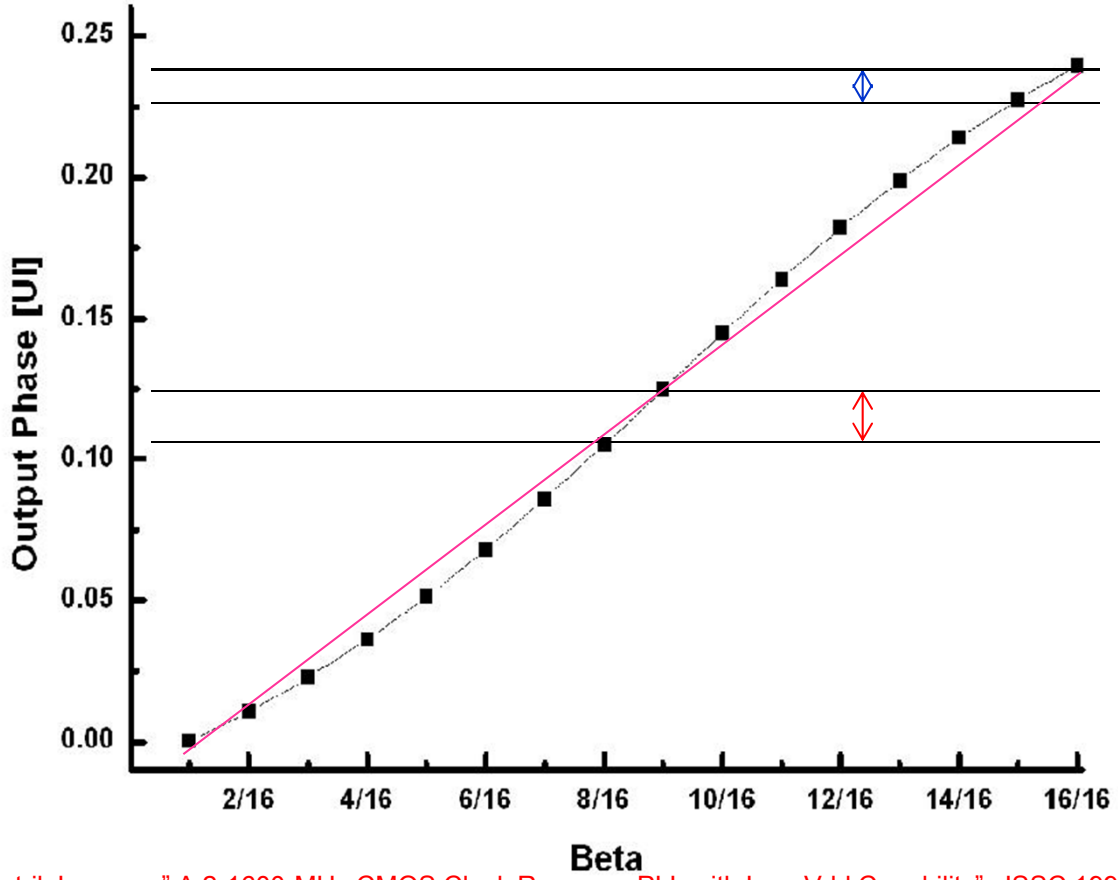
- PI-based phase controller (DLL)
  - Rotating two input clocks, it is possible to generate 360° phase.



Stefanos Sidiropoulos-"A Semidigital Dual Delay-Locked Loop" JSSC 1997

Phase controller

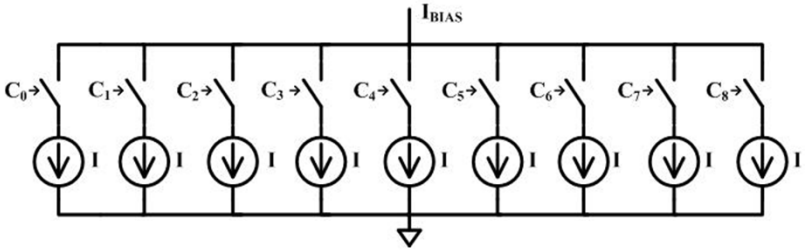
- PI-based phase controller



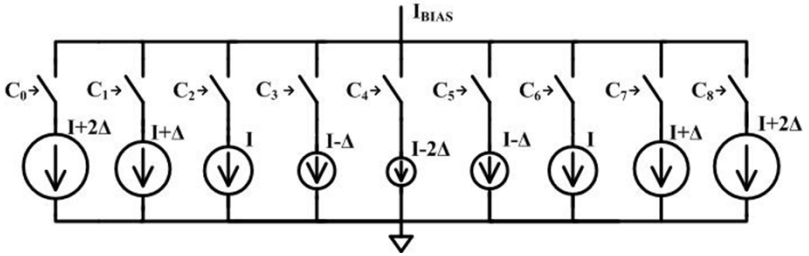
Patrik Larsson-" A 2-1600-MHz CMOS Clock Recovery PLL with Low-Vdd Capability", JSSC 1999

Phase controller

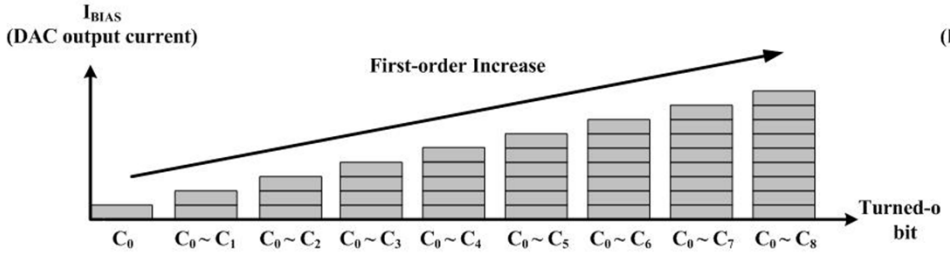
- PI-based phase controller
  - Linearization of PI output phase



< Schematic of Linear DAC >



< Schematic of Non-linear DAC >



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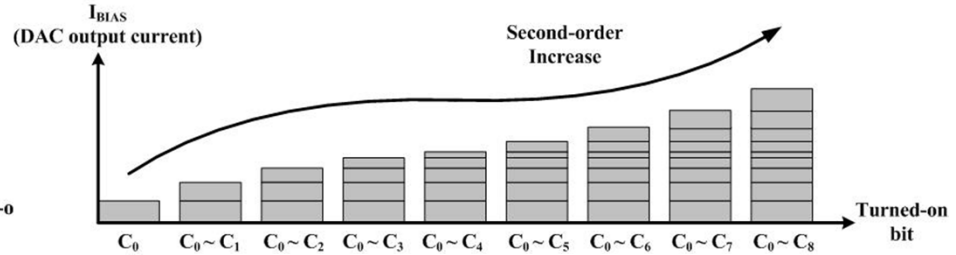

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Patrik Larsson-" A 2-1600-MHz CMOS Clock Recovery PLL with Low-Vdd Capability", JSSC 1999