High-speed Serial Interface

Lect. 15 – Clock and Data Recovery 2
PLL-Based CDR

• CDR Dynamic Characteristics
  – Similar to PLL
  
  \[
  T(s) = \frac{\alpha I_{cp}}{2\pi} \left( R + \frac{1}{sC} \right) K_{VCO} \frac{1}{s} \frac{\alpha I_{cp}(sRC + 1)K_{VCO}}{2\pi C} \frac{1}{s^2} + \frac{\alpha I_{cp}R K_{VCO}}{2\pi M} \frac{1}{s} + \frac{\alpha I_{cp}K_{VCO}}{2\pi C}
  \]

  – PD gain depends on data pattern
PLL-Based CDR

- PD gain for Hogge PD
CDR Jitter Characteristics

- Jitter Generation
  - Jitter amount for CDR output with input data having no jitter
  - Specs are given in UI
  - Example:
    < 10mUI rms jitter and < 100mUI peak-to-peak jitter for OC192 (10G SONET)
CDR Jitter Characteristics

- Jitter Tolerance
  - Maximum amount of input jitter allowed on the input for low BER (for example, 10e-12 for OC 192)
  - LF jitter can be large since CDR can track it
  - HF jitter above CDR bandwidth cannot be high
Jitter Characteristics in CDR

• Jitter transfer
  – How much input jitter transfers to the output

  – If the transfer function has peaking, jitter can be amplified
Burst-mode CDR

- Sporadic Input signal with data packet
  - Phase-locking required for every data packet
  - Training period (preamble) has to be as short as possible to maximize throughput
  - Fast-locking required during preamble
  - PLL-based CDR typically has long locking time
Burst-mode application

- Time Domain Multiple Access (TDMA)
- Example: Passive Optical Network (PON)
Gated Oscillator

• Chain of buffers with a NAND gate
  – Control the oscillation with a control signal
    • With control L, output H
    • With control H, output oscillation
  – Oscillation phase is reset at the rising edge of the enable signal
  – Oscillation freq. change possible with buffer delay change (VCO)
Clock Recovery with Gated-oscillator

- How to match data clock frequency with oscillator frequency?
Gated-oscillator-based CDR

• External Ref. clock required

• Advantage:
  – Instantaneous clock recovery
  – Small area

• Disadvantage
  – No jitter rejection
  – Maximum run length limitation limited because of frequency offset between gated oscillators

M. Banu – “Clock recovery circuits with instantaneous locking” Electronics Letter 1992
Blind oversampling CDR

Jaeha Kim – “Multi-gigabit-rate clock and data recovery based on blind oversampling” IEEE Communication magazine 2003
Blind oversampling CDR

- **Blind oversampling**
  - Input data is oversampled by internally generated multi-phase clocks.
  - Rx clock is not phase-/frequency-locked into Tx clock.

- **Decision**
  - Digital circuitry finds bit boundary by voting for a given data window
  - Sample at farthest phase from bit boundary is selected.

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Jaeha Kim – “Multi-gigabit-rate clock and data recovery based on blind oversampling” IEEE Communication magazine 2003

13 High-Speed Circuits and Systems Lab., Yonsei University 2013-1
Blind oversampling CDR

- **Advantage**
  - Instantaneous locking
  - Easy to port to another process
  - No more noise after sampling

- **Disadvantage**
  - High power consumption
  - Large area