High-speed Serial Interface

Lect. 16 – Clock and Data Recovery 3
CDR Design Example (권대현)

• Clock and Data Recovery Circuits
  – Transceiver
    • PLL vs. CDR
  – High-speed CDR
    • Phase Detector
    • Charge Pump
    • Voltage Controlled Oscillator
  – Design target & Considerations
  – Layout
  – Post-layout simulation
Clock and Data Recovery

- Asynchronous data transmitted with serial link
- Noisy + Asynchronous data
- Similar with PLL
- Input ➔ Data
PLL vs. CDR

- Clock edge periodic ↔ Data edge random
- PLL → Phase & Frequency detecting possible
- CDR → Phase detecting possible, Frequency detecting impossible
  - *Additional block* is needed for frequency detecting
  - PLL or FD (Frequency Detector)
High-speed CDR

- Limitations??
  - Phase Detector
    - Linear PD vs. Bang-bang PD
  - Charge pump
  - VCO
Phase Detector

- **Linear Phase Detector**
  - Hogge PD
    - Adequate to analyze dynamics
    - Constant gain
    - Charge pump ripple
    - Inadequate to high speed!!
## Phase Detector

- **Bang-bang PD**
  - Only direction!!
  - Infinite gain
  - High speed possible
  - Difficulty in analysis of dynamics

<table>
<thead>
<tr>
<th></th>
<th>Clock leads data</th>
<th>Clock lags data</th>
<th>No data transition</th>
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<tbody>
<tr>
<td><strong>Data</strong></td>
<td>![Diagram]</td>
<td>![Diagram]</td>
<td>![Diagram]</td>
</tr>
<tr>
<td><strong>Clock</strong></td>
<td>![Diagram]</td>
<td>![Diagram]</td>
<td>![Diagram]</td>
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<tr>
<td><strong>Xor</strong></td>
<td>![Diagram]</td>
<td>![Diagram]</td>
<td>![Diagram]</td>
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<tr>
<td></td>
<td>Up (0) Down (1)</td>
<td>Up (1) Down (0)</td>
<td>Up (0) Down (0)</td>
</tr>
</tbody>
</table>
Charge pump

- Speed limitation in conventional CP
  - Leakage & mismatch effect much marginal than PLL $\Rightarrow$ update much faster!!
  - High-speed $\Rightarrow$ Divider X (cause of latency)
  - CMFB X $\Rightarrow$ single node control
VCO & Sampler

• Ring-type VCO
  – Circular connection of inverter chain
  – Period = 2 X N X T_D (gate delay)
  – Frequency = 1 / period

• Sampler
  – High speed data + High speed clock \( \rightarrow X \)
  – Inaccuracy in inductor
  – High speed data + Low speed clock \( \rightarrow O \)
Multiphase clock CDR

- **Quarter-rate sampling**

10GHz: $0^\circ, 180^\circ$

5GHz: $0^\circ, 90^\circ, 180^\circ, 270^\circ$

2.5GHz: $0^\circ, 45^\circ, 90^\circ, 135^\circ, 180^\circ, 225^\circ, 270^\circ, 315^\circ$
Quarter-rate CDR

- Phase Detector
  - Bang-bang PD
  - Sampler X 8 \(\rightarrow\) quarter-rate clock sampling
Design Target & Consideration

• Design Target
  – 25-Gb/s quarter-rate CDR
  – Under 75-mW power consumption
  – Single signaling ➔ Decreasing complexity of layout

• Design Consideration
  – High input sensitivity
  – Multiphase clock alignment
  – Deserializing
• Design spec.
  
  - 25-Gb/s quarter-rate CDR
  - 40 [ mW ] power consumption
  - Chip size
    - Core size: 200 X 160 [um^2]
    - Output Driver: 100 X 160 [um^2]

Input Data (25 Gb/s)
Post-layout simulation

Retimed Data (6.25 Gb/s)

Retimed clock (6.25 GHz)

Locking process
Digital CDR (최광천)

• DCO quantization error
  – DCO has limited resolution, so that frequency cannot be perfectly matched with single code.
  – This quantization error in frequency is integrated in the phase domain. That results in cycle slip in time domain
Digital PLL vs. CDR

- DCO quantization error
  - Phase is updated at
    - Rising edges of reference clock in the PLL
    - Transition edges in the CDR
Digital PLL vs. CDR

• DCO quantization error
  – Phase is updated much-faster in CDR since input transition is way more than reference clock (<100MHz in HSI applications)
  – Maximum phase error is larger in digital PLL
Digital CDR Category

• PLL-based DCDR
  – Similar with ADPLL
  – $\text{CLK}_{\text{REF}}$ not required
  – Freq. detector required

• DLL-based DCDR
  – High freq. $\text{CLK}_{\text{REF}}$ required
  – FD not required
  – More stable
  – Easy to design
PLL-based digital CDR

- Most intuitive implementation

Pavan Kumar Hanumolu – "A 1.6Gbps Digital Clock and Data Recovery Circuit" CICC 2006
PLL-based digital CDR

- Linearized model
  - Z-domain model can be transformed into S-domain model as ADPLL.
  - DCO part is analogous so that it cannot be perfectly modeled.
PLL-based digital CDR

- Majority vote
  - Voting filter can alleviate the DLF operating speed requirement.

Pavan Kumar Hanumolu – "A 1.6Gbps Digital Clock and Data Recovery Circuit" CICC 2006
PLL-based digital CDR

- Delta-sigma modulator
  - DSM to improve timing resolution is also preferred in CDR applications.

Pavan Kumar Hanumolu – "A 1.6Gbps Digital Clock and Data Recovery Circuit" CICC 2006
**DLL-based digital CDR**

- Digital to phase converter
  - Previously shown DLL-based phase controller is employed

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**Diagram:**

- !!PD
- Voting filter
- DLF
- D2P

**Legend:**

- $d_n$
- $p_n$
- $d_{n-1}$

**Diagrams:**

- Bang-Bang Phase Detector
- Decimation
- Phase Integ.
- Digital to Phase Converter

Bank of W (word width) phase detectors, each producing a 2 bit output

Jeff L. Sonntag – “A Digital Clock and Data Recovery Architecture for Multi-Gigabit/s Binary Links” JSSC 2006
DLL-based digital CDR

- Easily analyzed with z-domain model
  - Digital-to-phase converter is well-defined phase output, thus, very good to model real situation.

Jeff L. Sonntag – “A Digital Clock and Data Recovery Architecture for Multi-Gigabit/s Binary Links” JSSC 2006
Linear PD

• Bang-bang phase detector is much more appropriate for digital loop filter.
  – Bang-bang PD provides binary output.
  – Phase detection is possible even after deserialized.

• It is hard to give up linear dynamics.
  – Linear dynamics provides predictable bandwidth and stability.
  – But TDC used in digital PLL is not applicable in digital CDRs because reference period is much smaller in CDR applications.

• How to digitize linear PD??
Digitizing linear PD

- Hogge PD gives linear output
  - Phase error is proportional to phase error
Digitizing linear PD

- Integrating and analog-to-digital conversion
  - Sigma-delta ADC and hogge PD are employed in this example.

Michael H. Perrott – "A 2.5-Gb/s Multi-Rate 0.25-m CMOS Clock and Data Recovery Circuit Utilizing a Hybrid Analog/Digital Loop Filter and All-Digital Referenceless Frequency Acquisition" JSSC 2006
## Digital CDR trend

- Moderate data rate and power consumption

<table>
<thead>
<tr>
<th>Year</th>
<th>Journal</th>
<th>Title</th>
<th>Data rate [Gb/s]</th>
<th>Power [mW]</th>
<th>Power [nJ/bit]</th>
<th>Process [nm]</th>
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<tbody>
<tr>
<td>2012</td>
<td>JSSC</td>
<td>A 3x9 Gb/s Shared, All-Digital CDR for High-Speed, High-Density I/O</td>
<td>6-9</td>
<td>34.4333</td>
<td>3.82593</td>
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<td>2011</td>
<td>TCAS2</td>
<td>Clock- and Data-Recovery Circuit With Independently Controlled Eye-Tracking Loop for High-Speed Graphic DRAMs</td>
<td>5.8</td>
<td>109.8</td>
<td>18.931</td>
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<td>2011</td>
<td>JSSC</td>
<td>A TDC-Less 7 mW2.5 Gb/s Digital CDR With Linear Loop Dynamics and Offset-Free Data Recovery</td>
<td>0.5-3.2</td>
<td>7</td>
<td>2.8</td>
<td>130</td>
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<td>2011</td>
<td>JSSC</td>
<td>A 1.0–4.0-Gb/s All-Digital CDR With 1.0-ps Period Resolution DCO and Adaptive Proportional Gain Control</td>
<td>1-4</td>
<td>11.4</td>
<td>3.8</td>
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<td>2011</td>
<td>JSSC</td>
<td>A 0.5-to-2.5 Gb/s Reference-Less Half-Rate Digital CDR With Unlimited Frequency Acquisition Range and Improved Input Duty-Cycle Error Tolerance</td>
<td>0.5-2.5</td>
<td>6.1</td>
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<td>2009</td>
<td>ASSCC</td>
<td>Loop Latency Reduction Technique for All-Digital Clock and Data Recovery Circuits</td>
<td>1.25</td>
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<td>2006</td>
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<td>A Digital Clock and Data Recovery Architecture for Multi-Gigabit/s Binary Links</td>
<td>5</td>
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<td>2006</td>
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<td>A 2.5-Gb/s Multi-Rate 0.25-m CMOS Clock and Data Recovery Circuit Utilizing a Hybrid Analog/Digital Loop Filter and All-Digital Referenceless Frequency Acquisition</td>
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<td>2006</td>
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<td>A 1.6Gbps Digital Clock and Data Recovery Circuit</td>
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