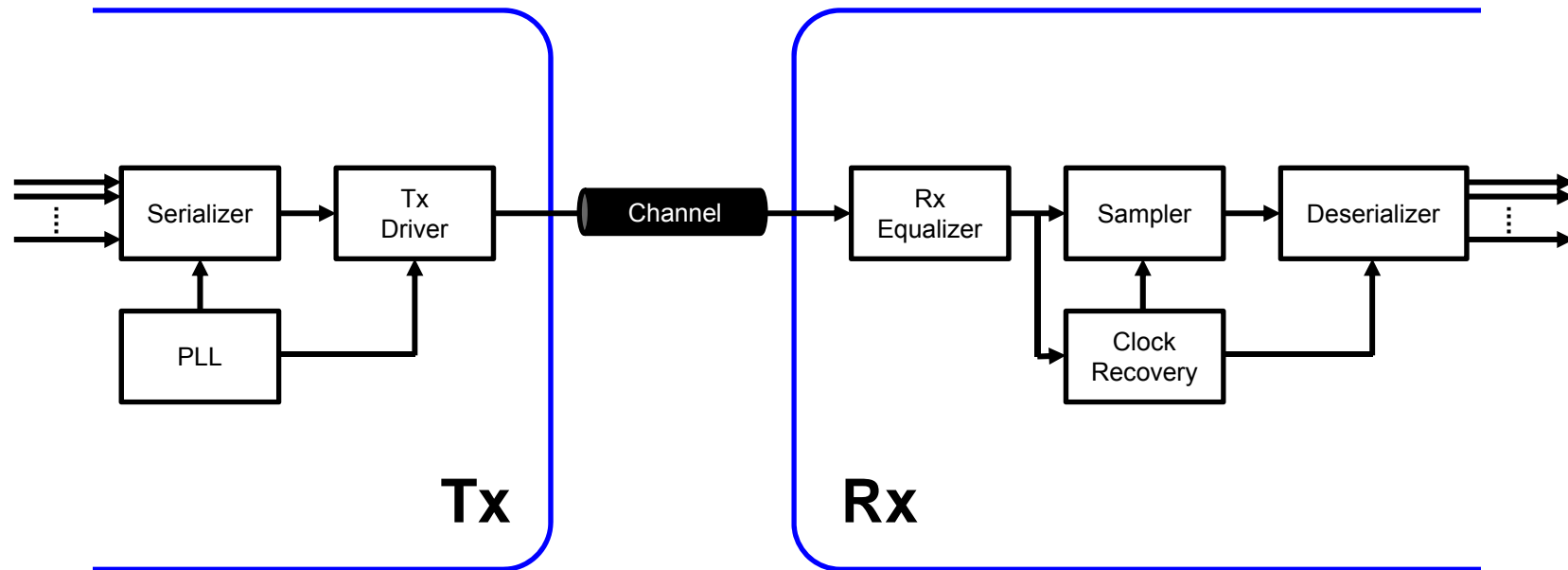


# High-speed Serial Interface

## Lect. 2 – Channel Characteristic

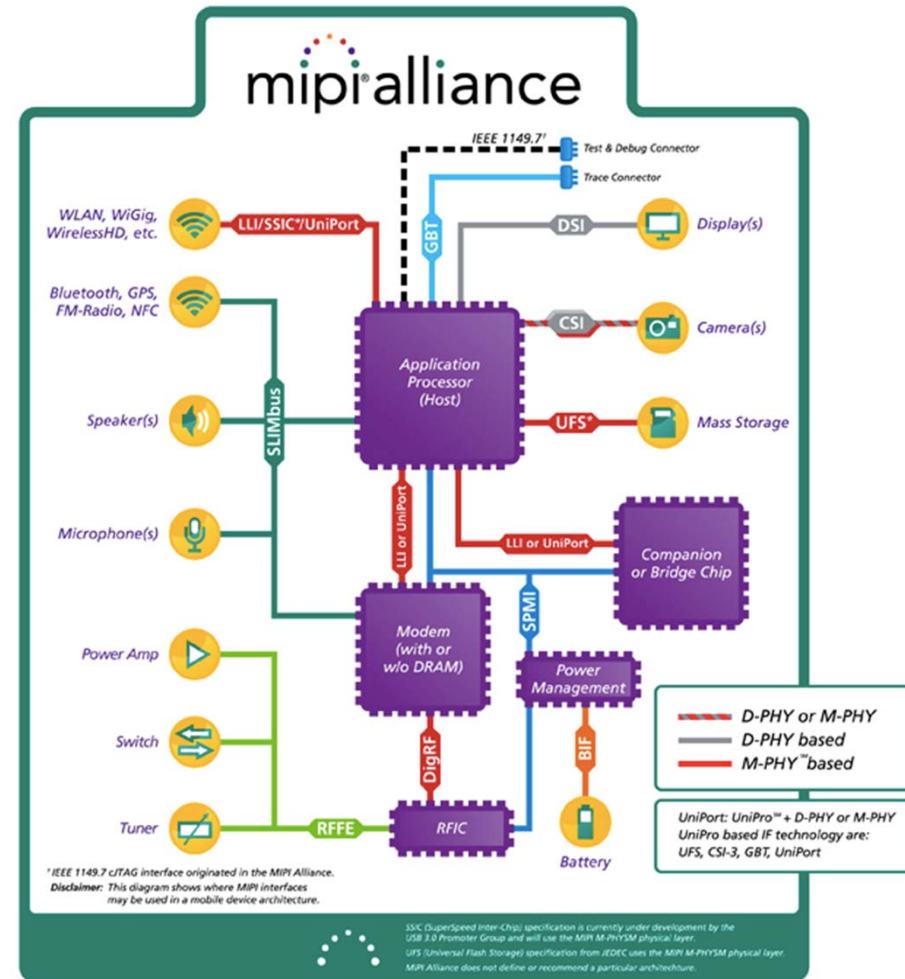
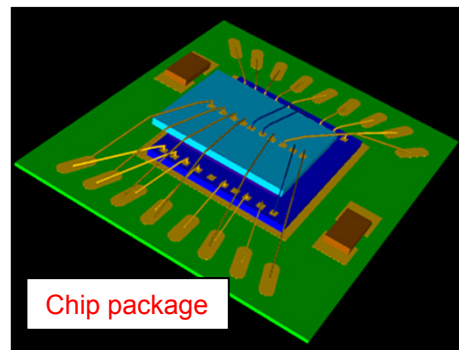
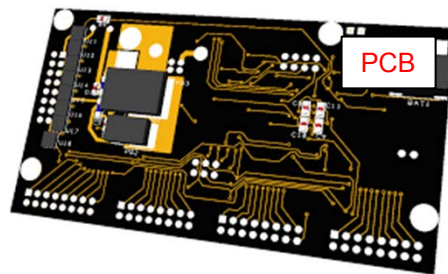
# Block diagram

- Where are we today?



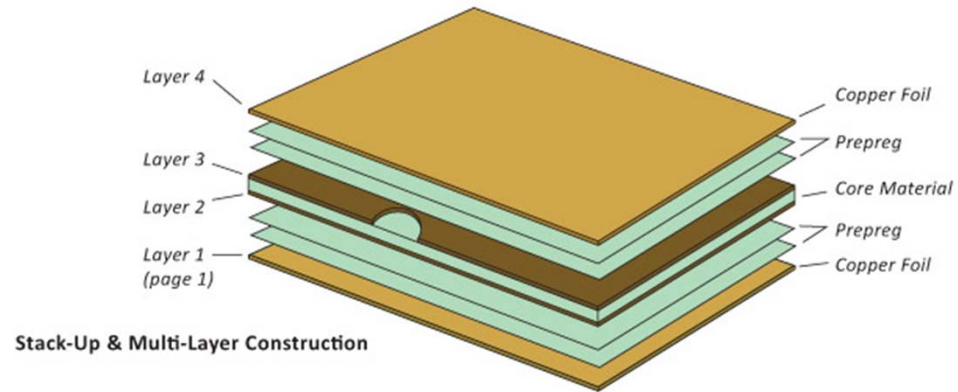
# Interface Channels

- Chip-to-chip
  - PCB
  - Chip packages



# Interface Channels

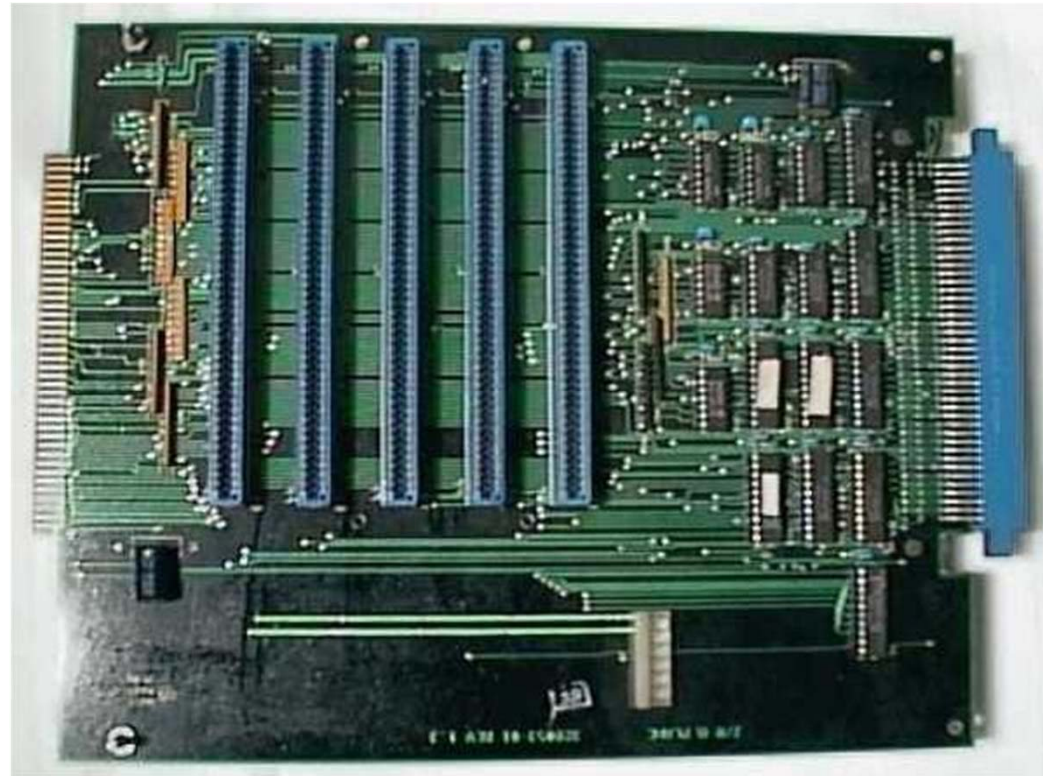
- PCB



- PCB Stack-Up  
Core (Copper traces with FR4)  
+ Prepreg + Copper Foil
- Various stack-up schemes  
(Signal, Power, Ground planes)
- Vias connect different layers

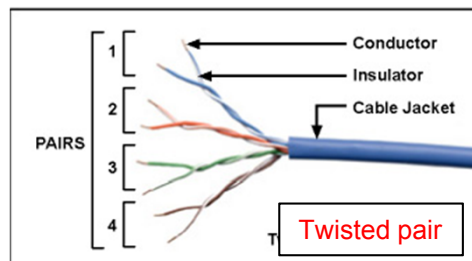
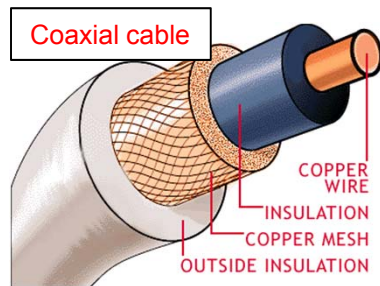
# Interface Channels

- Backplane and Linecard



# Interface Channels

- Box-to-box
  - Cables

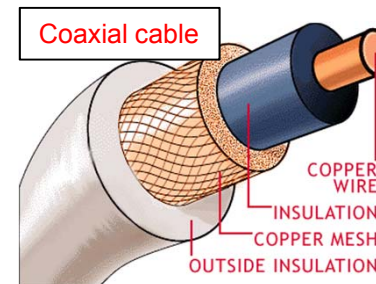
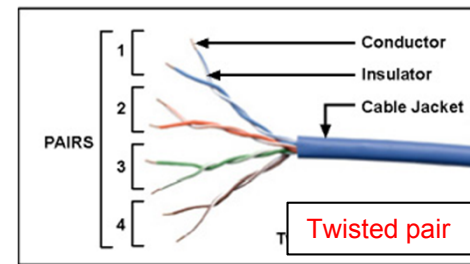


# Interface Channels

- Box-to-box

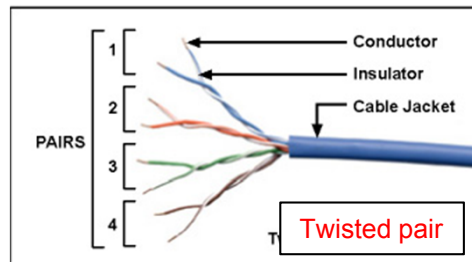
- Cables

- [Coaxial cable](#)
    - [Mineral-insulated copper-clad cable](#)
    - [Twinax cable](#)
    - [Flexible cables](#)
    - [Non-metallic sheathed cable](#)
    - [Metallic sheathed cable](#)
    - [Multicore cable](#)
    - [Shielded cable](#)
    - [Single cable](#)
    - [Twisted pair](#)
    - [Twisting cable](#)



# Interface Channels

- Twisted Pair



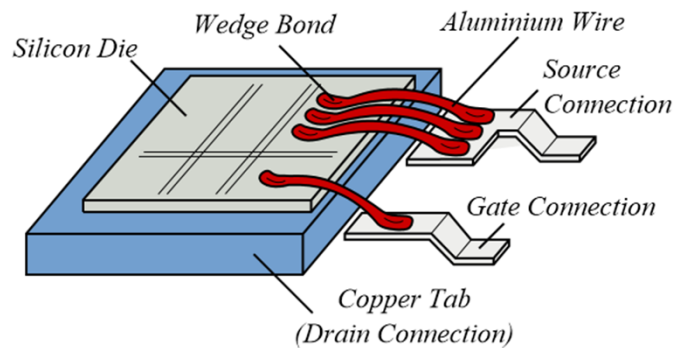
Name	Type	Bandwidth	Applications
Level 1		0.4 MHz	Telephone and modem lines
Level 2		4 MHz	Older terminal systems, e.g. IBM 3270
Cat3	UTP <sup>[7]</sup>	16 MHz <sup>[7]</sup>	10BASE-T and 100BASE-T4 Ethernet <sup>[7]</sup>
Cat4	UTP <sup>[7]</sup>	20 MHz <sup>[7]</sup>	16 Mbit/s <sup>[7]</sup> Token Ring
Cat5	UTP <sup>[7]</sup>	100 MHz <sup>[7]</sup>	100BASE-TX & 1000BASE-T Ethernet <sup>[7]</sup>
Cat5e	UTP <sup>[7]</sup>	100 MHz <sup>[7]</sup>	100BASE-TX & 1000BASE-T Ethernet <sup>[7]</sup>
Cat6	UTP <sup>[7]</sup>	250 MHz <sup>[7]</sup>	10GBASE-T Ethernet
Cat6a		500 MHz	10GBASE-T Ethernet
Class F	S/FTP <sup>[7]</sup>	600 MHz <sup>[7]</sup>	Telephone, CCTV, 1000BASE-TX in the same cable. 10GBASE-T Ethernet.
Class Fa		1000 MHz	Telephone, CATV, 1000BASE-TX in the same cable. 10GBASE-T Ethernet.



# Chip package

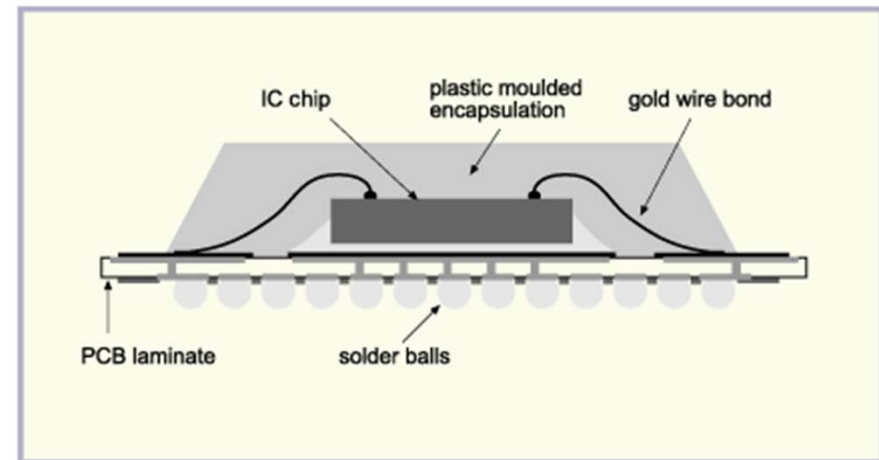
- Wire bonding
  - Bonding wires connect pads and package lead frames

→ Inductance due to wires



Limited pin number

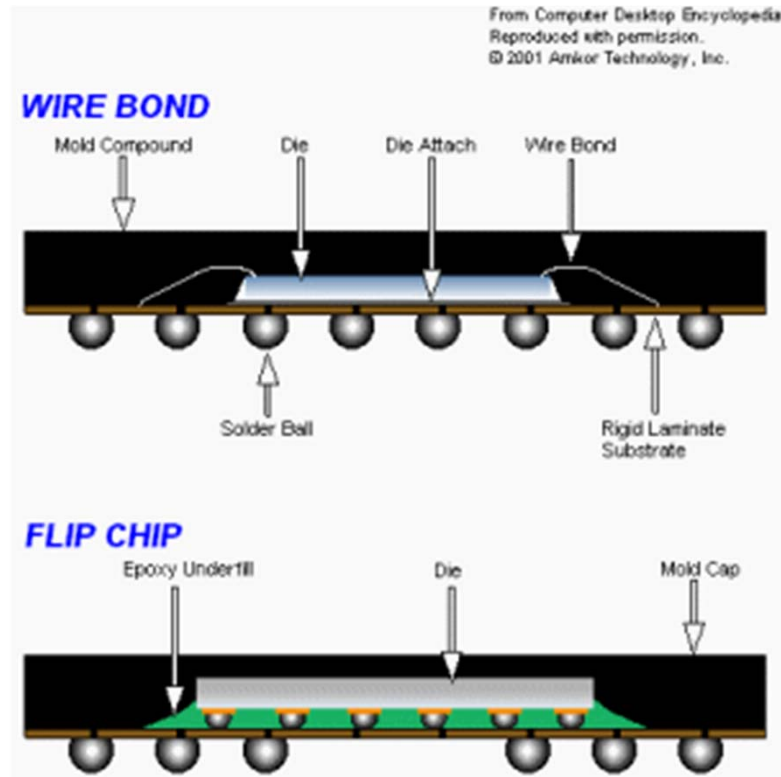
## Ball Grid Array



Note: Reproduced from the only available original

# Chip package

- Flip Chip



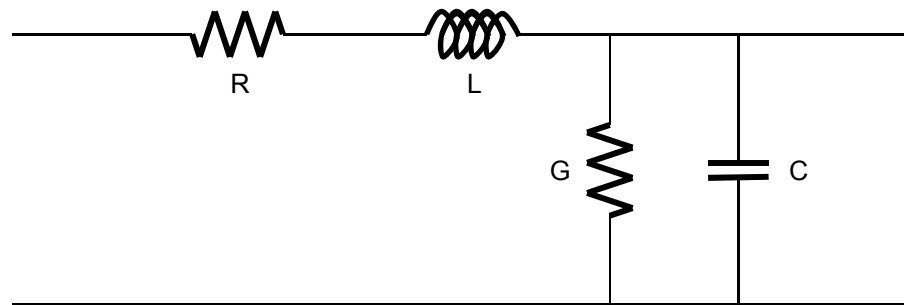
- Package type often decides the maximum data rate!

# Interface Channels

- Relatively-large SNR and Bandwidth
  - Compared with wireless application
  - Simple modulation such as ASK, NRZ is often sufficient
- Frequency-Dependent Loss
  - Dielectric loss
  - Skin effect
- Reflection
  - Broadband impedance matching

# Channel loss

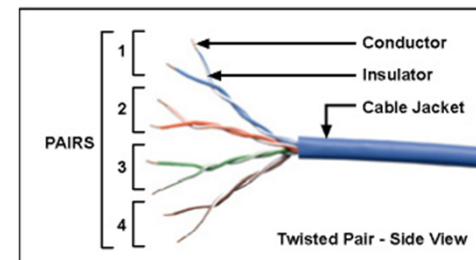
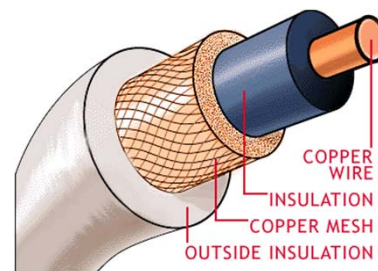
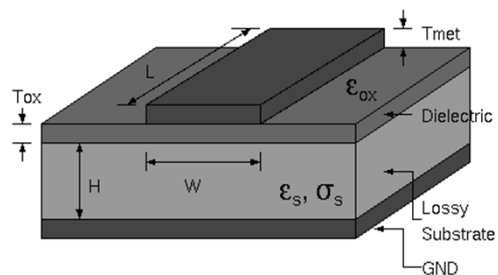
- Two main loss components
  - Dielectric loss
  - Skin effect
- In the view of transmission line,
  - Dielectric loss  $\rightarrow G \uparrow$
  - Skin effect  $\rightarrow R \uparrow$



# Channel loss

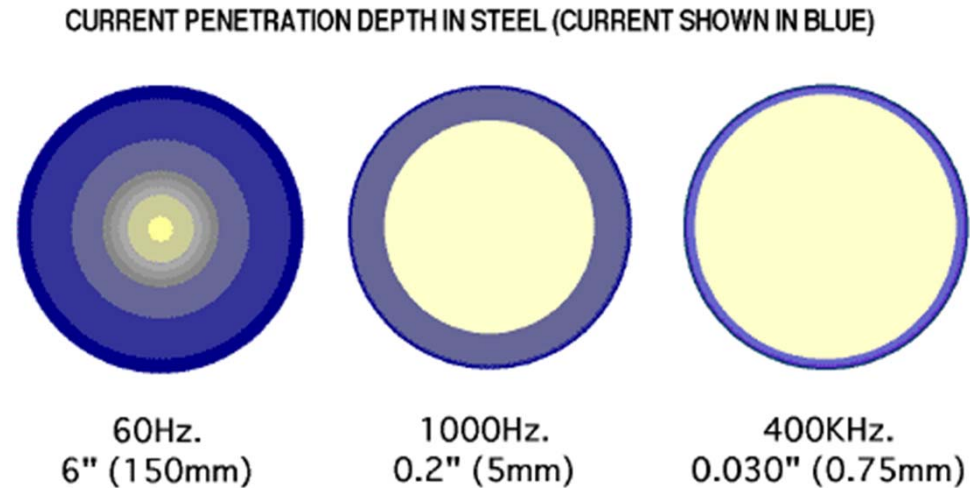
- Dielectric loss
  - Loss between 2 metal separated by insulation material
  - Occurs in any kind of channels including insulation
  - Loss increases as  $f \uparrow$

$$|H(f)| = e^{-\frac{l\pi \tan \delta \sqrt{\epsilon_r}}{c} \cdot 2fe}$$



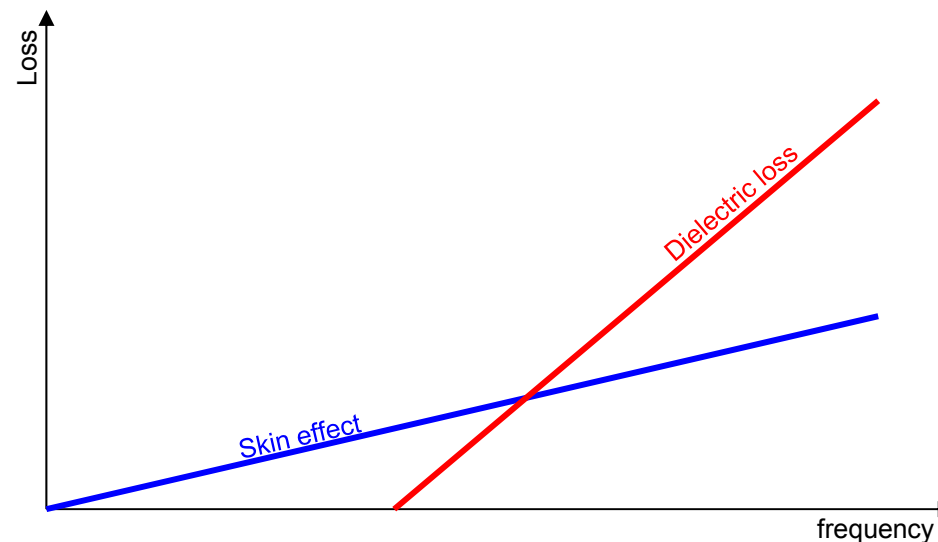
# Channel loss

- Skin effect
  - As frequency increases, less current flows at the center of conductor.
  - Loss increases as  $\sqrt{f} \uparrow$



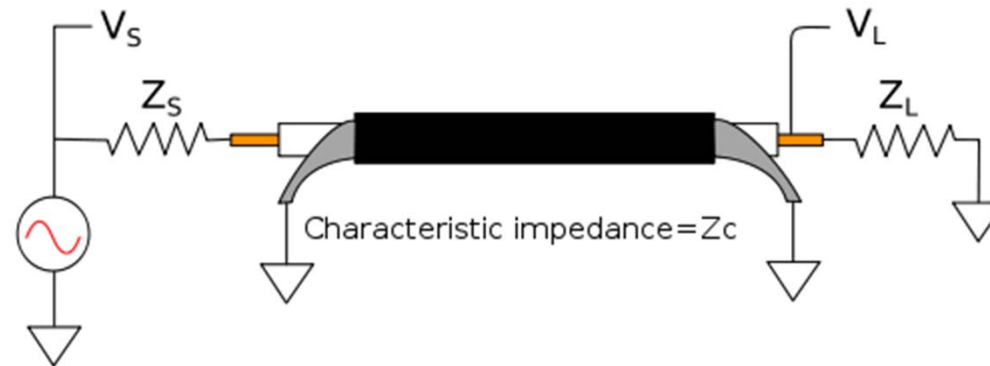
# Channel loss

- Total loss
  - In low frequency, skin effect  $>$  dielectric loss
  - In high frequency, skin effect  $<$  dielectric loss



- Bandwidth limitation due to f-dependent loss!

# Impedance mismatch

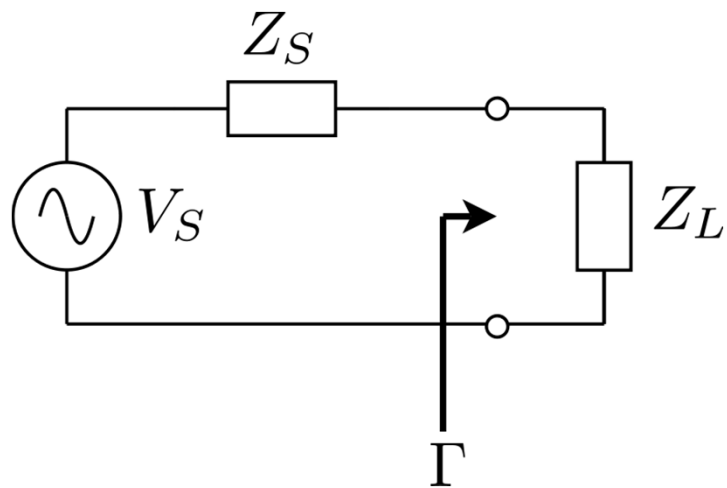


- Ideally  $Z_s = Z_c = Z_L$
- Practically not possible to achieve this due to PVT variations for ICs, manufacturing uncertainties for PCB traces and vias, connectors

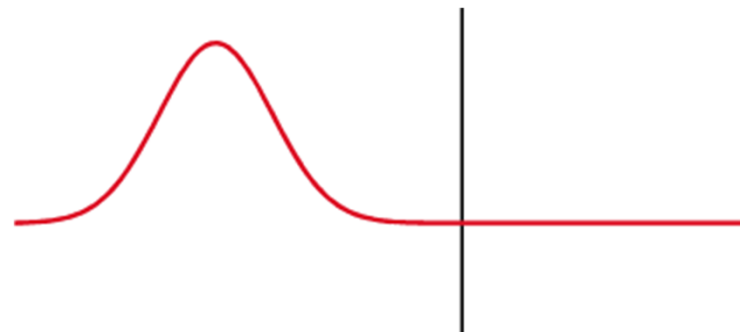


# Impedance mismatch

- Reflection

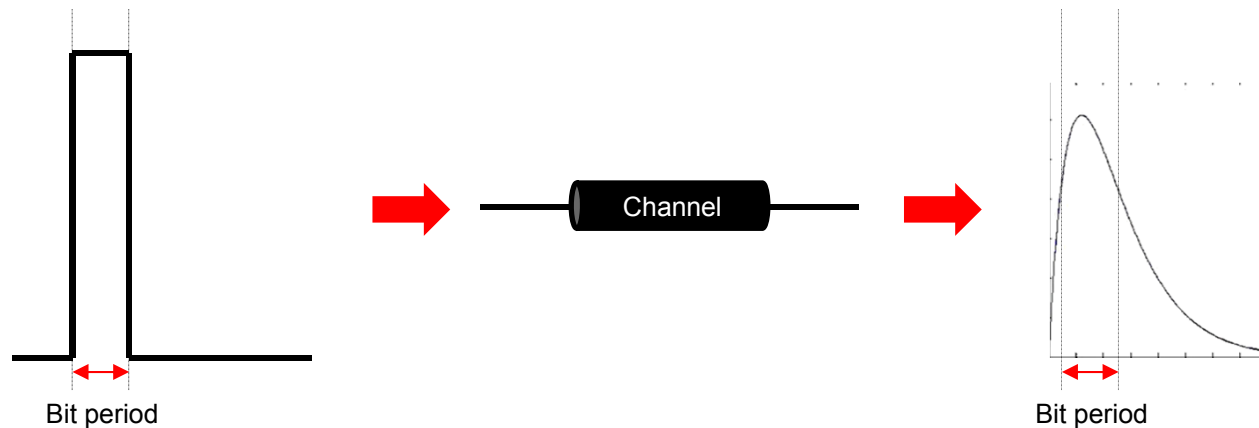


$$\Gamma = \frac{Z_L - Z_S}{Z_L + Z_S}$$



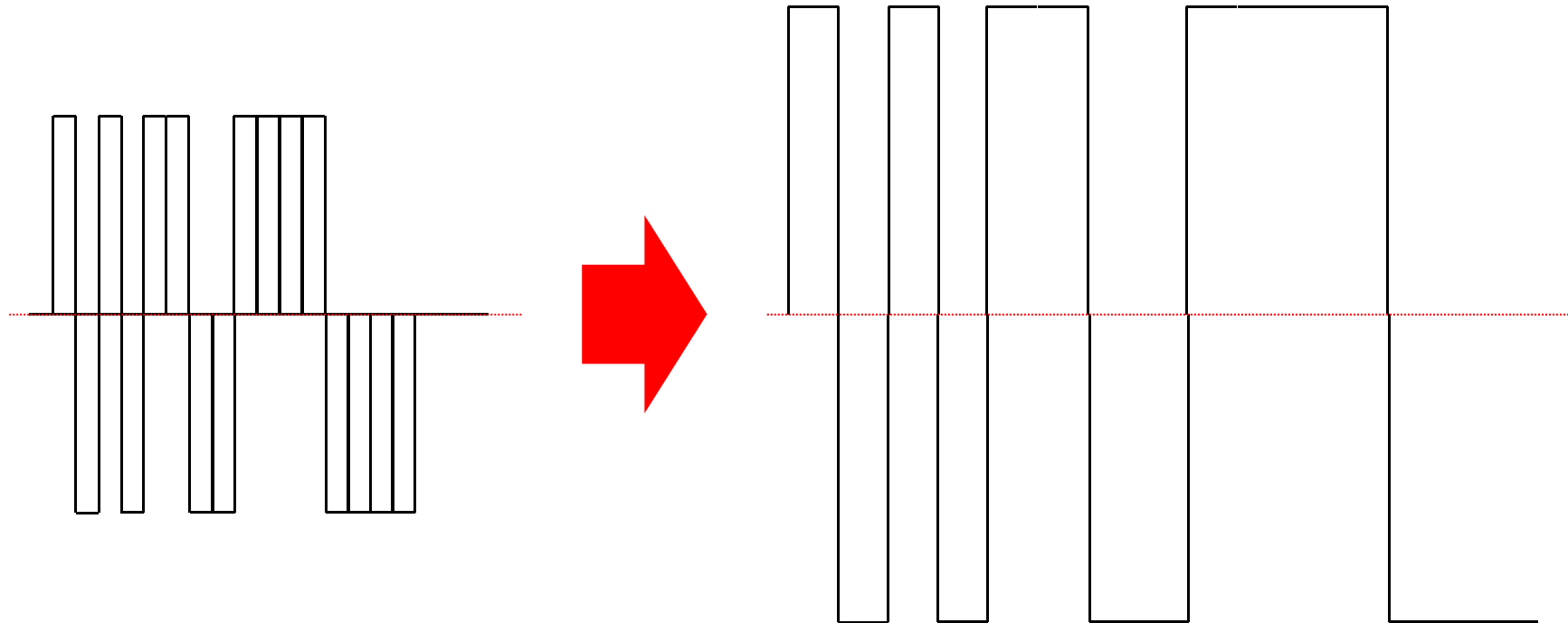
# Inter-symbol interference

- Channel with f-dependent loss, reflection distorts pulse response
  - Pulse response outside bit period becomes non-zero.
  - Waveform of present bit is affected by former bits.



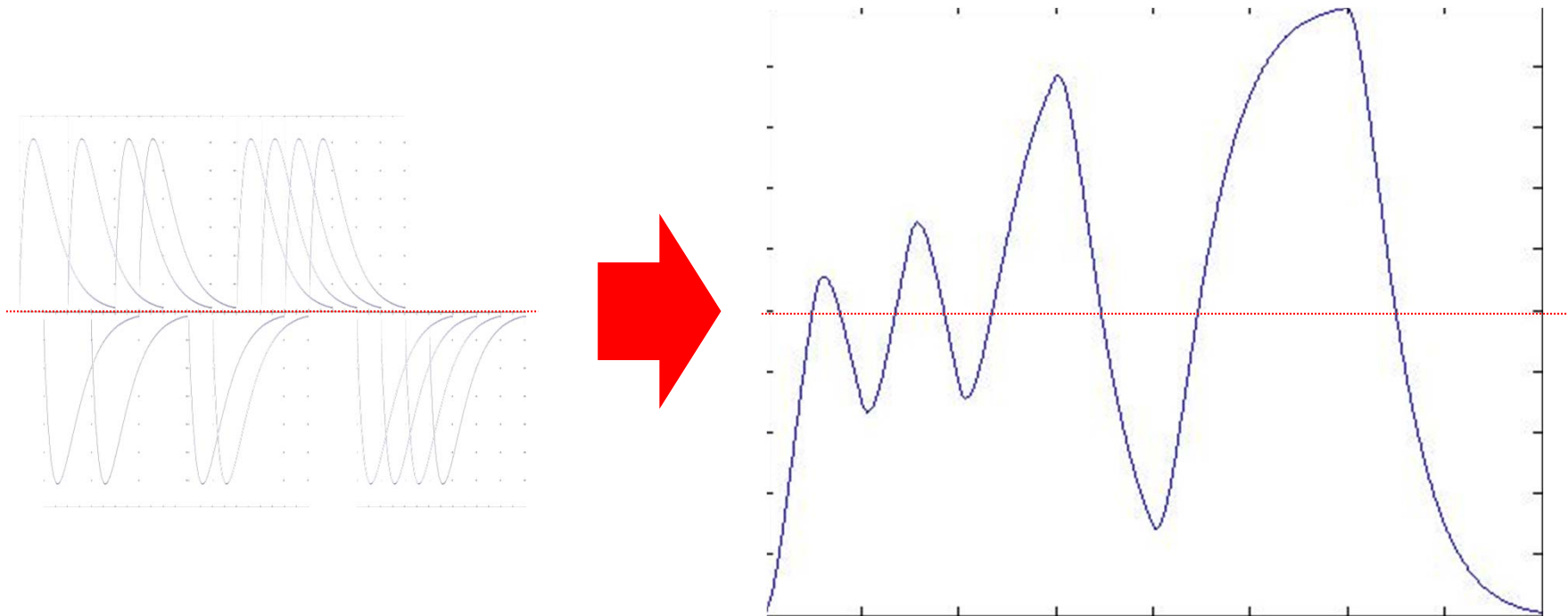
# Inter-symbol interference

- Waveform example: ideal case
  - Given data pattern: 1010110011110000



# Inter-symbol interference

- Waveform example: w/ ISI
  - Given data pattern: 1010110011110000



# Inter-symbol interference

- How ISI affects performance?
  - Receiver has sampling circuits (ADC or D-FF).
  - Sampling circuits require setup/ hold time to meet required BER spec.

1. ISI distorts position of edge
2. Setup/ hold margin of sampling circuit ↓
3. Error sampling ↑
4. BER performance ↓

