Project #1 for Electronic Circuit II

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- Deadline : 11:59 pm on Apr. 26, 2015. Penalties for late hand-in.

- Team

Students are expected to form a team of two members to do the project and hand in one project report. Equal grades will be given to the members of the same team. Each team must do its own simulation and analysis.

Team organization deadline : Submit names and ID numbers of team by e-mail until Apr. 6, 2015 before TA session. If you cannot find your partner, contact TA by e-mail. Otherwise, we will match your partner randomly.

- MOS PSpice parameters

Use Level 7 PSpice parameters for 0.25㎛ CMOS process. The course homepage has PSpice 9.1 student version, level 7 PSpice parameters as well as PSpice basic manual.

- Design rules

1. VDD = 2.5V
2. 0.25㎛ ≤ length of gate ≤ 2㎛
3. 0.25㎛ ≤ width of gate ≤ 100㎛
4. 0.1 pF ≤ all capacitors ≤ 20 ㎌
5. 0 Ω < all resistors ≤ 800kΩ
6. Body of pMOS must connect to VDD
7. Body of nMOS must connect to GND

- Goal

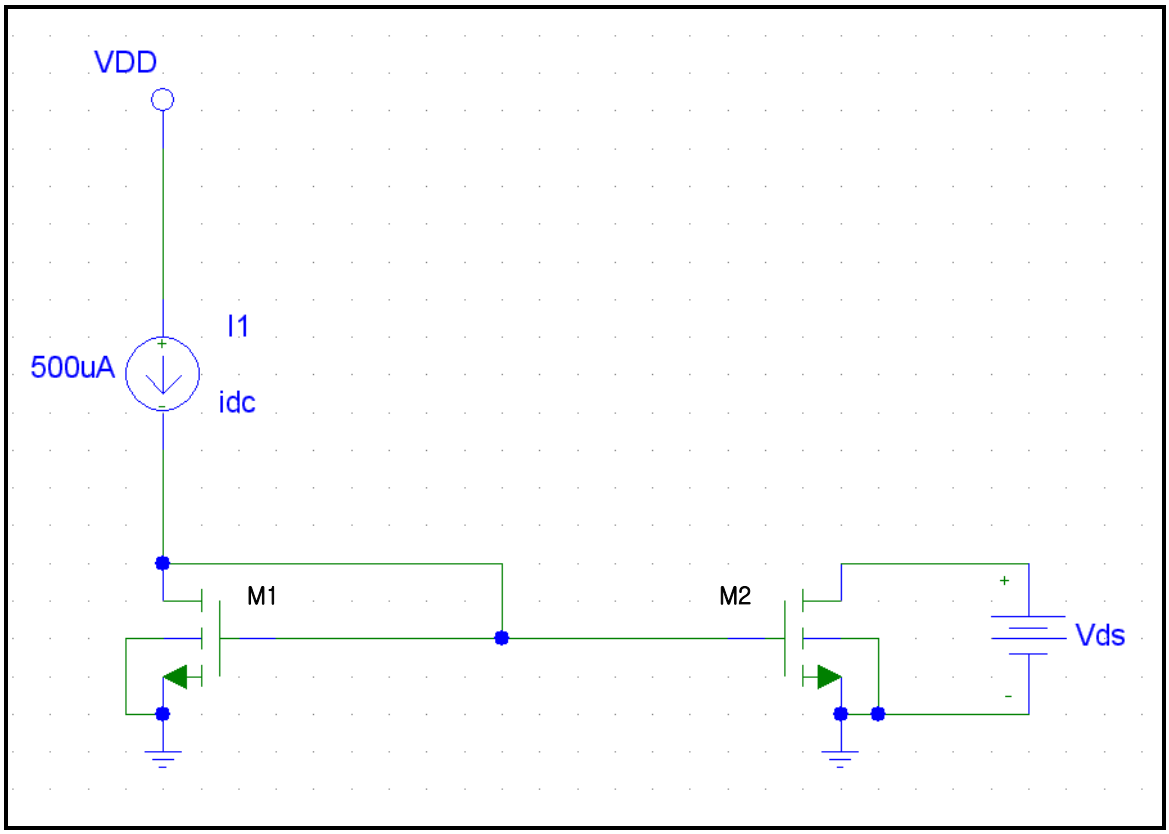
You are expected to design 2-stage OTA (Operational Transconductance Amplifier) satisfying given specifications. The project is divided into three parts (Current Mirror, Single-stage OTA, Mirrored OTA) so that you can build up your design.

Your design will be evaluated based on following criteria:

1. How well you satisfy the specifications.
2. 10 extra points will be given for up to five designs that satisfy all the specifications and produce highest gain-bandwidth products for Part Ⅲ in the class.
3. How good your design report is. Three extra points will be given if your report is written in English (Optional).
4. Three best designs will be selected and their designers will be given opportunities to present their results in class in English for extra 5 points.

I. Current Mirror Design[5]

Design Current Mirror that satisfies the following specifications



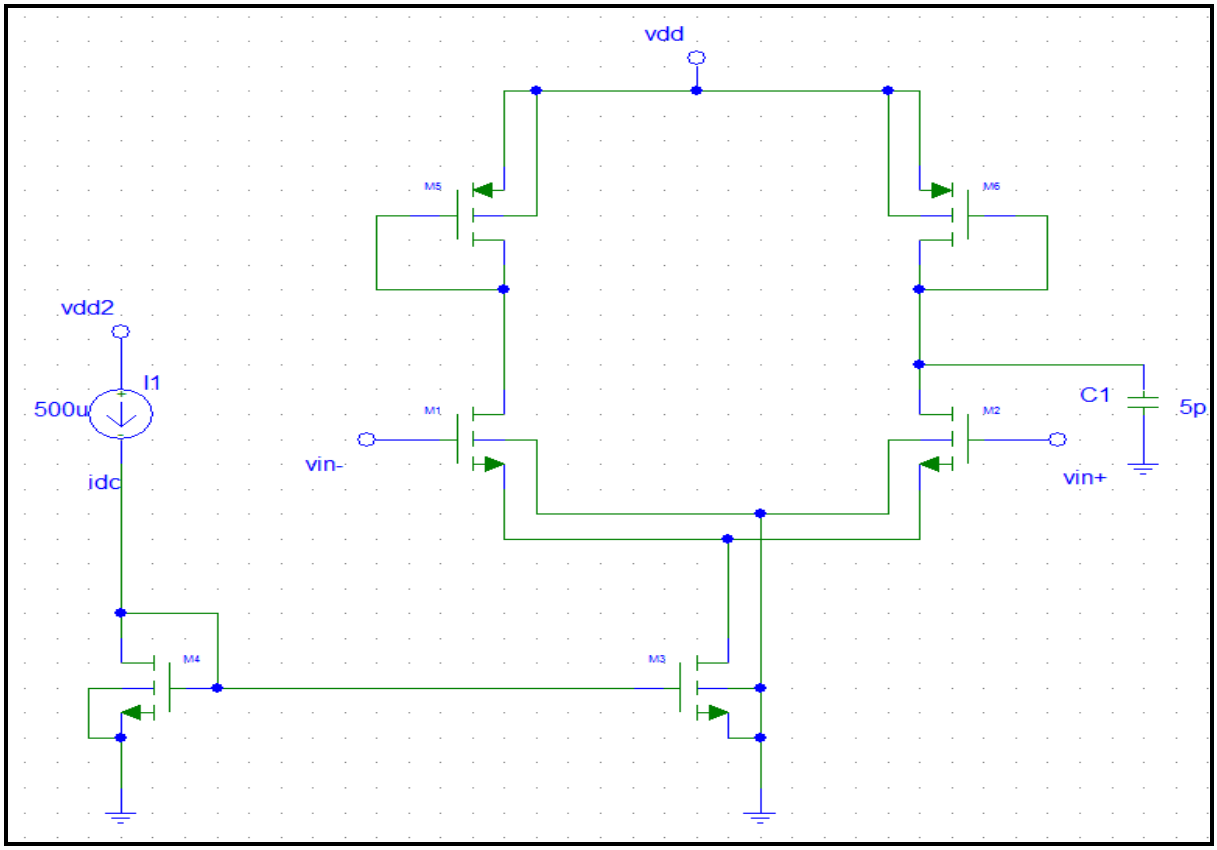
< Figure 1. Current Mirror >

- Current Mirror Specifications

Parameter	**Value**
V_{DS}	<0.7 (V)
Output Resistance	>63 (KOhm)
Current Copied	>99%

II. Single-Stage Differential OTA [25]

Design Single-Stage OTA which satisfies the following specifications. V_{cm}=1.25V.



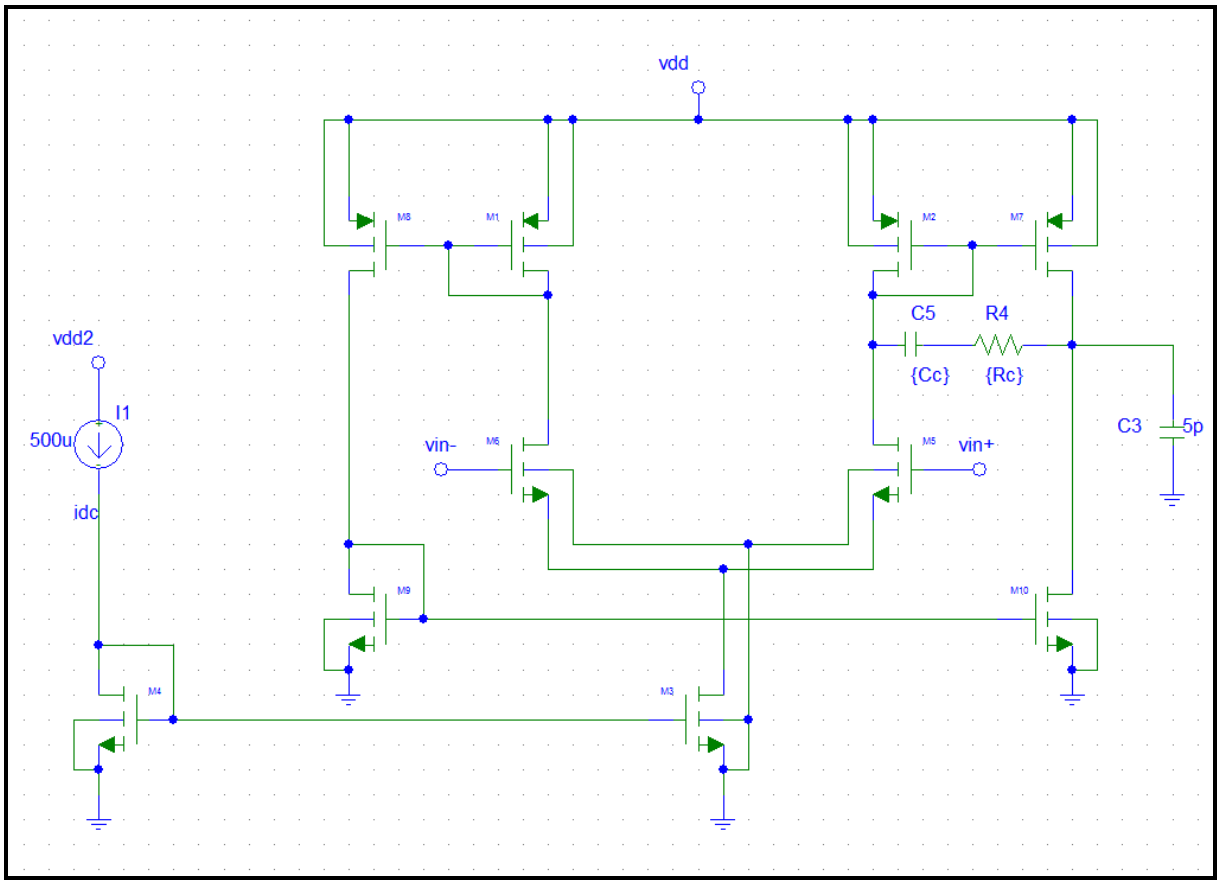
< Fig. 2 > Single-Stage Differential Amplifier Schematic

-Singe-stage Differential OTA specifications

Parameter	**Value**
A_V	>16dB
Bandwidth	>20MHz
Input common mode range	Range> 1.1V
Power Consumption	<1.5 mW

III. Mirrored OTA [50]

Design Mirrored OTA which satisfies the following specifications. V_{cm}=1.25V.



< Fig. 3 > Mirrored OTA Schematic

- Mirrored OTA Specifications

Parameter	**Value**
A_V	>56dB
Bandwidth	>60KHz
Phase Margin	>65°
V_{p-p}	>1.5V
Slew Rate	>13MV/s
CMRR	>85dB
Power Consumption	<2.5mW

III. Design Report [20]

Write a design report in which you clearly explain how you come up with your transistor W/L values, what you have achieved for design specifications, and supporting simulation results. All your design results should be summarized in Design Summary Sheets. Place the Design Summary Sheets right after the cover page of your report.

**** Maximum Report pages : 10 (Not including Cover, Design Summary Sheet)**

Design Summary Sheet

Name : Student ID No. :

Name : Student ID No. :

< Current Mirror >

$(W/L)_1$	
$(W/L)_2$	
V_{DS}	
Output Resistance	
Current Copied	

< Single Stage Differential OTA >

$(W/L)_1$	
$(W/L)_2$	
$(W/L)_3$	
$(W/L)_4$	
$(W/L)_5$	
$(W/L)_6$	
A_v	
Bandwidth	
ICMR	
Power Consumption	

< Mirrored OTA >

$(W/L)_1$	
$(W/L)_2$	
$(W/L)_3$	
$(W/L)_4$	
$(W/L)_5$	
$(W/L)_6$	
$(W/L)_7$	
$(W/L)_8$	
$(W/L)_9$	
$(W/L)_{10}$	
A_V	
Bandwidth	
Phase Margin	
Output Swing($V_{p-p)}$	
Slew Rate	
CMRR	
Power Consumption	