Project 1
Design Guide

High-Speed Circuits & Systems Lab.
Dept. of Electrical and Electronic Engineering
Yonsei University

High-Speed Circuits and Systems Laboratory
HSCS

Introduction

The Project is composed of 3-parts

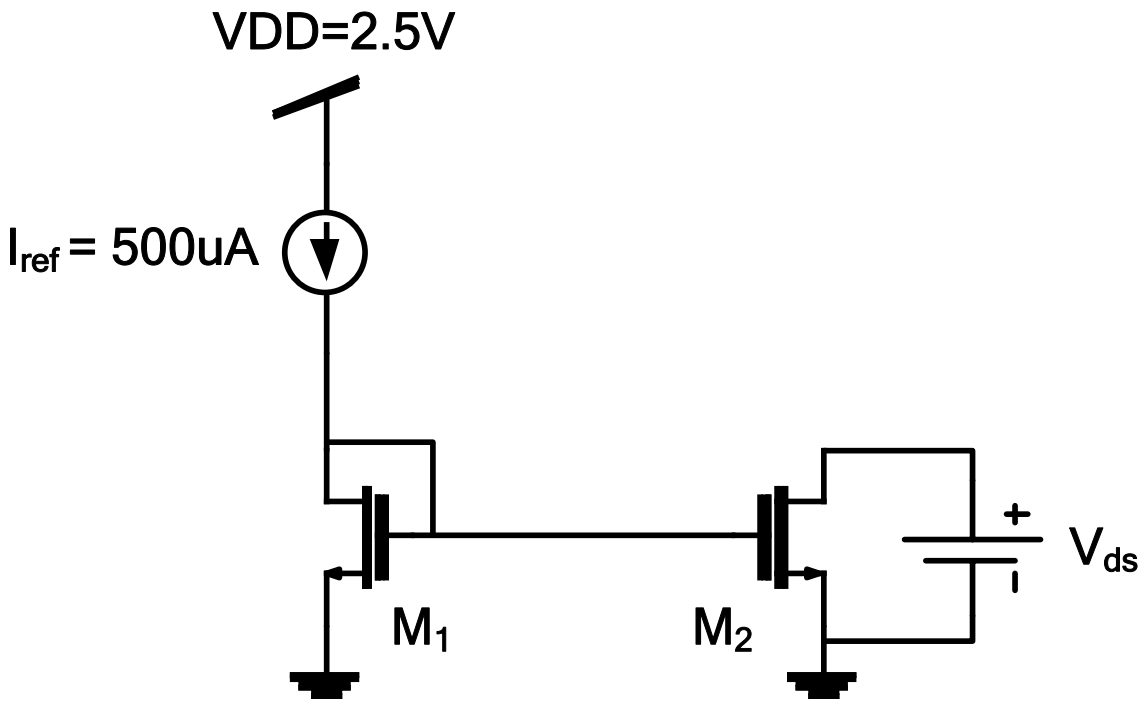
1. Current Mirror Design

2. Single-Stage Differential OTA Design

3. Mirrored OTA with Compensation RC Design

Deadline : Submit hardcopy
until 11:59 PM on Apr. 26, 2015 @ B629

Current Mirror

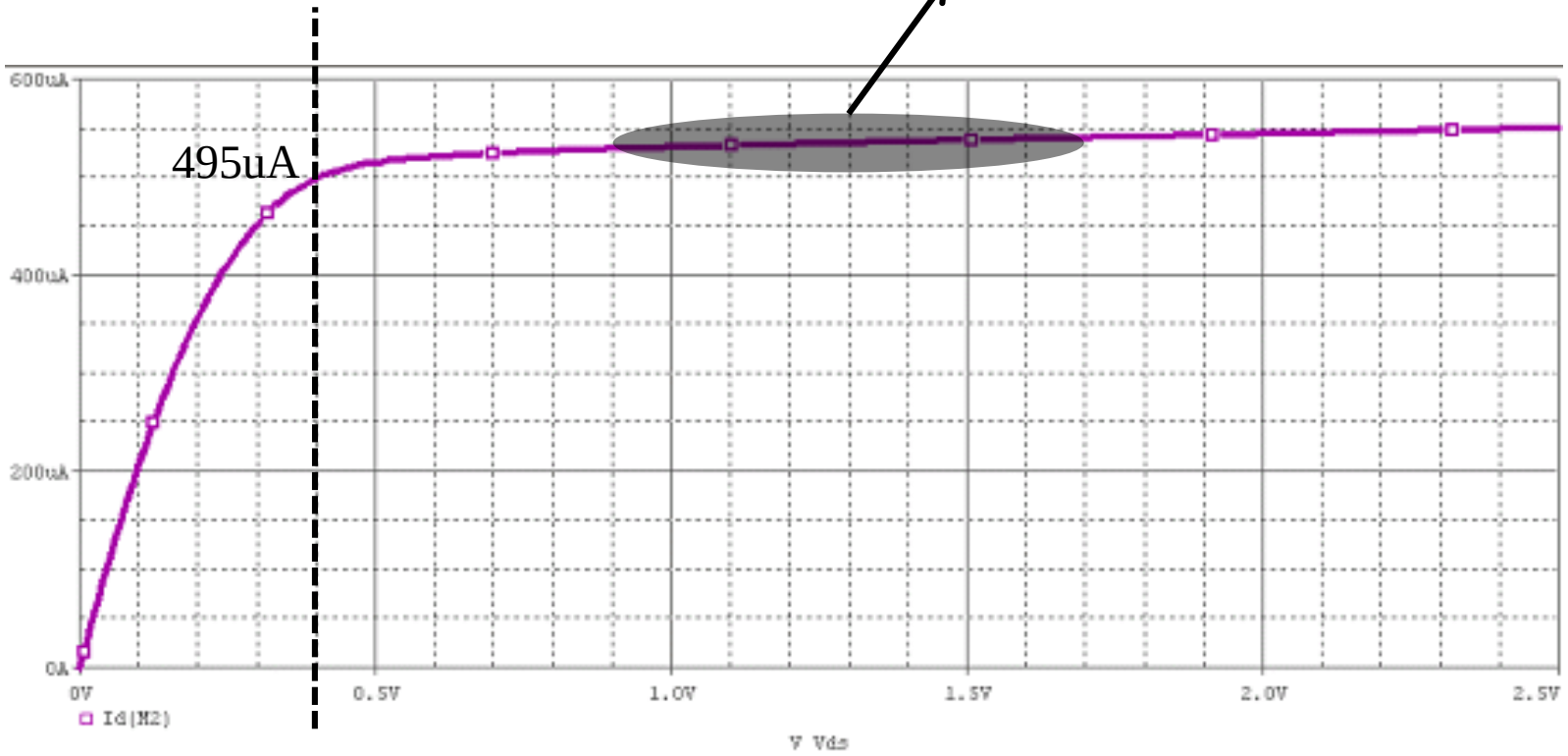


Design Specification

Parameter	Value
Vds	< 0.7V
Output Resistance	>63KOhm
Current Copy	>99%

Simulation Guide

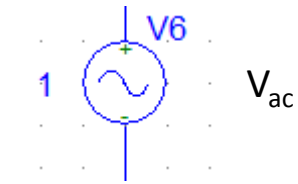
Slope = $1/r_0$ ➔ average slope from 1V to 1.5V



$V_{DS} < 0.7V$

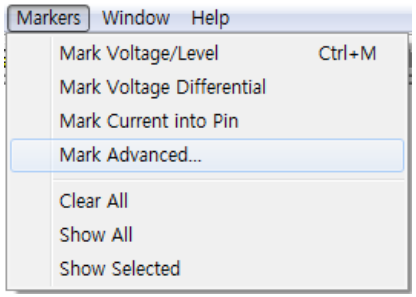
AC Simulation

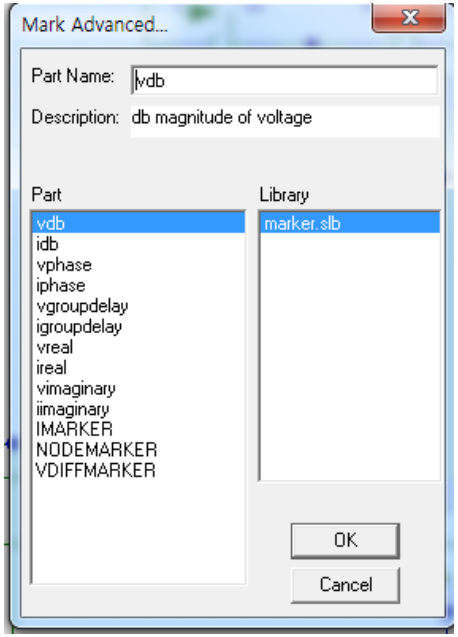
Input

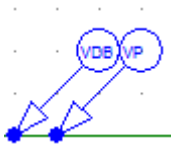


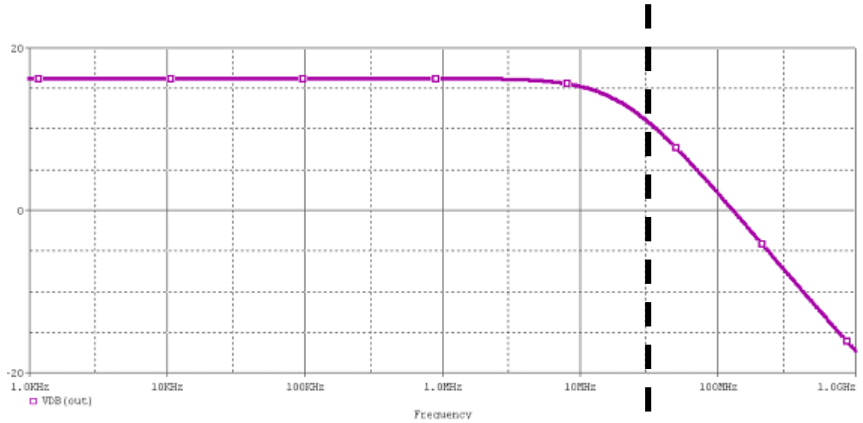
Magnitude = 1

Output







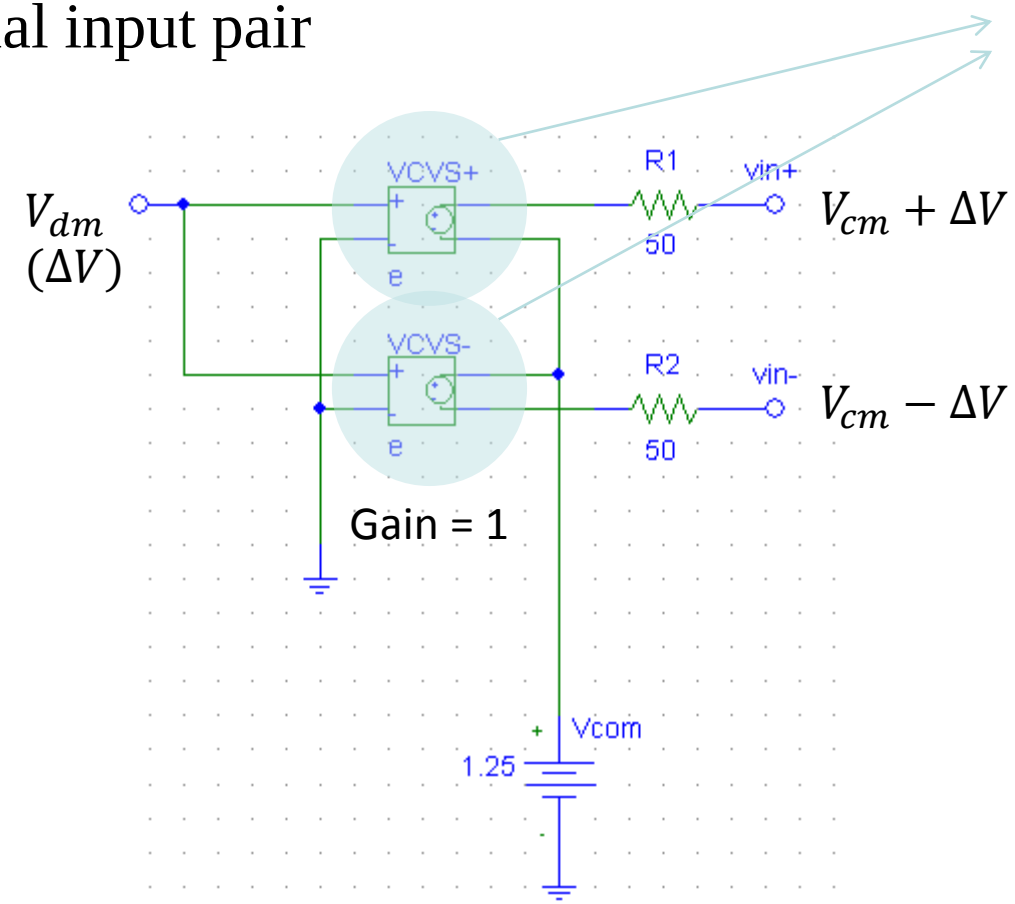


3dB searching ➔ search level(max-3)
cf) search xvalue()

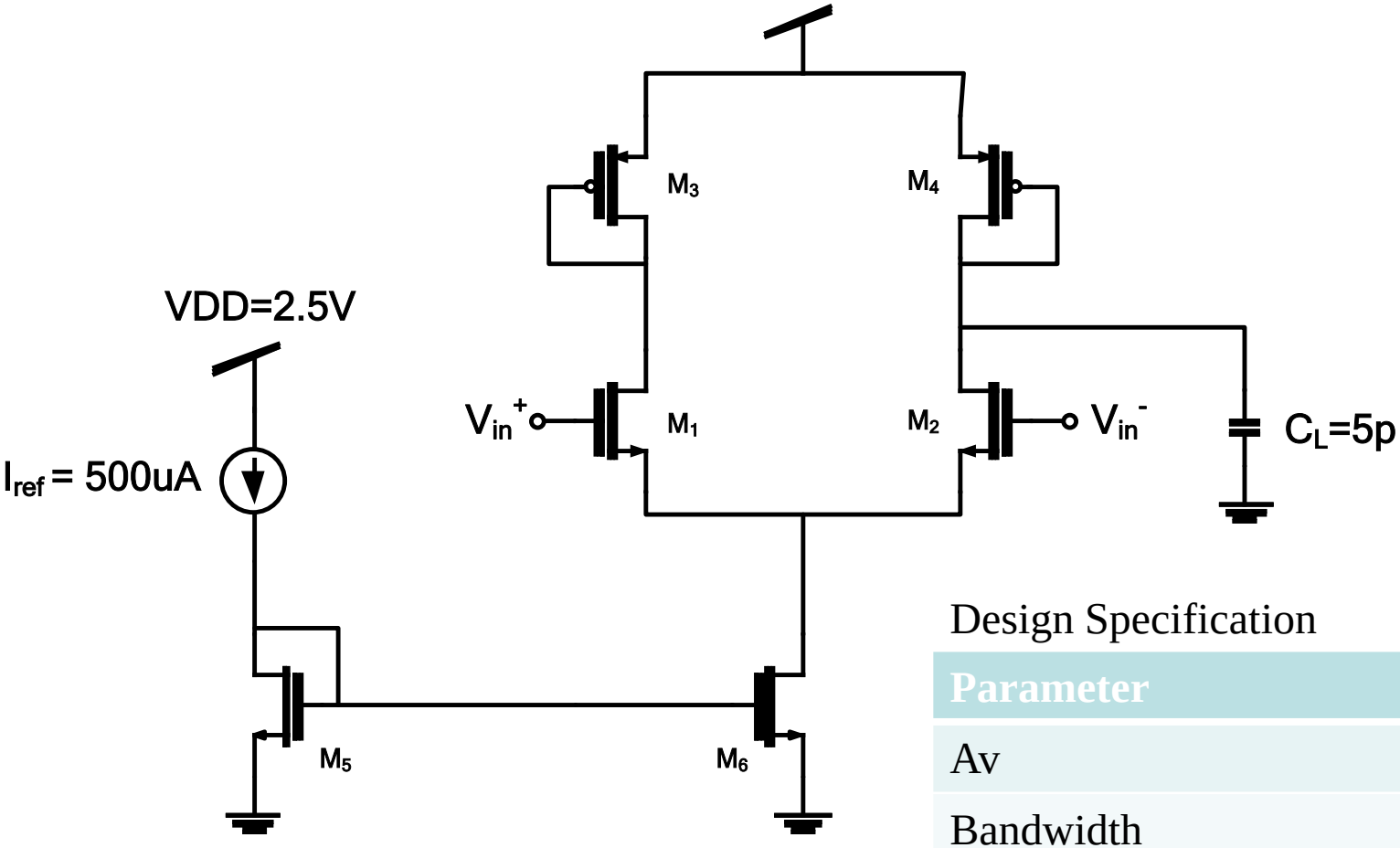
Simulation Tips

Differential input pair

Part Name : ‘e’



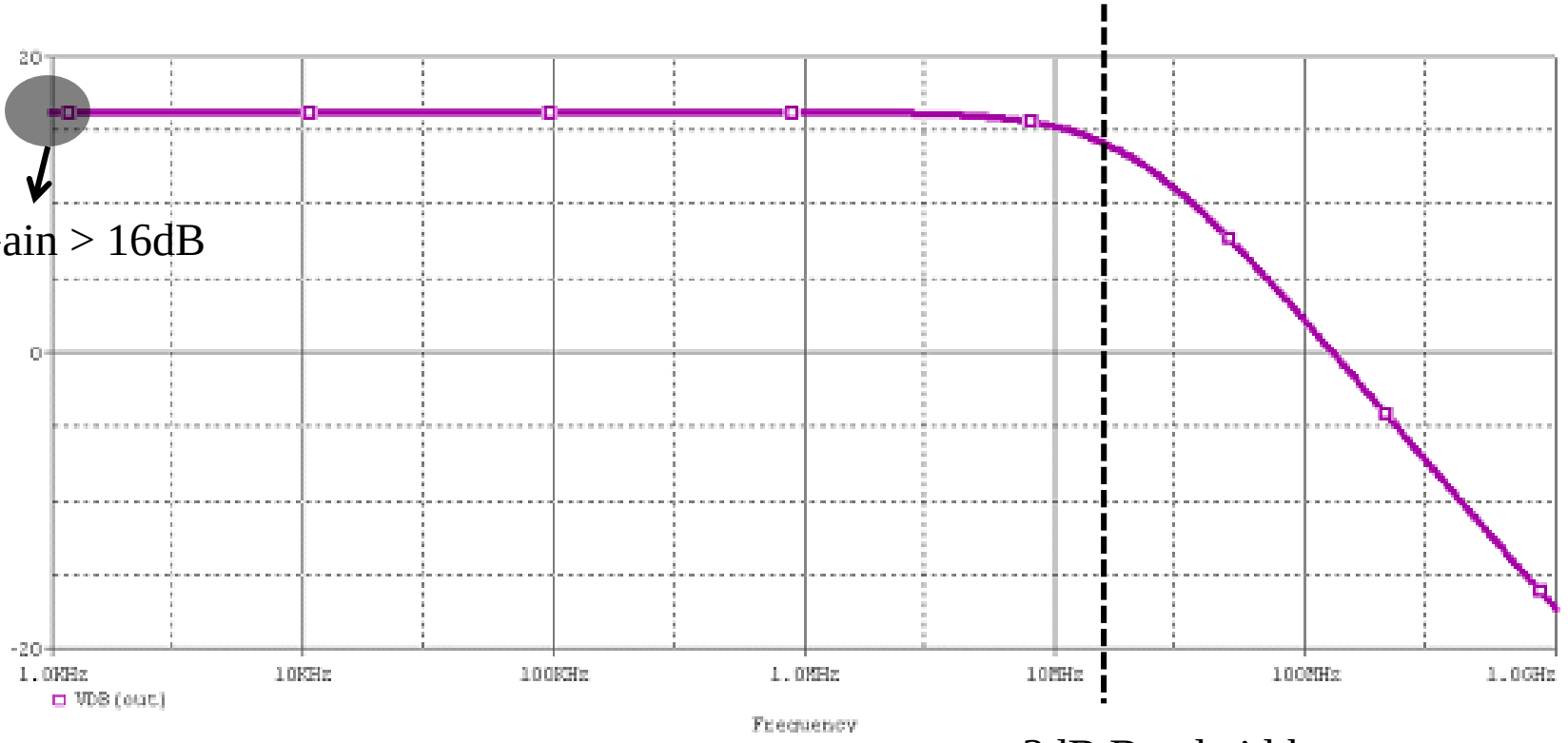
Single-Stage Differential OTA



Design Specification

Parameter	Value
Av	>16dB
Bandwidth	>20MHz
ICMR	>1.1V
Power Consumption	<1.5mW

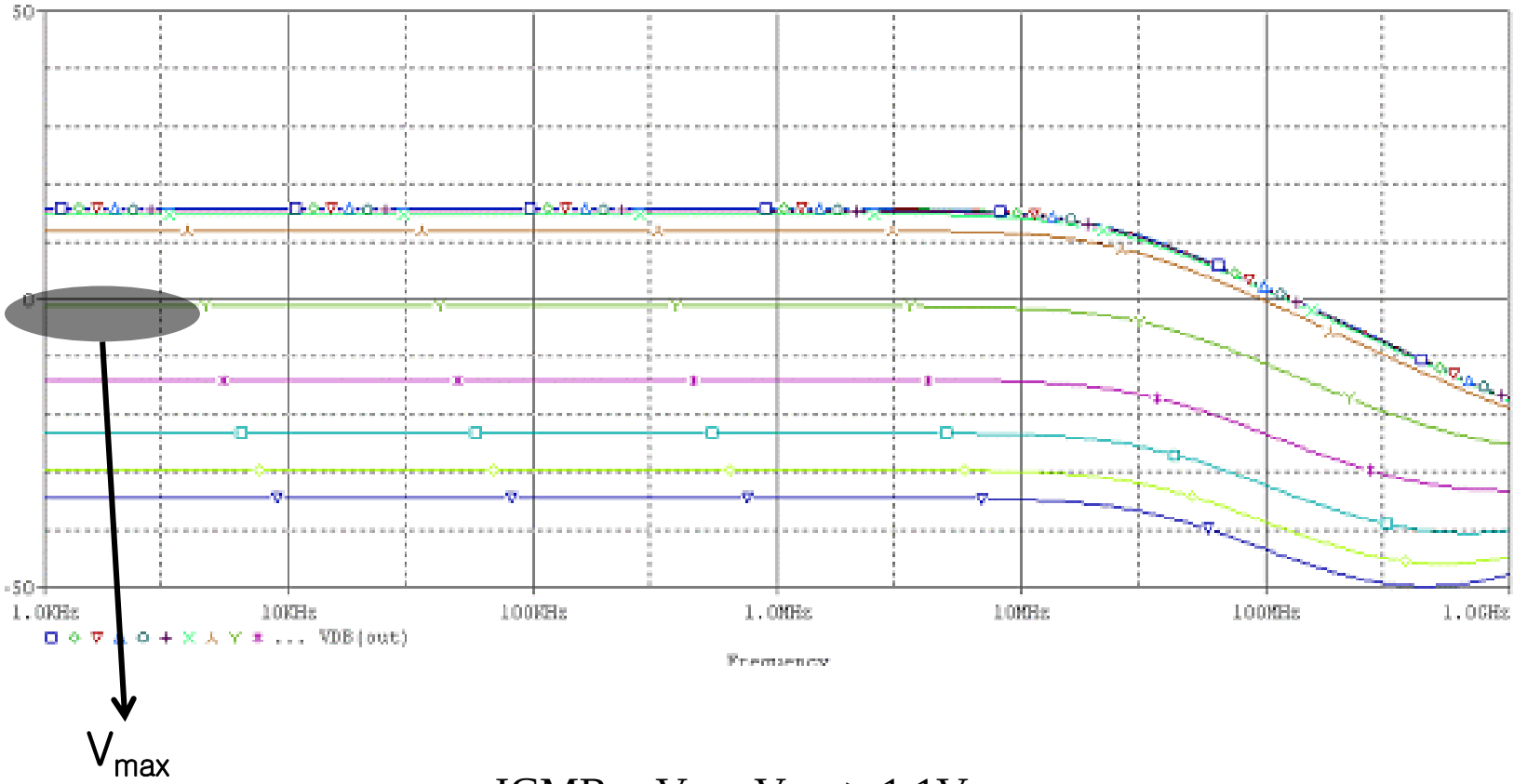
Simulation Guide



DC Gain > 16dB

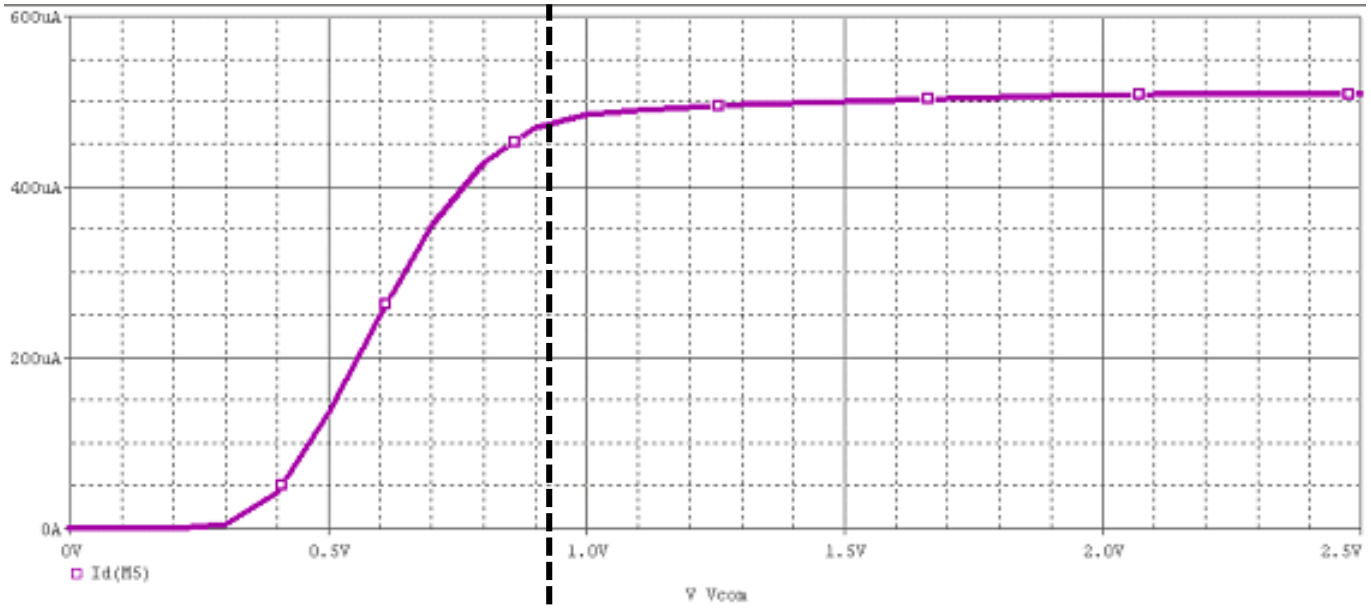
3dB Bandwidth > 20MHz

Simulation Guide



$$ICMR = V_{max}\text{-}V_{min} > 1.1V$$

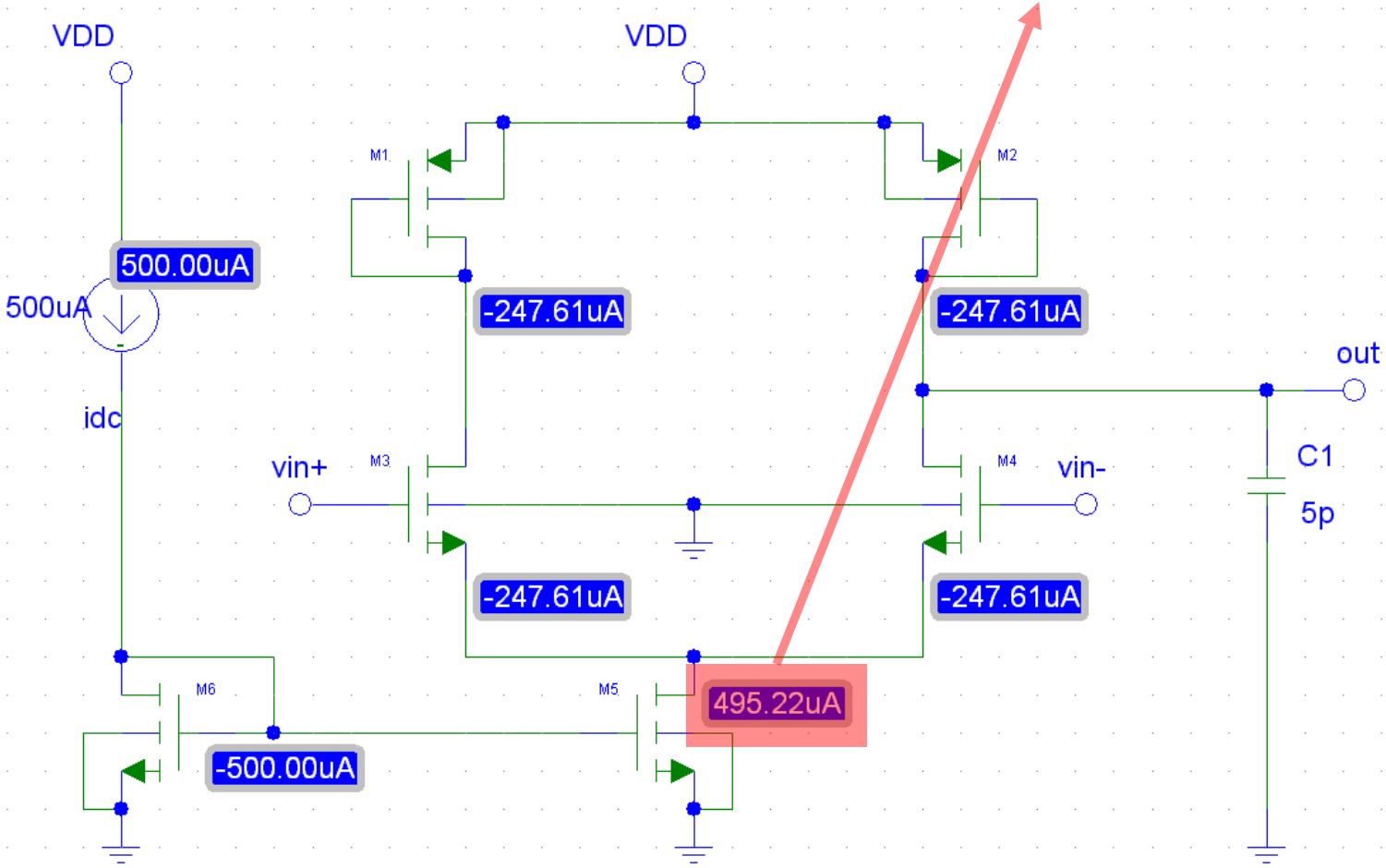
Simulation Guide



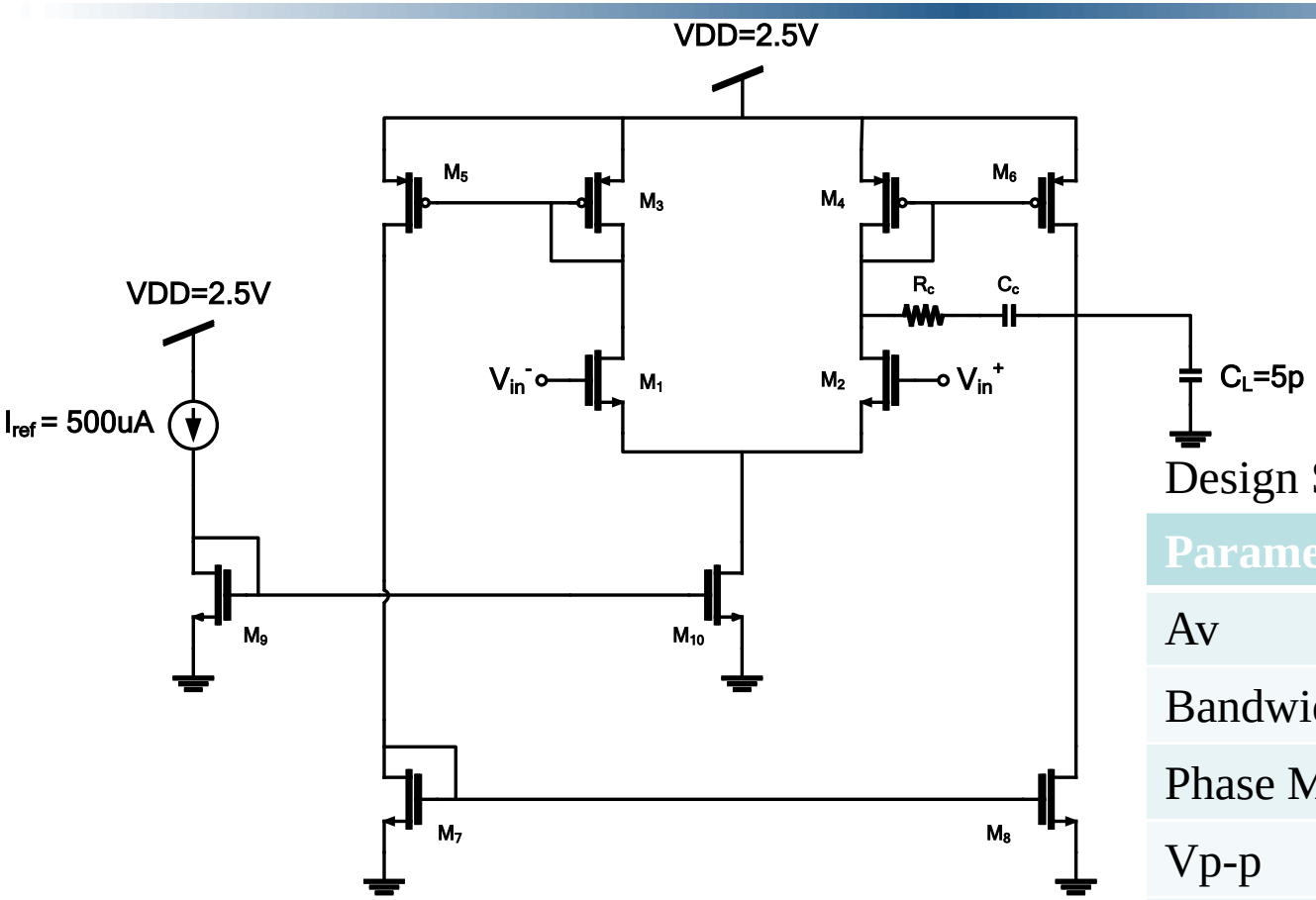
V_{min}
:Current copied 90% @ M6

Simulation Guide

Power = Total Current * VDD < 1.5mW



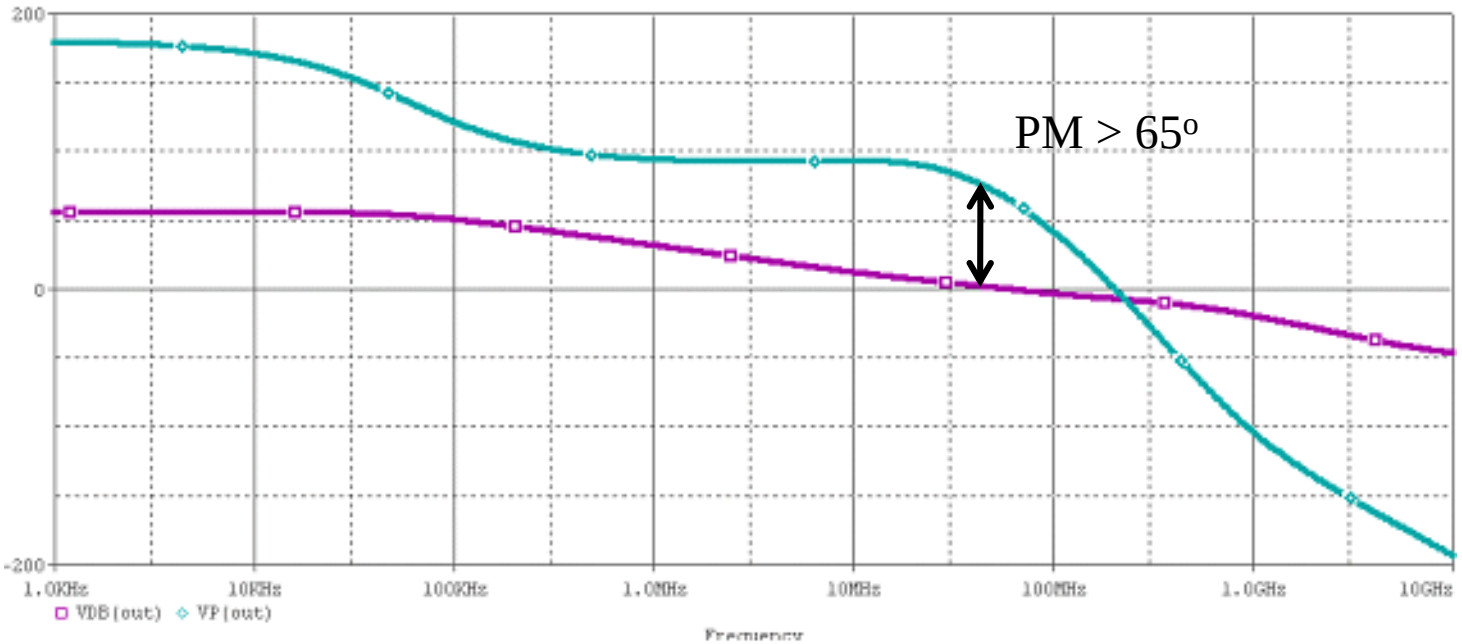
Mirrored OTA



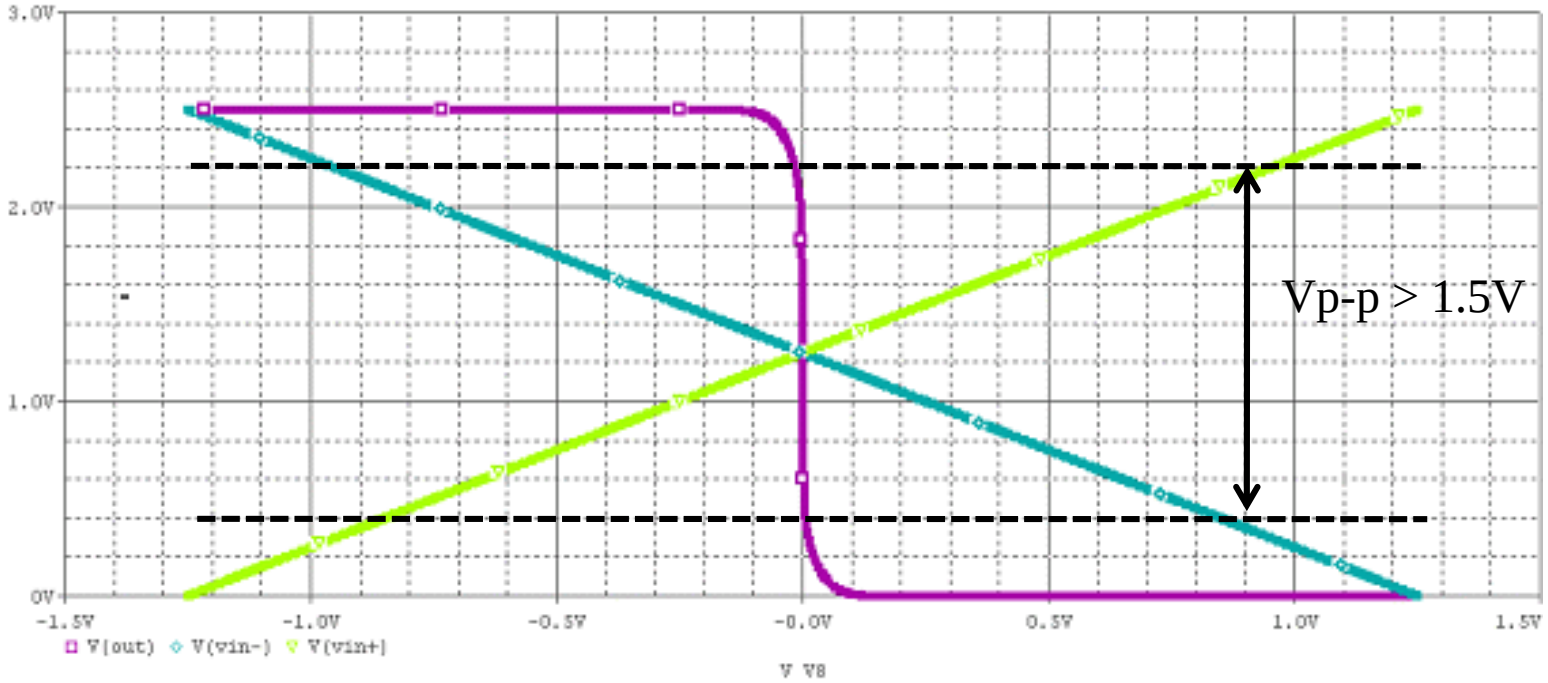
Design Specification

Parameter	Value
Av	>56dB
Bandwidth	>60kHz
Phase Margin	>65
Vp-p	>1.5V
Slew Rate	>13V/us
CMRR	>85dB
Power Consumption	<2.5mW

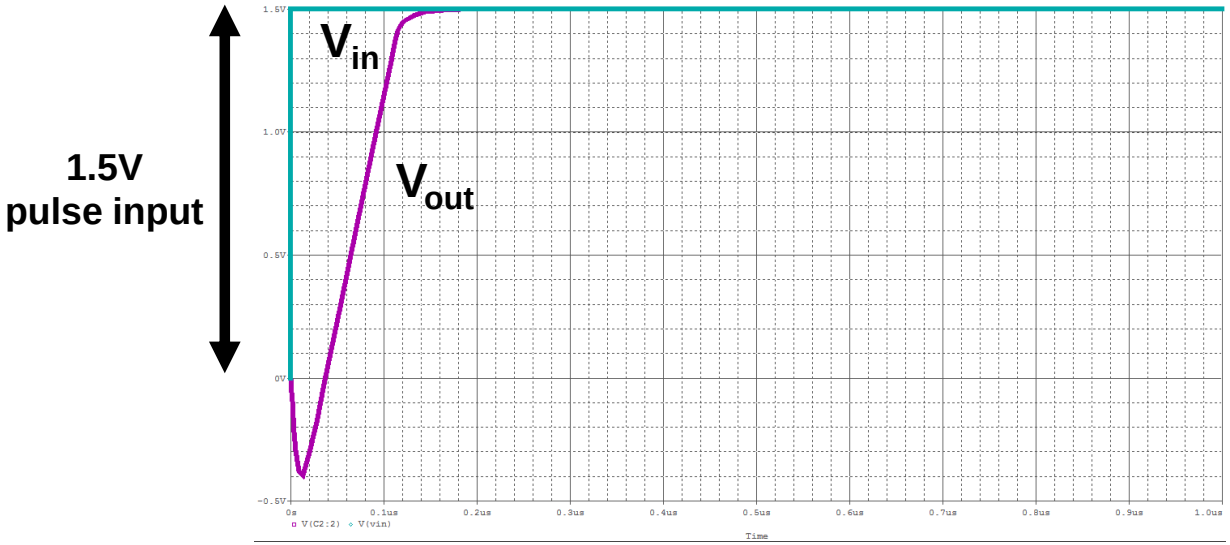
Simulation Guide



Simulation Guide

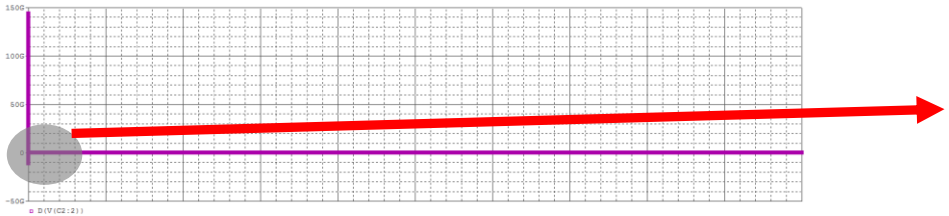


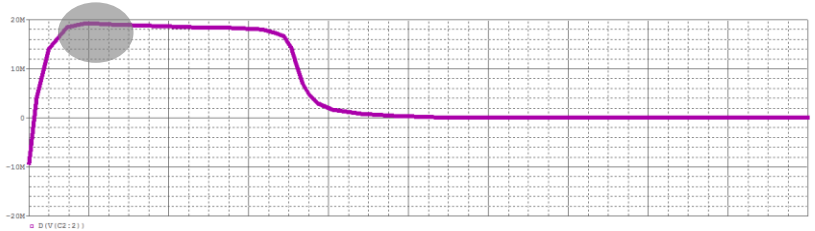
Simulation Guide



Derivative

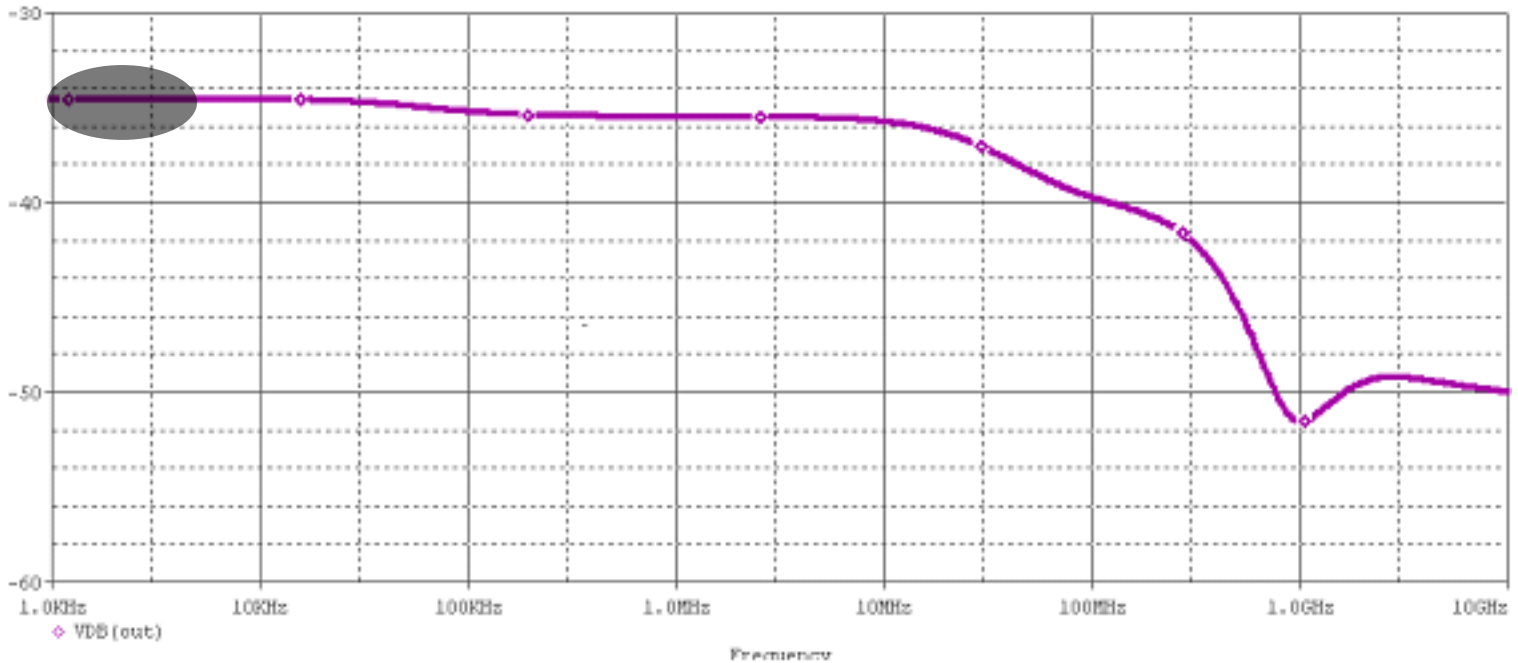
Slew rate > 13M V/s



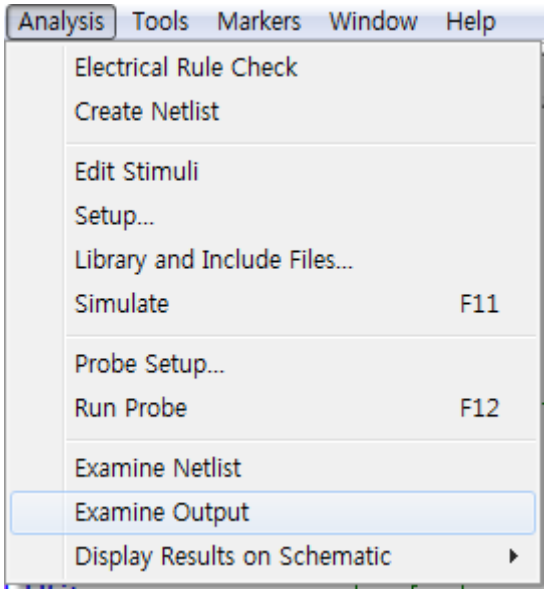


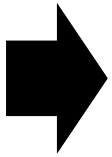
Simulation Guide

CMRR = Adv / Acv > 85dB



Simulation Tips





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**** MOSFETS

NAME         M_M3         M_M4         M_M2         M_M5         M_M1
MODEL        orbit2L2N    orbit2L2N    orbit2L2P    orbit2L2N    orbit2L2P
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I_D, V_{DS}, V_{GS}, V_{TH}, etc…

Grading Policy

- Current mirror[5], Single stage OTA[25], Mirrored OTA[50], Report[20]
- 10 extra points will be given for up to five designs that satisfy all the specifications and produce highest gain-bandwidth products for Part III in the class
- Three best designs will be selected and their designers will be given opportunities to present their results in class in English for extra 5 points.
- GB product = Gain * BW = $10^{\frac{Gain[dB]}{20}}$ * BW[Hz]