Project #3 for Electronic Circuit II

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June 1, 2015

- Deadline : 6:00 pm on June 22, 2015. Penalties for late hand-in.

- Team

Students are expected to form a team of two members to do the project and hand in one project report. Equal grades will be given to the members of the same team. Each team must do its own simulation and analysis.

- MOS PSpice parameters

Use Level 7 PSpice parameters for 0.25㎛ CMOS process. The course homepage has PSpice 9.1 student version, level 7 PSpice parameters as well as PSpice basic manual.

- Design rules

1. VDD = 2.5V
2. 0.25㎛ ≤ length of gate ≤ 2㎛
3. 0.25㎛ ≤ width of gate ≤ 200㎛
4. 0.1 pF ≤ all capacitors ≤ 20 ㎌
5. 0 Ω < all resistors ≤ 800㏀
6. Body of pMOS must connect to VDD
7. Body of nMOS must connect to GND

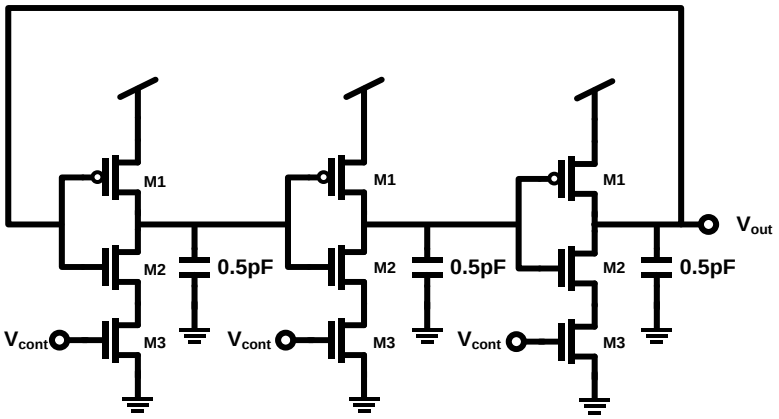
- Goal

You are expected to design a Phase-Locked Loop satisfying given specifications. Your design will be evaluated based on following criteria:

1. How well you satisfy the specifications.
2. How good your settling time of PLL is.
3. How good your design report is.

I. Ring-type Voltage Controlled Oscillator Design [20]

Design a ring-type VCO that satisfies the given design goals. The circuit configuration is given below.



<Fig. 1> Ring-type Voltage Controlled Oscillator schematic

Design Goals	
Parameter	**Value**
Target oscillation frequency	500MHz
Average VCO gain	100MHz/V~ 150MHz/V
Control voltage	0.75~2.25V

You should include the following in the report.

(1) How you achieved design goals.

(2) Simulation results:

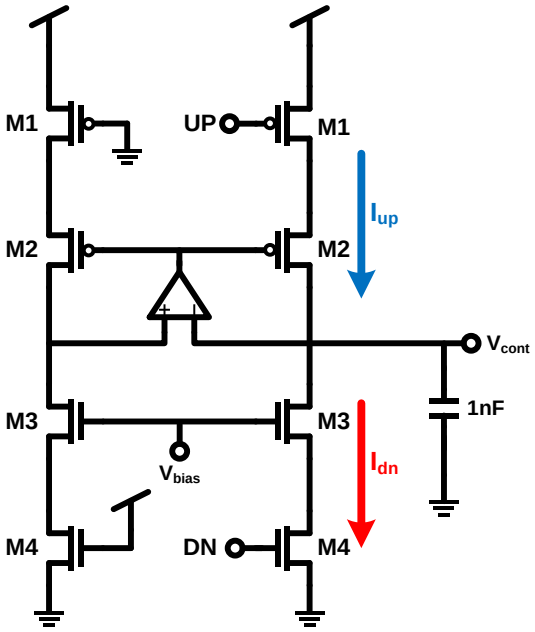
- Plot V_{out} in time domain when the VCO has the oscillation frequency of 500MHz.
- Oscillation frequency vs. V_{cont} plot and discussions.

(3) Average VCO gain (K_{vco})

= (Maximum frequency – Minimum frequency)/1.5

II. Charge Pump Design [20]

Design a charge-pump circuit having the following configuration. The circuit should satisfy design goals given below.



<Fig. 2> Charge pump schematic

Design Goals	
Parameter	**Value**
Up current(I_{up}) & down current(I_{dn}) @ V_{cont} that produces 500MHz in VCO design	4mA~6mA
Mismatch current, $\lvert I_{up} - I_{dn} \rvert$ when UP = 0V, DN = 2.5V	< |50| uA
Available V_{cont} range (V_{cont} satisfying mismatch current condition)	>1.45V

You should include the following items in the report.

(1) How above circuit operates & your design strategy

(2) Simulation results:

- Plot for up & down currents vs control voltage
- Plot for mismatch current vs control voltage

Ⅲ. PLL Design [50]

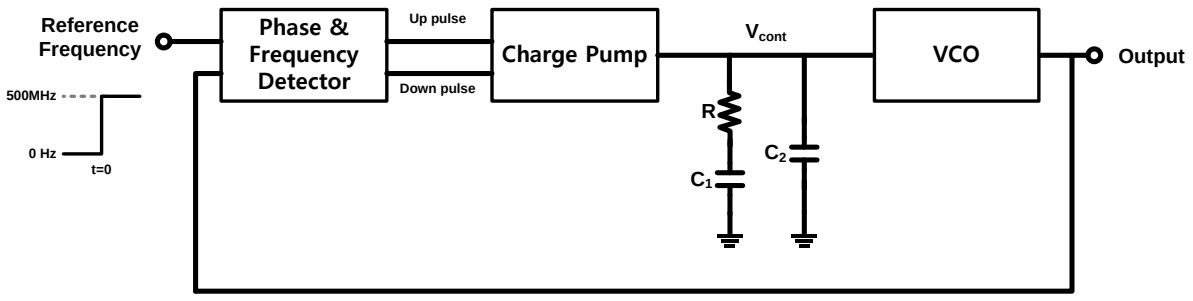
Determine the values for R and C_1 that satisfy the given design goals when resonance frequency (f_0) is 25MHz. Use $C_2 = C_1/10$ and R value should be determined between 580Ω and 600Ω.

(a) Derive the transfer functions of PLL (open-loop and closed-loop) and show Bode plot for each transfer function using MATLAB. For parameter values, use your design results (average VCO gain and charge pump up/down currents) determined in Part Ⅰ & Ⅱ. The transfer functions should satisfy the following design goal. If they do not, you should go back to Part Ⅰ & Ⅱ and re-design your circuits.

Design Goals	
Parameter	**Value**
Phase margin for open-loop transfer function	> 50 deg
Max. peaking for closed-loop transfer function	< 2 dB

(b) Simulate the transient response of V_{cont} when the reference frequency jumps to 500 MHz from 0 Hz at t=0. Do your simulation in MATLAB using PLL Simulink modules provided to you. For the module parameters, use your design results (average VCO gain and charge pump up/down currents, they should be same as those used in Ⅲ(a)) determined in Part Ⅰ & Ⅱ.

Design Goals	
Parameter	**Value**
Settling time (Locking time)	As low as possible



<Fig. 3> PLL block diagram

You should include the following items in the report.

(1) How you derived the transfer functions for (a)

(2) MATLAB code with annotations and Bode plots and discussions for (a)

(3) Transient response of V_{cont} for (b) and discussions. Use the second-order approximation (C_2=0) for your discussion.

(4) Your Simulink diagram for (b)

IV. Design Report [10]

You should write a design report in which you clearly explain how you come up with your transistor W/L values and what values you have achieved for design specifications. All your design results should be summarized in Design Summary Sheet. Place the Design Summary Sheet right after the cover page of your report. Three extra points will be given if your report is written in English.

Design Summary Sheet

Name 1: **Student ID No.:**

Name 2: **Student ID No.:**

< Ring-type VCO Design >

$(W/L)_1$	
$(W/L)_2$	
$(W/L)_3$	
Min. frequency	
Max. frequency	
Average VCO gain	

< Charge pump Design >

$(W/L)_1$	
$(W/L)_2$	
$(W/L)_3$	
$(W/L)_4$	
Up & down current	
Available range	

< PLL Design >

R	
C1	
C2	
Phase margin	
Max. peaking	
Settling(Locking) time	