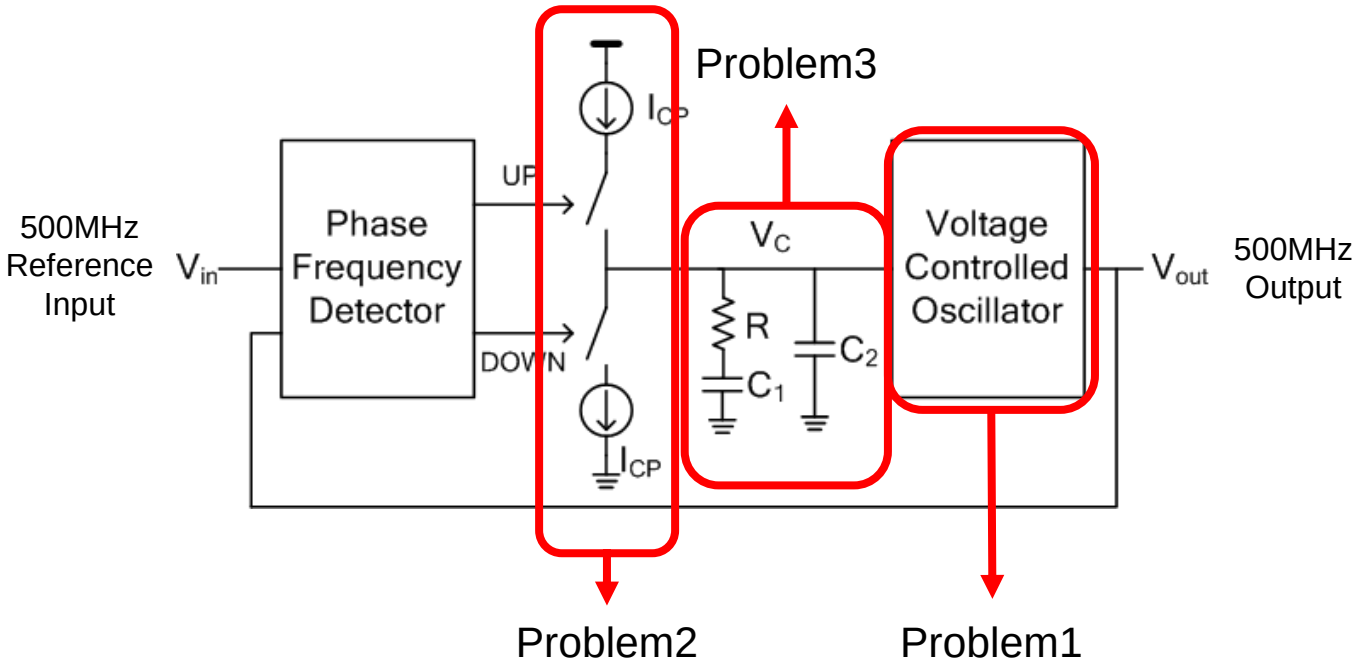
# Project 3
# Design Guide

High-Speed Circuits & Systems Lab.
Dept. of Electrical and Electronic Engineering
Yonsei University

High-Speed Circuits and Systems Laboratory
HSCS

# Goal

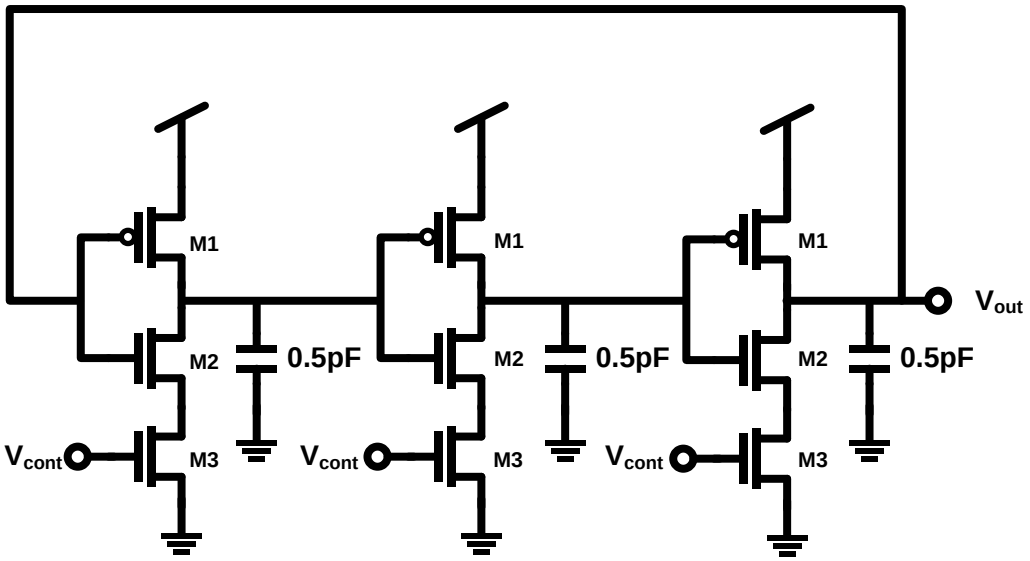



Phase Locked Loop

- ✓ Output clock frequency : 500MHz
- ✓ 2.5V supply voltage
- ✓ $V_{cont}$ : 0.75~2.25V

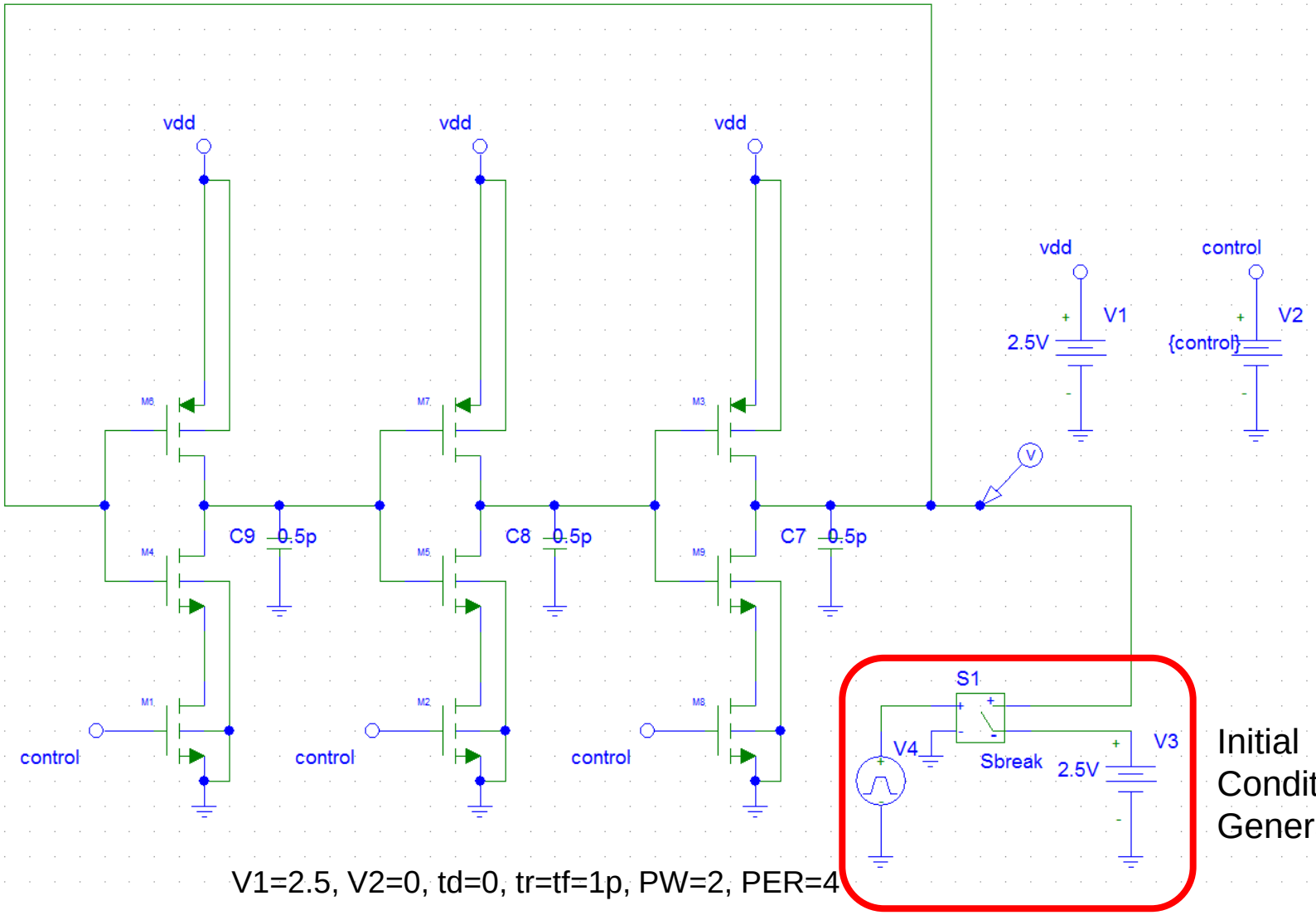
# Problem 1

## I. Ring-type Voltage Controlled Oscillator(VCO) Design[20]




| Design Goals | |
|---|---|
| Parameter | Value |
| Target Oscillation Frequency | 500MHz |
| Average VCO gain | 100MHz/V~150MHz/V |
| $V_{cont}$ | 0.75~2.25V |

# VCO Design



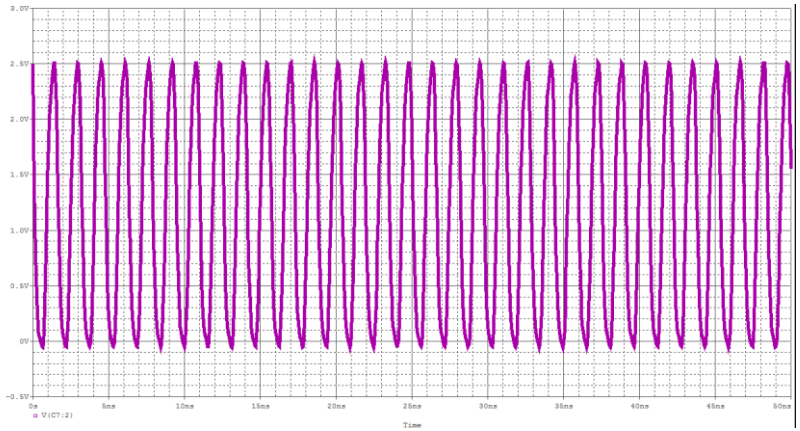

Initial Condition Generator

V1=2.5, V2=0, td=0, tr=tf=1p, PW=2, PER=4

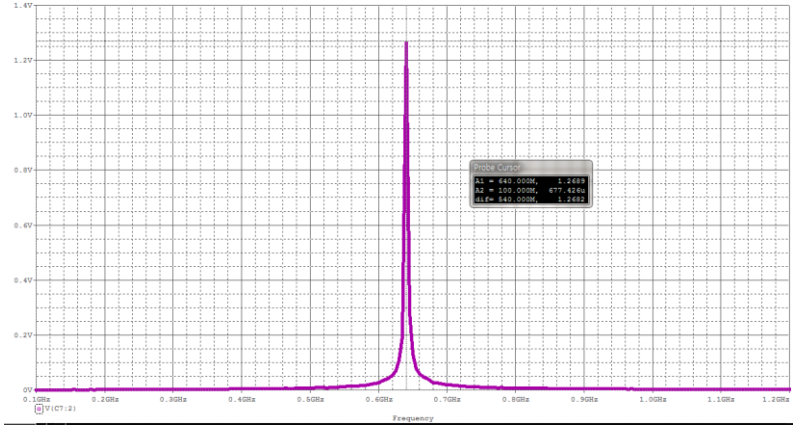
# Simulation Result

**Transient simulation**

- ✓ **Print step : 0.1ns**
- ✓ **Final time : 200ns**



**FFT**

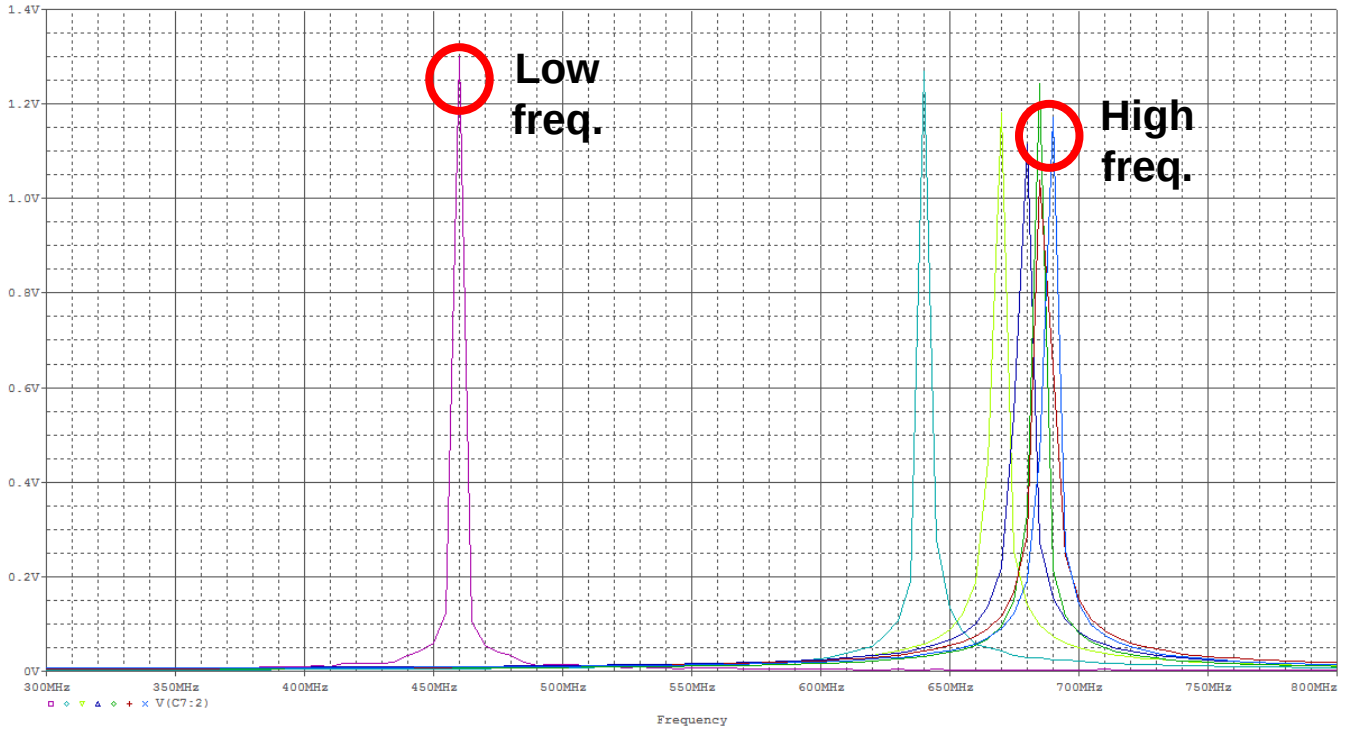


Find point which has maximum value

Determine $V_{cont}$ whose oscillation frequency is 500MHz
➔$V_{cont}$ should be within 0.75V~2.25V

# Simulation Result

**$V_{cont}$ parametric sweep(0.75~2.25V)**



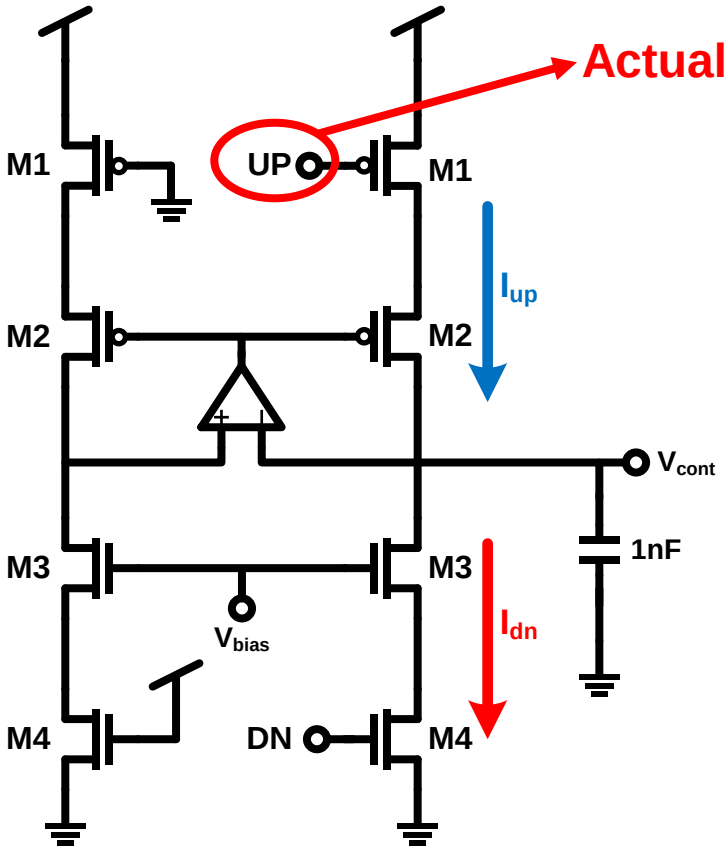

Average VCO gain : (High freq.-Low freq.)/1.5

➔Average VCO gain should be within 100~150MHz/V

➔Plot $V_{cont}$ vs frequency

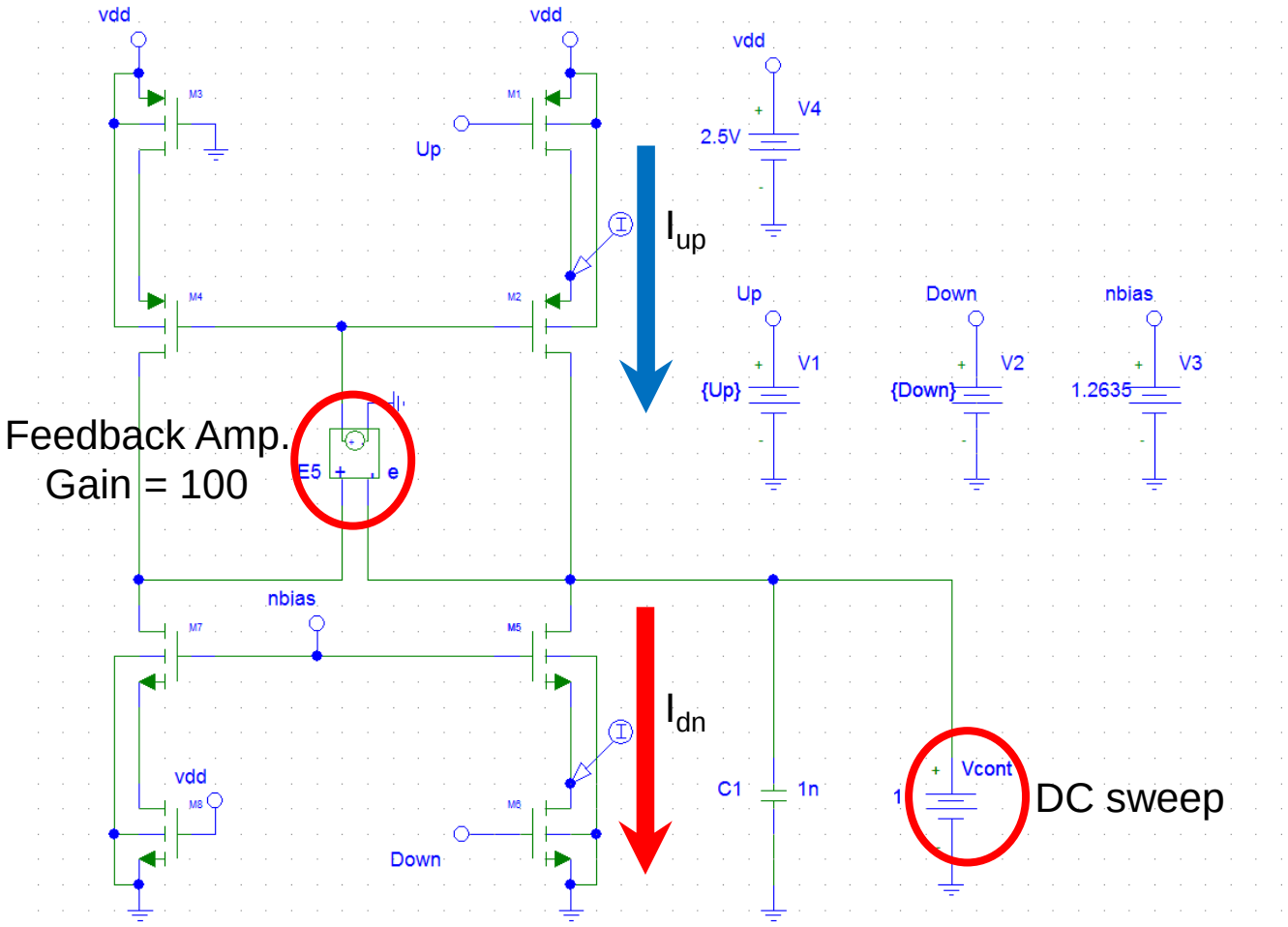
# Problem 2

## II. Charge Pump Design[20]



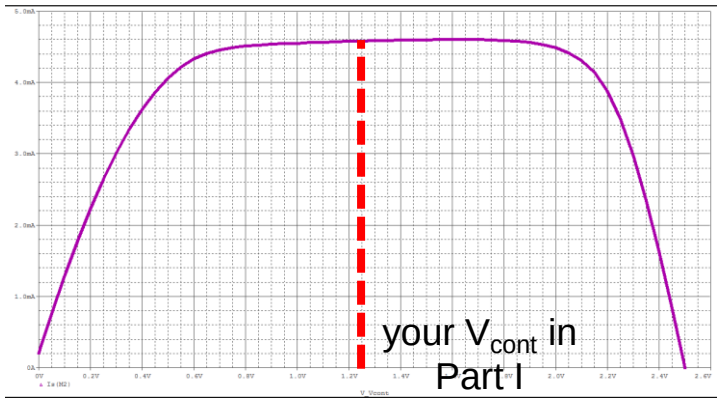

| Design Goals | |
|---|---|
| Parameter | Value |
| Up current($I_{up}$) & down current($I_{dn}$) @ $V_{cont}$ that produces 500MHz in VCO design | 4~6mA |
| Mismatch current, $\lvert I_{up} - I_{dn} \rvert$ when UP = 0V, DN = 2.5V | $<\lvert 50 \rvert \mu A$ |
| Available $V_{cont}$ range ($V_{cont}$ satisfying mismatch current condition) | >1.45V |

# Charge Pump Design

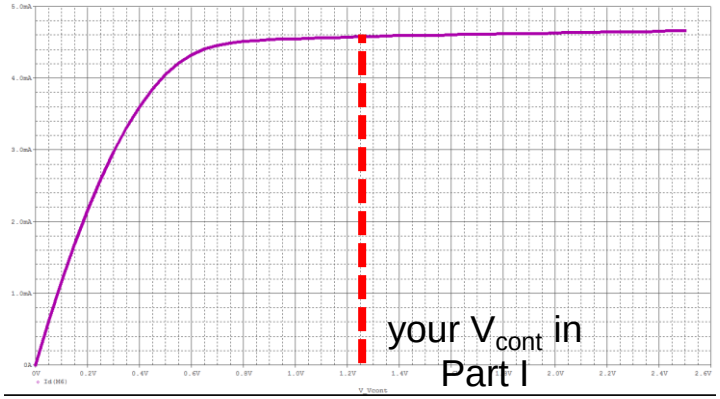


# Simulation Result

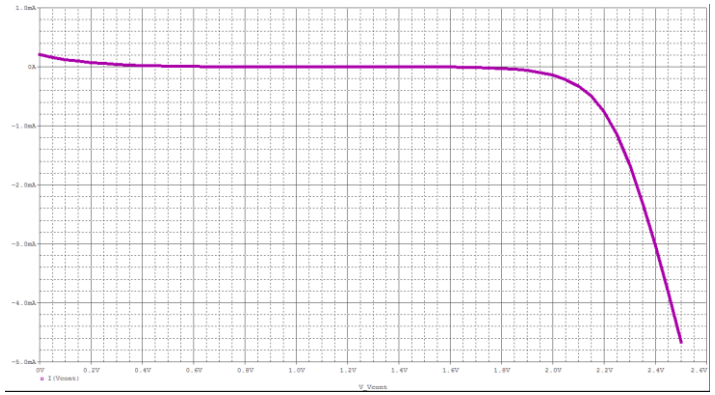
**$V_{cont}$ DC sweep(0~2.5V)**




**<$V_{cont}$ vs $I_{up}$>**




**<$V_{cont}$ vs $I_{dn}$>**

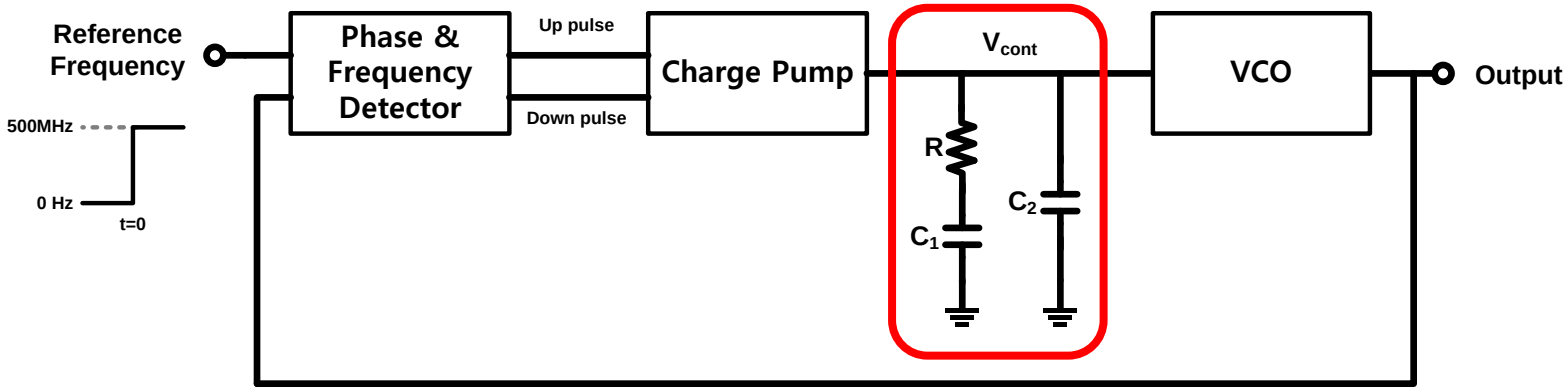


**<$V_{cont}$ vs $I_{up}$-$I_{dn}$>**

1. $I_{up}$ & $I_{dn}$ @ your $V_{cont}$ should be within 4~6mA
2. Mismatch current < $50\mu A$
3. Available $V_{cont}$ range > 1.45V

# Problem 3

## III. PLL Design[50] – MATLAB simulation




- ✓ Determine the values for R & $C_1$ with given conditions following:
- ✓ Resonance frequency($f_0$) = 25MHz, $C_2$=$C_1$/10, $580\Omega \leq R \leq 600\Omega$, $\omega_0 = \sqrt{\frac{I_{cp}K_{VCO}}{2\pi C_1}}$
- ✓ Use design parameters($I_{cp}$ & $K_{VCO}$) determined in Part I&II

<Problem 3(a), frequency response>

**Design Goals**

| Parameter | Value |
|---|---|
| Phase margin for open-loop transfer function | > 50 deg |
| Max. peaking for closed-loop transfer function | < 2dB |

<Problem 3(b), step response(time)>

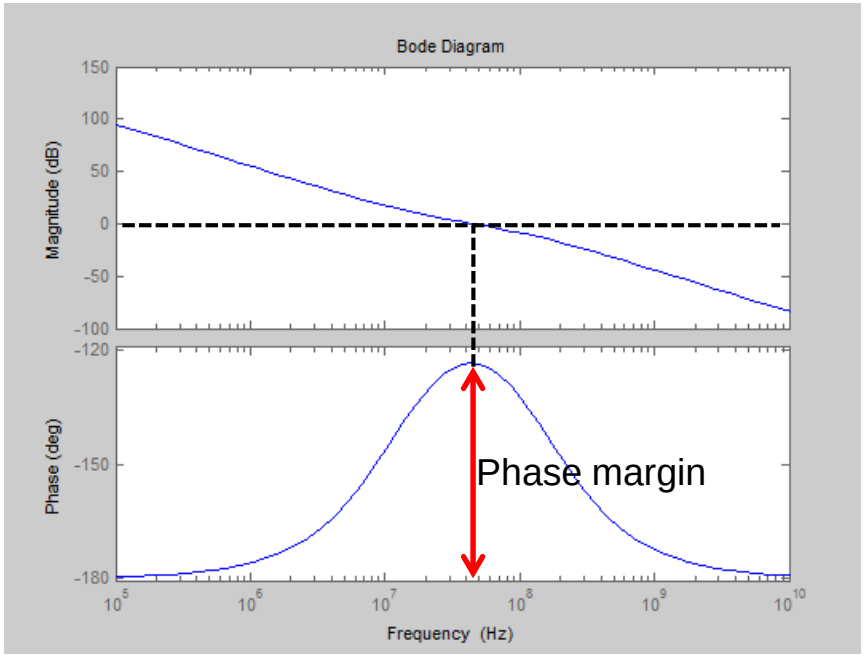
**Design Goals**

| Parameter | Value |
|---|---|
| Settling time (Locking time) | As low as possible |

# Simulation Result

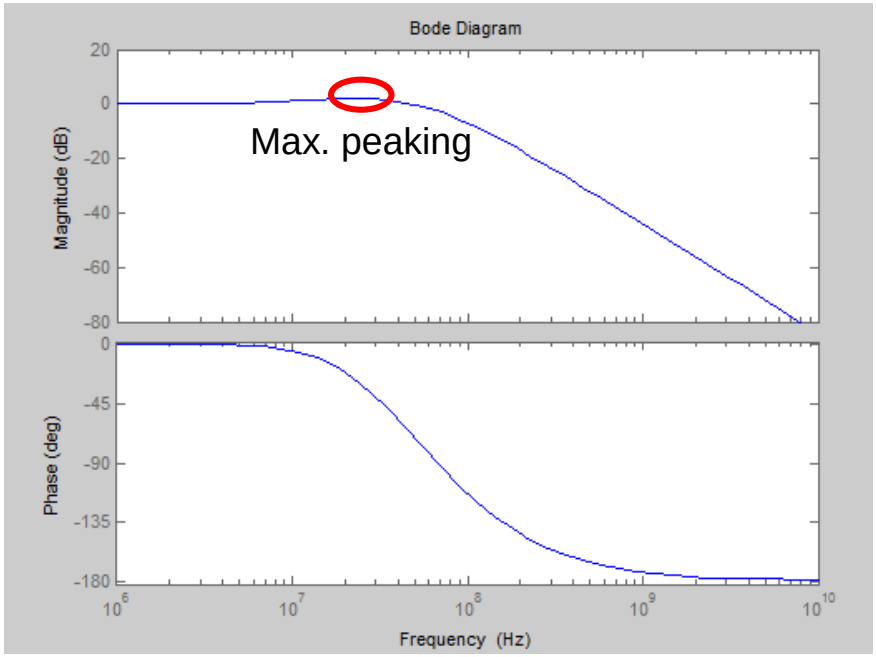
## Problem 3(a) – MATLAB simualtion

Open-loop transfer function




✓ Phase margin > 50deg

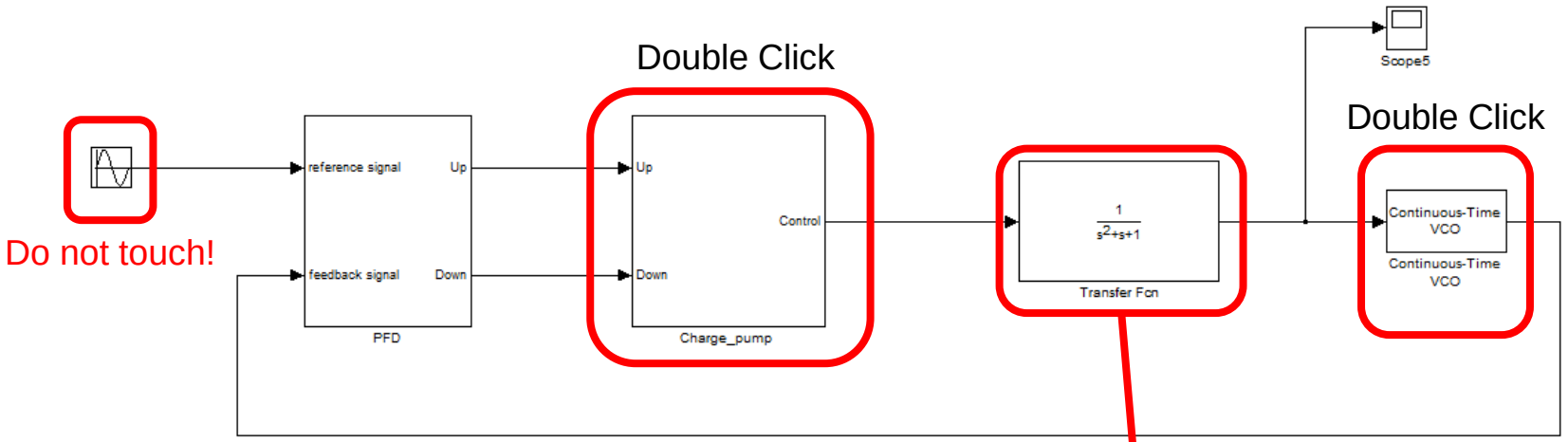
Closed-loop transfer function




✓ Max. peaking < 2dB

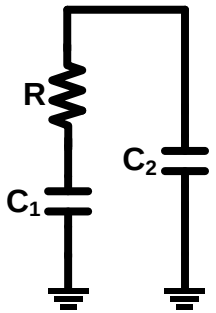
# Simulation Setup

## Problem 3(b) – MATLAB Simulink simulation

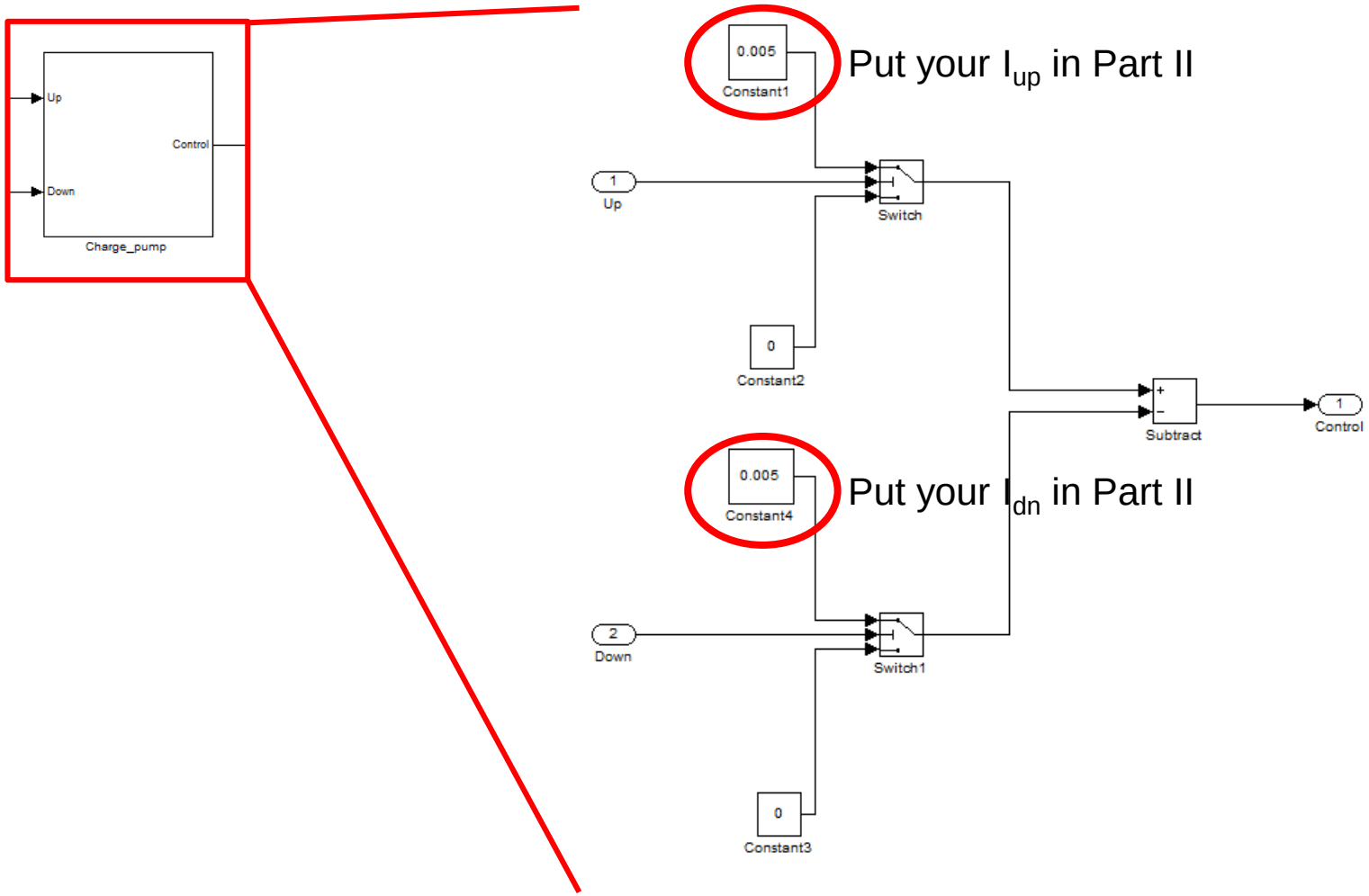



**<Given Simulink PLL module>**

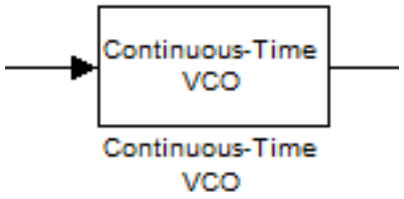
Loop Filter transfer function

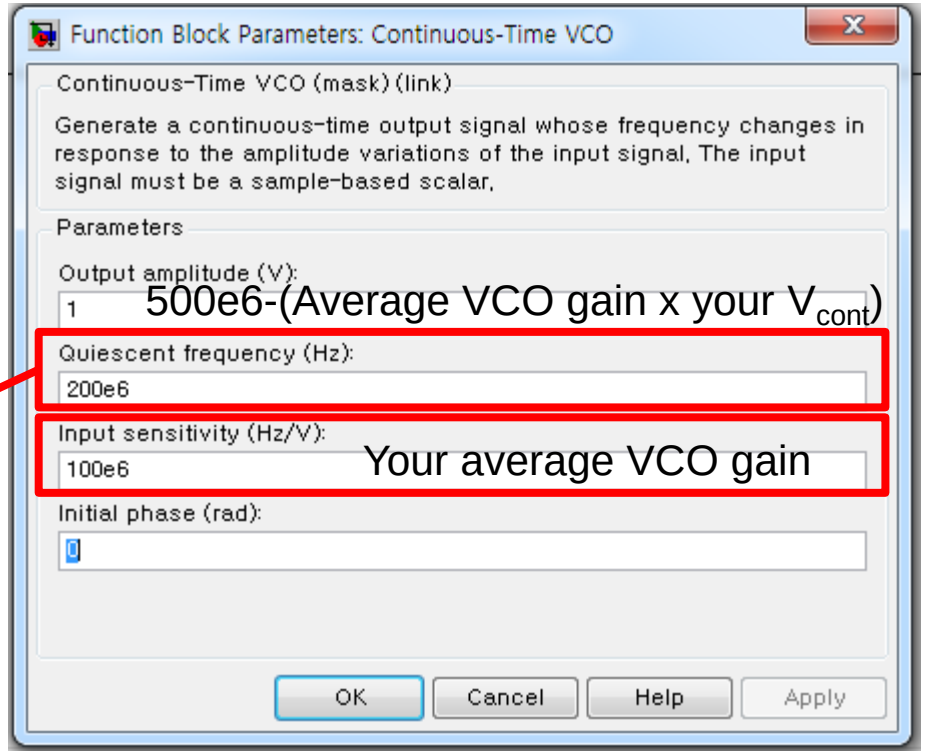


# Simulation Setup



# Simulation Setup

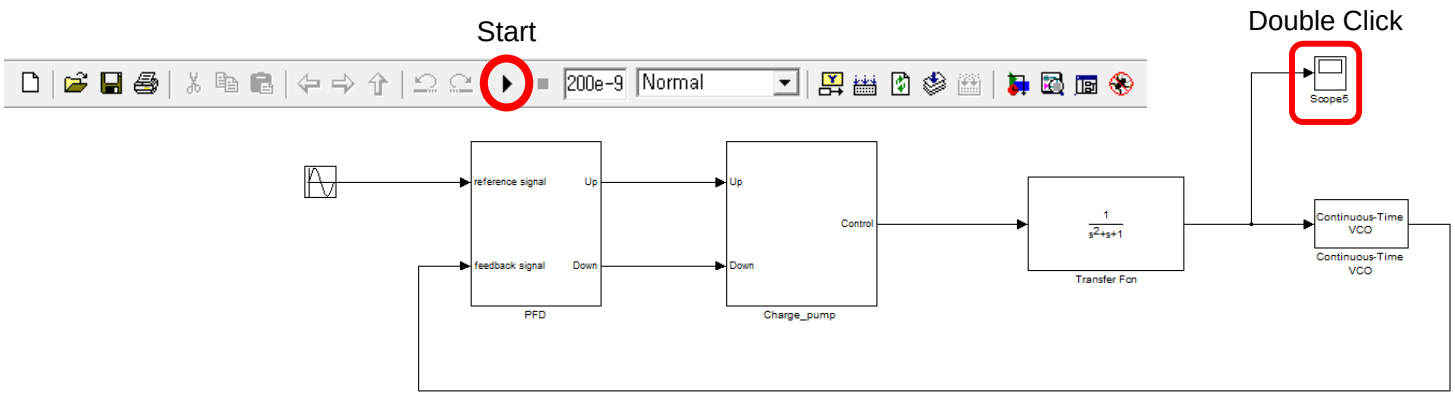



$f_{out} = f_0 + gain \times \mathrm{V_{cont}}$

Quiescent frequency = $f_0$

# Simulation Result

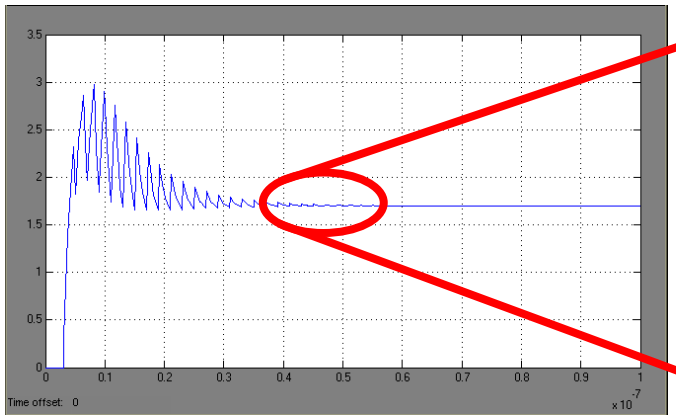


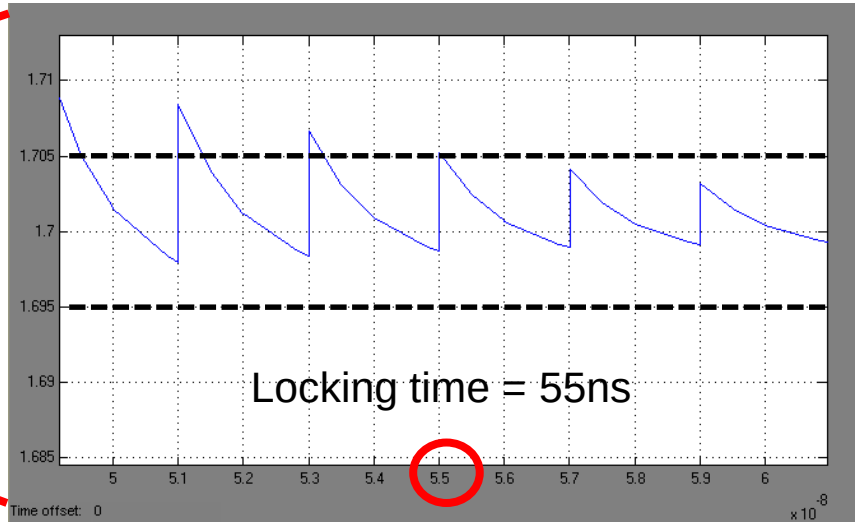

**<Given Simulink PLL module>**

Settling time

your $V_{cont}$-0.005 < Ripple < your $V_{cont}$+ 0.005

ex)your $V_{cont}$=1.7V



# Simulation Tip

✓ MATLAB transfer function

-Sample code for $H(s) = \frac{s+1}{s^2+s+1}$

```
1
2 -    s=tf('s'); %define s-domain
3 -    transfer_function=(s+1)/(s^2+s+1); %put your transfer function
4 -    bode(transfer_function); % bode plot
```

# Grading Policy

- VCO design[20], Charge pump design[20], PLL design[50], Report[10]
- Describe how you get result with reasonable values in detail
- You will get more points for lower settling(locking time)
- Deadline : 6:00 PM , 22 June 2015 @ B629(Hardcopy)