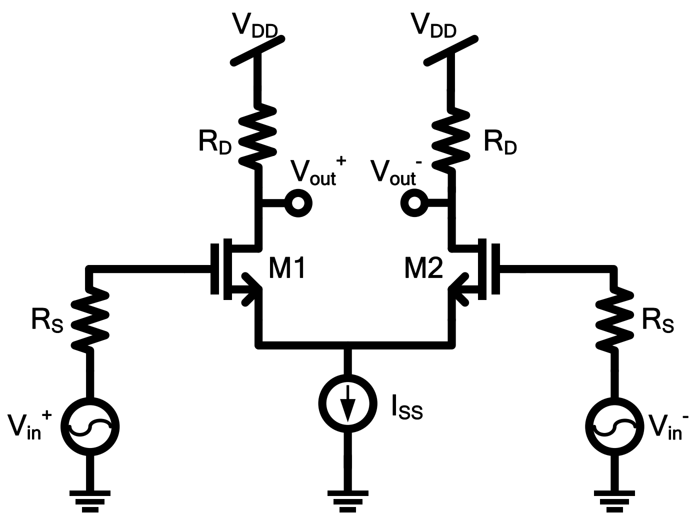
Test #2

June 8, 2015
Electronic Circuits (II)
Prof. Woo-Young Choi
Dept. of Electrical and Electronic Engineering
Yonsei University

Prob.1(30)

Consider the differential amplifier shown below. Assume M1 and M2 are identical, in saturation, have transconductance g_m. The channel length modulation can be ignored for this problem.



(a) (5) Redraw the circuit that contains all the capacitive elements of a MOS transistor, C_{GS}, C_{GD}, C_{SB}, C_{DB}.

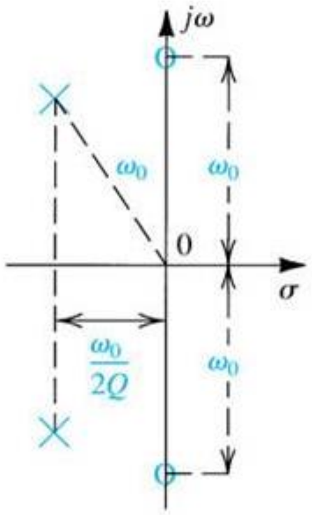
(b) (5) How many poles does the amplifier transfer function, $[V_{out}^+(s) - V_{out}^-(s)] / [V_{in}^+(s) - V_{in}^-(s)]$, have? What are the pole angular frequencies? Use the Miller's theorem for this problem.

(c) (10) Determine the 3-dB bandwidth in Hz of the amplifier from the results obtained in (b). Assume resistance values for R_s and R_D are compatible, and capacitance values for are compatible C_{GS}, C_{GD}, C_{SB}, C_{DB}.

(d) (10) Determine f_t, the unit-gain frequency in Hz of this amplifier using the Miller's theorem.

Prob.2 (30)

Consider a filter having the following pole-zero diagram (Q > 1/2)

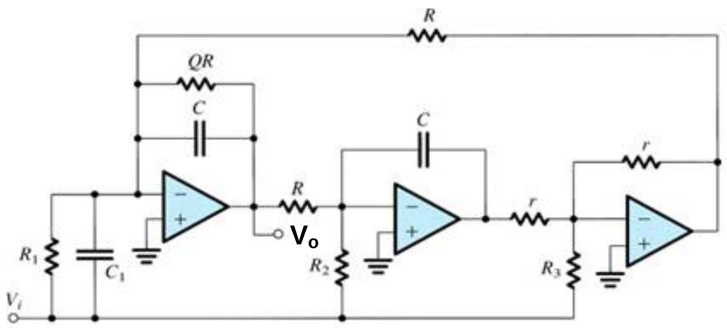


(a) (5) Determine the filter transfer function T(s). Normalize the transfer function so that T(s=0)=1.

(b) (5) Sketch the magnitude Bode plot of this filter. In your sketch, clearly indicate the locations and the values of any peaks.

(c) (10) Design this filter using passive components such as R, L, C. Specify conditions that R,L,C have to satisfy in terms of ω_0 and Q.

(d) (10) Design this filter using the Tow-Thomas biquad shown below. Redraw your Tow-Thomas filter including only the necessary components and specify the conditions that necessary components have to satisfy in terms of ω_0 and Q. You may satisfy only the magnitude of the filter.



Prob. 3 (20)

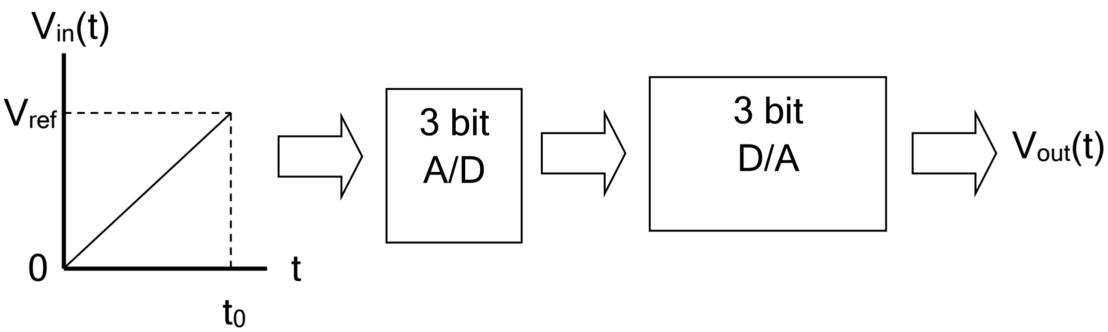
Give the transistor-level CMOS logic circuit for each of the following logic functions. You may use only NMOS and PMOS transistors in your answer.

(a) (10) $Y = ABC + D$

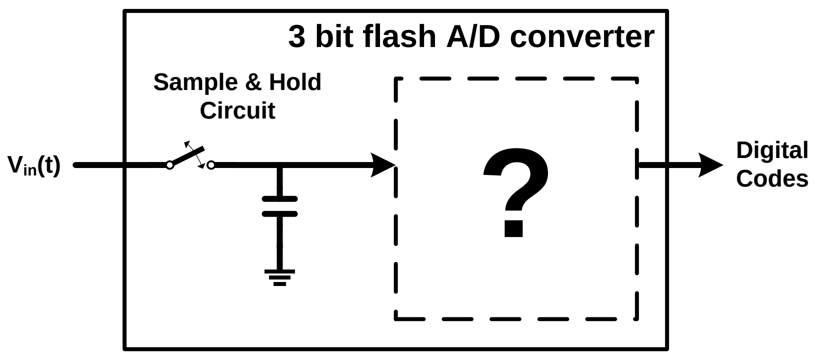
(b) (10) $Y = A \oplus B$ (A XOR B)

Prob. 4 (20)

We want convert $V_{in}(t)$ into binary codes and then back into analog signals using 3-bit A/D and 3-bit D/A as shown below. Assume the operation voltage ranges for A/D and D/A converters are from 0 to V_{ref}.



(a) (5) Complete the block diagram of a 3-bit flash A/D converter shown below.



(b) (5) Show the output binary code of the A/D converter as function of time.

(c) (5) Show the block diagram of 3-bit D/A converter based on R-2R ladder. Clearly indicate how the A/D output (b1, b2, b3 with b1 MSB) is connected to the D/A converter.

(d) (5) Plot the output of the D/A converter as function of time