

Lect. 1: Introduction

- Goals:
 - Review basics of MOS electronic circuits
 - Learn more about MOS electronic circuits
 - Practice technical presentation in English
- Teaching Staff
 - Lecturer: Prof. Woo-Young Choi (최우영)
Room: B625, Tel: 2123-2874
Email: wchoi@yonsei.ac.kr, Web: tera.yonsei.ac.kr
 - T.A.'s : Dongsung Kim (tongsungk@gmail.com, 010-7206-2272)
Minkyu Kim (minkyu226@gmail.com, 010-9265-9226)
Room: B629, Tel: 2123-7709
- Class Hours
 - Lecture: Mon. 14:00-15:50, Wed. 13:00-13:50 at B731
 - TA Session: Mon. 12:00-13:00 at B731
- Prerequisite: A passing grade in Electronic Circuits I

Lect. 1: Introduction

- Textbook: **Fundamentals of Microelectronics** by Razavi
- Class web page: tera.yonsei.ac.kr (Click Classes)
Lecture notes will be available in PDF files before the class
- Grades
 - Tests: $20 \times 3 = 60$ points
 - Projects: $15 + 15 = 30$ points
 - Presentation: 5 points
 - Attendance and Homework: 5 points
- Attendance:
Absent: - 0.5 point, Late: - 0.25 point
- Homeworks.: roughly one h.w. problem for one lecture
No homework: - 1.0 points, Suspected of copying: -3 points
- ➔ Max. penalty points for attendance and H.W. : - 5 points

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● 5 min. Review Presentation

Every student will have a chance to make 5 min. review presentation in English on the previous lecture materials. Students will be grouped into a pair of two students. One pair is responsible for a review of one lecture. The review presentation will be made by one randomly selected from two in the pair. Evaluation will be made based on how well the presenter understands and presents the review materials. Review presentation will start next week and a sign-up sheet will be available on this Wed during the class.

● Lunch Meeting:

Students are encouraged to participate in lunch meetings with fellow students and professor. Lunch meetings will be held on Wednesday from 12:00 - 12:50 in my office. Sign-up sheets will be available. We can have free conversation on the course, future career plans, etc. Sandwiches and drinks will be provided. A sign-up sheet will be available soon.

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- **Class Schedule (Tentative and subject to changes)**

- Part 1: Review
- Part 2: Frequency Response (Chap. 11 in Razavi)
- Part 3: Feedback (Chap. 12 in Razavi)
- Part 4: Analog Filters (Chap. 14 in Razavi)
- Part 5: Additional Topics in Electronics

Lect. 1: Introduction

- **Class Schedule (Tentative and subject to changes)**

- **Part 1: Review**

Lect. 1: Introduction

Lect. 2: MOS Transistors 1

Lect. 3: MOS Transistors 2

Lect. 4: MOS Amplifiers 1

Lect. 5: MOS Amplifiers 2

Lect. 6: MOS Amplifiers 3

Lect. 7: Current Mirrors and Cascode Amplifiers

Lect. 8: Differential Amplifiers

Test 1 (Part 1): 3/23

Lect. 1: Introduction

● Class Schedule (Tentative and subject to changes)

- Part 2: Frequency Response

Lect. 9: Pole, Zero, Bode Plot

Lect. 10: High-Frequency Response of MOS Transistors

Lect. 11: High-Frequency Response of MOS Amplifiers

- Part 3: Feedback

Lect. 12: Properties of Negative Feedback

Lect. 13: Feedback Topologies 1

Lect. 14: Feedback Topologies 2

Lect. 15: Feedback Topologies 3

Lect. 16: High-Frequency Response of MOS Amplifiers

Test 2(Part 2 and 3): 4/27

Design Project 1 (Part 1,2,3): deadline TBD

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● Class Schedule (Tentative and subject to changes)

-Part 4 : Filters

Lect. 17: First-Order Filters

Lect. 18: 2nd-order passive filters

Lect. 19: Second-order active filters

Lect. 20: Integrator-based biquad

Lect. 21: Approximation of Filter Response

Lect. 22: Switched Capacitor Filters

-Part 5 : Additional Topics in Electronics

Lect. 23: Inverters

Lect. 24: CMOS Logic Gates

Lect. 25: Phase-Locked Loops 1

Lect. 26: Phase-Locked Loops 2

Lect. 27 : Data Converters

Test 3 (Part 1,2,3,4): 6/1

Design Project 2 (Part 4,5): deadline TBD