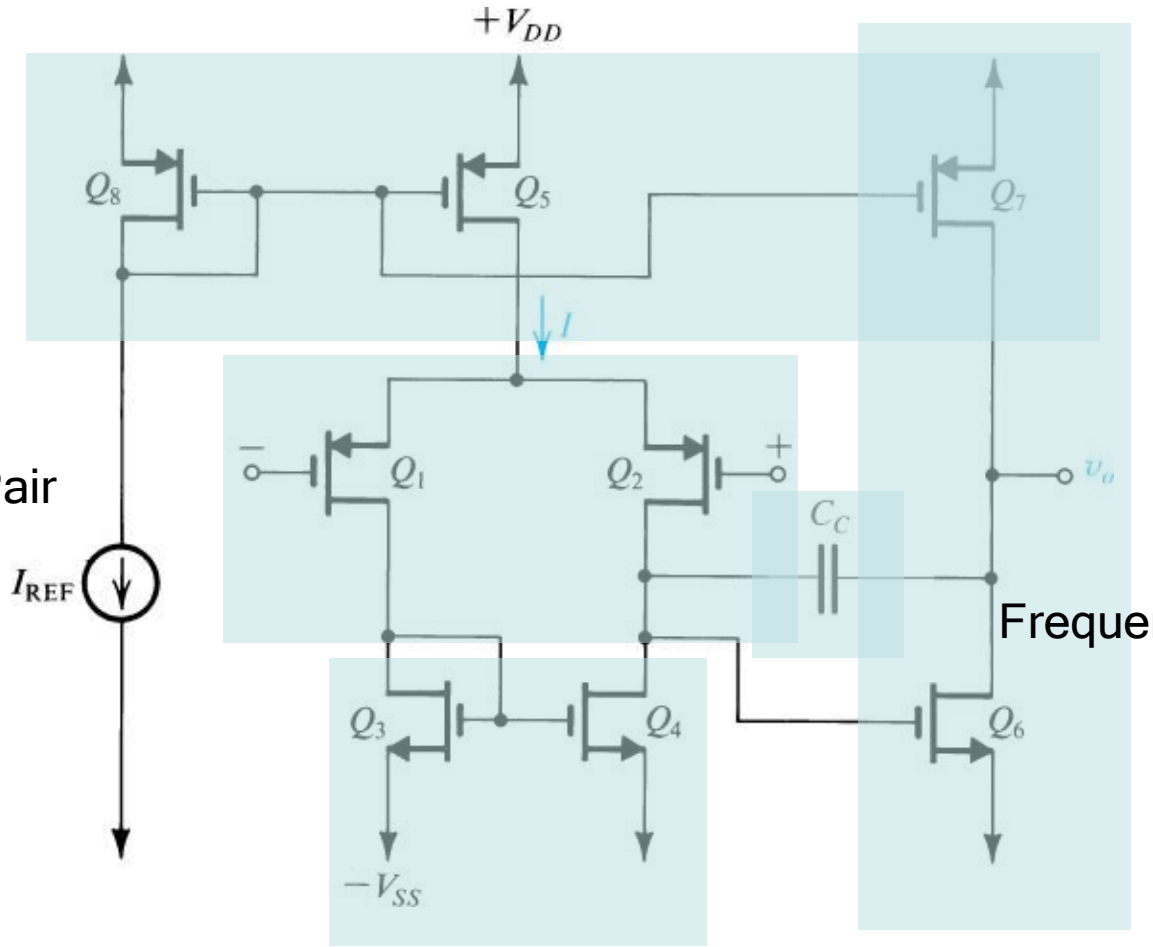
Lect. 15: Two-Stage Amplifier



Current Mirrors

Differential Pair

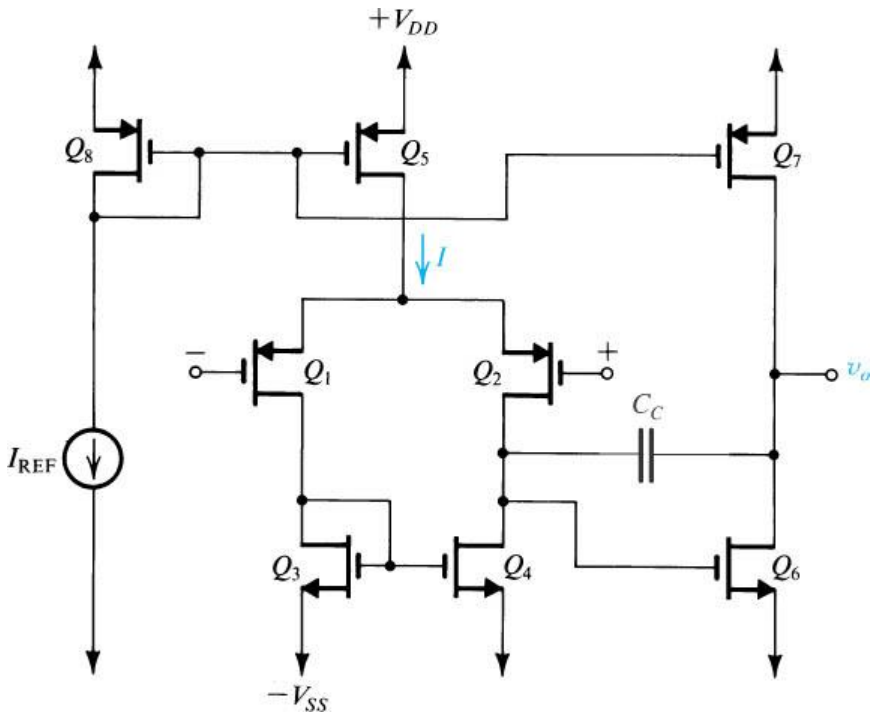
Frequency Compensation

CS Amp

Analysis of Two-Stage Transconductance Amplifier: Qualitative Understanding

Lect. 15: Two-Stage Amplifier

Input Common-Mode Range



For $V_{ICM,min}$, Q_1, Q_2 should be in saturation

$$V_{SD1} > V_{SG1} - |V_{tp}|$$

$$V_{S1} - V_{D1} > V_{S1} - V_{ICM} - |V_{tp}|$$

$$V_{ICM} > V_{D1} - |V_{tp}|$$

$$\mathbf{V_{ICM,min} = -V_{ss} + V_{GS3} - |V_{tp}|}$$

For $V_{ICM,max}$, Q_5 should be in saturation

$$V_{SD5} > V_{SG5} - |V_{tp}|$$

$$V_{S5} - V_{D5} > V_{S5} - V_{G5} - |V_{tp}|$$

$$V_{D5} < V_{G5} + |V_{tp}| = V_{DD} - V_{SG5} + |V_{tp}|$$

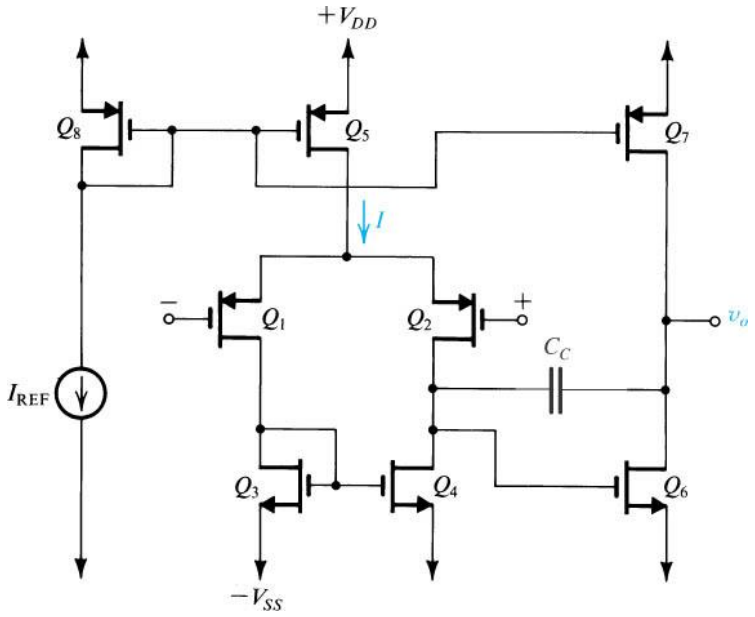
$$V_{ICM} + V_{SG1} < V_{DD} - V_{SG5} + |V_{tp}|$$

$$\mathbf{V_{ICM,max} = V_{DD} - V_{SG5} - V_{SG1} + |V_{tp}|}$$

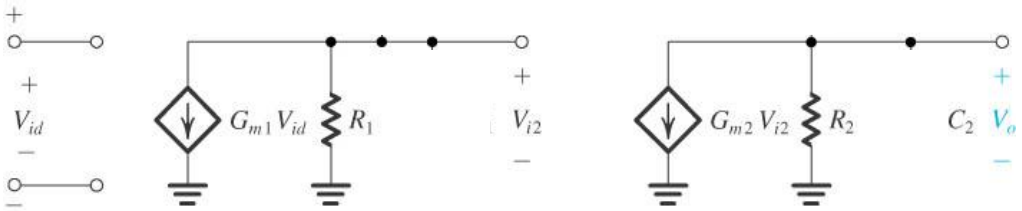
Large I ➔ Large V_{SG5}, V_{SG1}, V_{GS3}

➔ Small input CM range

Lect. 15: Two-Stage Amplifier



Small Signal Model



Voltage Gain (DC)

Two CS amps in cascade

G_{m1}=

R_1=

A_{v1} =

G_{m2}=

R_2 =

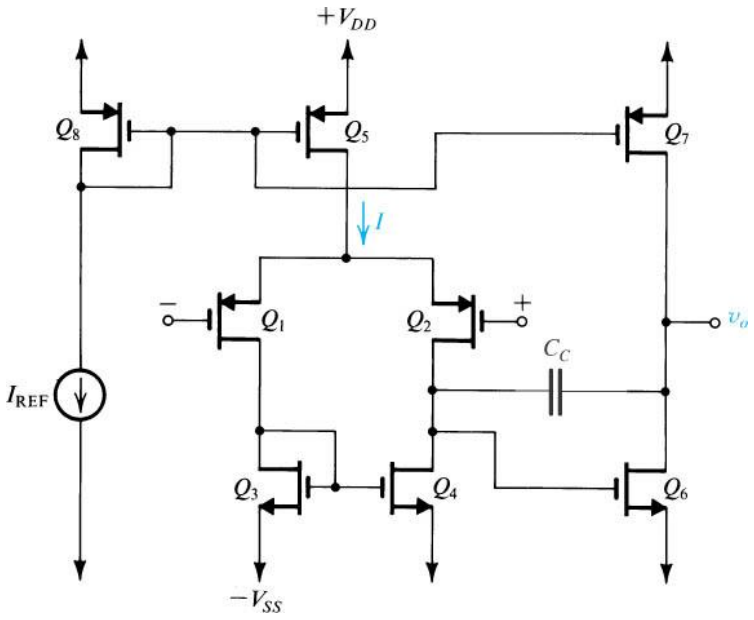
A_{v2} =

A_v=

R_{in}:

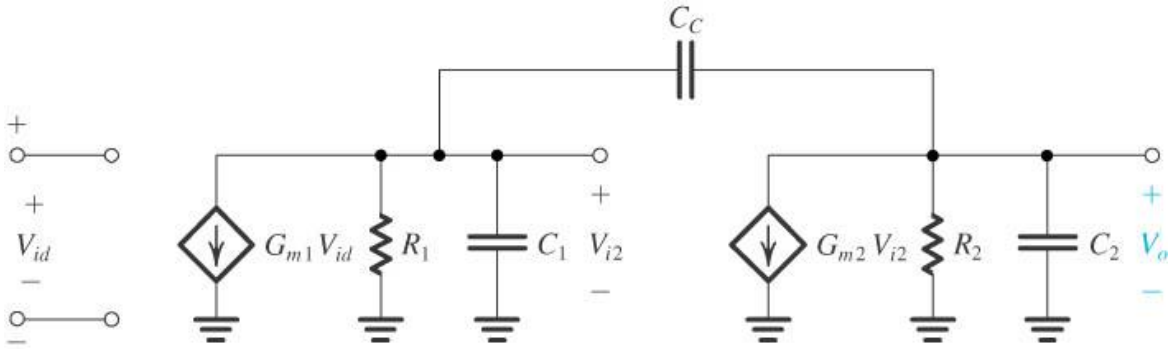
R_{out}:

Lect. 15: Two-Stage Amplifier

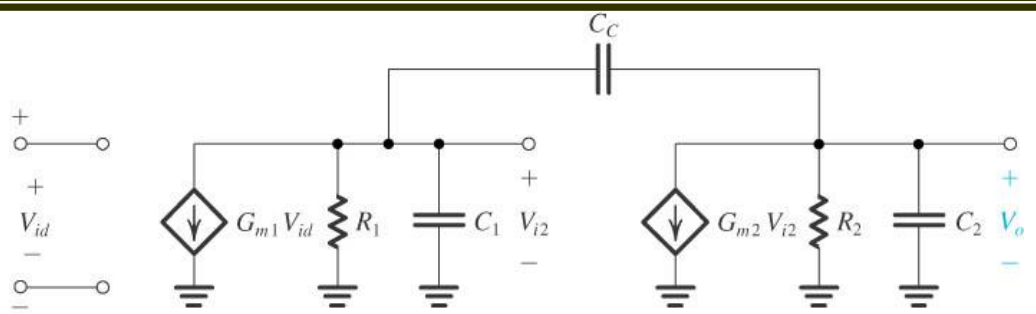


Frequency Response

For simplicity, assume all the capacitive elements are lumped together as C_1 and C_2.

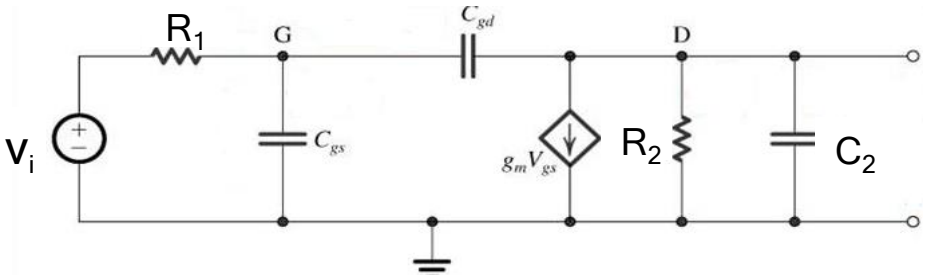


Lect. 15: Two-Stage Amplifier



$$\frac{V_o(s)}{V_{id}(s)} = ?$$

In Lect. 14,



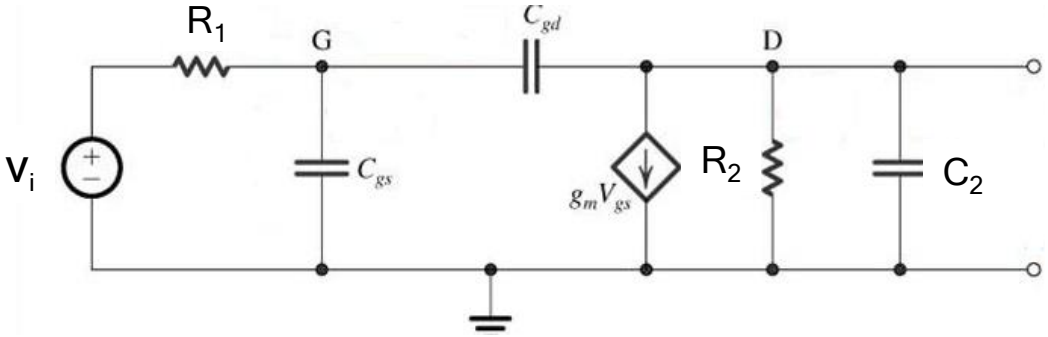
$$\frac{V_o}{V_i} = \frac{\left(g_m - sC_{gd}\right)R_2}{1 + s\left[C_{gs}R_1 + C_2R_2 + C_{gd}\left(g_mR_1R_2 + R_1 + R_2\right)\right] + s^2\left[C_{gs}C_2 + C_{gd}\left(C_{gs} + C_2\right)\right]R_1R_2}$$

Since $V_i = -G_{m1}V_{id}R_1$, $\dfrac{V_o(s)}{V_{id}(s)} = -G_{m1}R_1\dfrac{V_o(s)}{V_i(s)}$ Same pole zero characteristics!

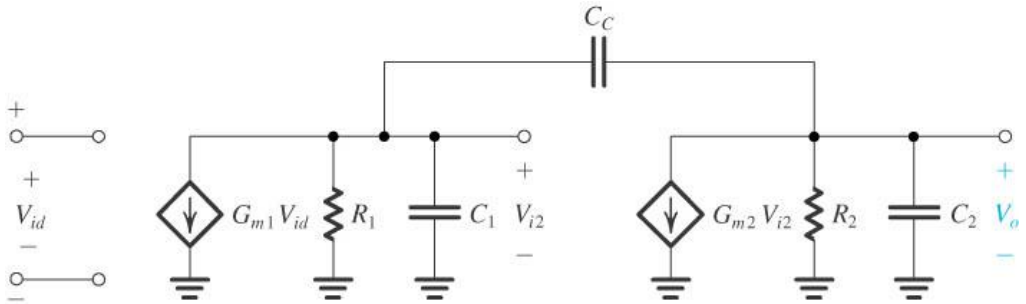
With corresponding parameter changes

Lect. 15: Two-Stage Amplifier

In Lect. 14,



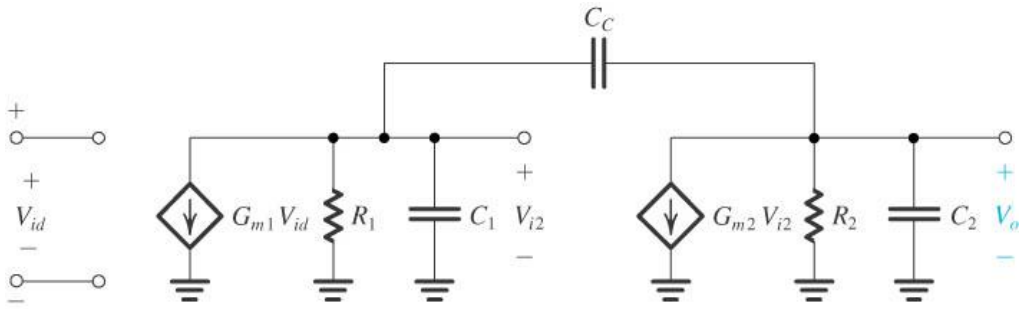
$$\omega_{P1} \sim \frac{1}{C_{gd} g_m R_2 R_1} \qquad \omega_{P2} \sim \frac{g_m C_{gd}}{C_{gs} C_2 + C_{gd}\left(C_{gs} + C_2\right)}$$



$$\omega_{P1} \sim \frac{1}{C_C G_{m2} R_2 R_1} \qquad \omega_{P2} \sim \frac{G_{m2} C_C}{C_1 C_2 + C_C\left(C_1 + C_2\right)}$$

Can be used for initial design of the amp for the desired bandwidth and phase margin

Lect. 15: Two-Stage Amplifier

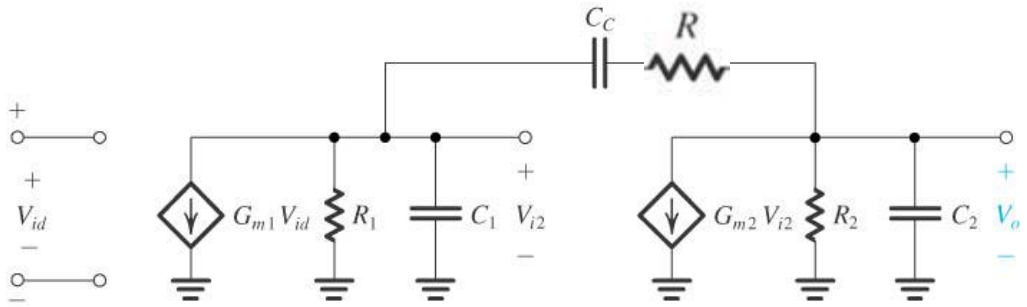


Where is zero?

- Zero in the right half-plane decreases the phase margin

- Move the zero to the left half-plane!

Lect. 15: Two-Stage Amplifier



- Move the zero to the left half-plane!

With $V_o = 0$ $\quad V_{i2} = G_{m2}V_{i2}\left(R + \frac{1}{sC_c}\right)$

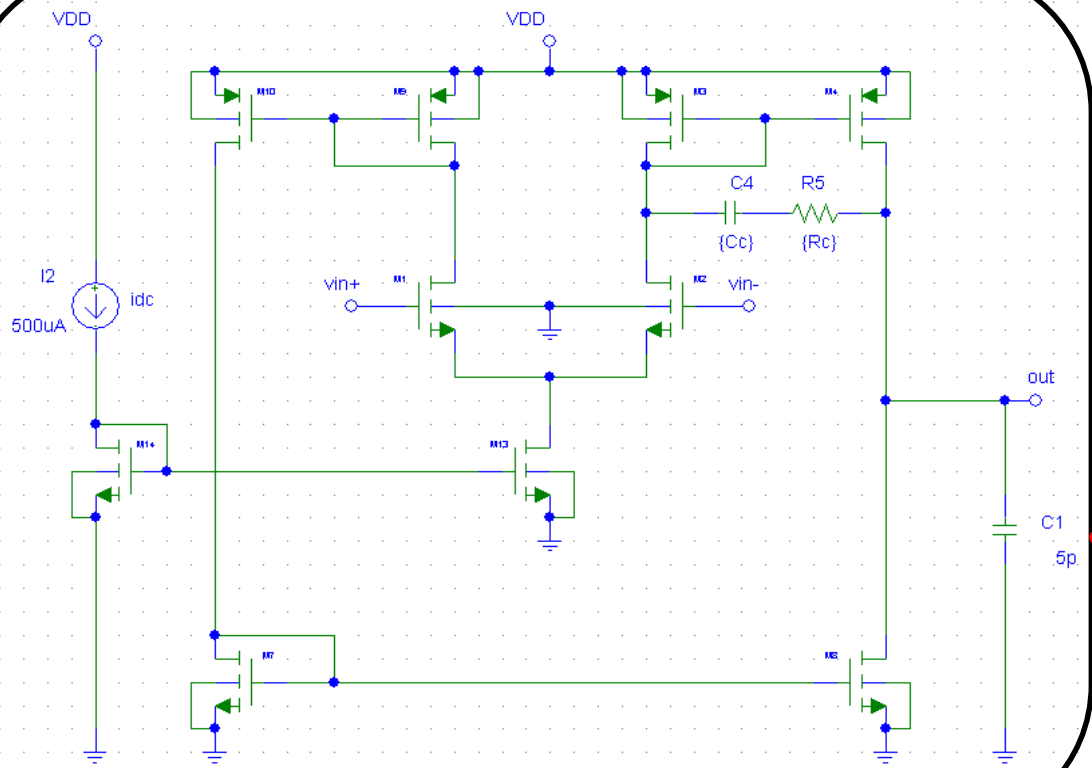
Zero at $\quad s = \frac{1}{C_c\left(1/G_{m2} - R\right)}$

When $R > 1/G_{m2}$, the zero moves to the left-half plane!

➔ Good for phase margin!

Lect. 15: Two-Stage Amplifier

Mirrored OTA for Design Project #1

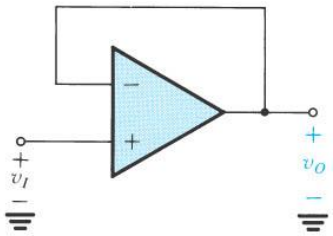


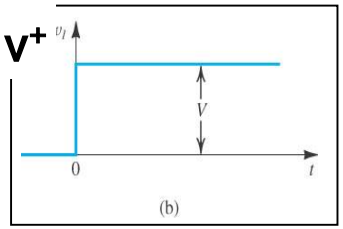
- Mirrored OTA Specifications

Parameter	Value
A_V	>56dB
Bandwidth	>60KHz
Phase Margin	>65°
V_{p-p}	>1.5V
Slew Rate	>13MV/s
CMRR	>85dB
Power Consumption	<2.5mW

Lect. 15: Two-Stage Amplifier

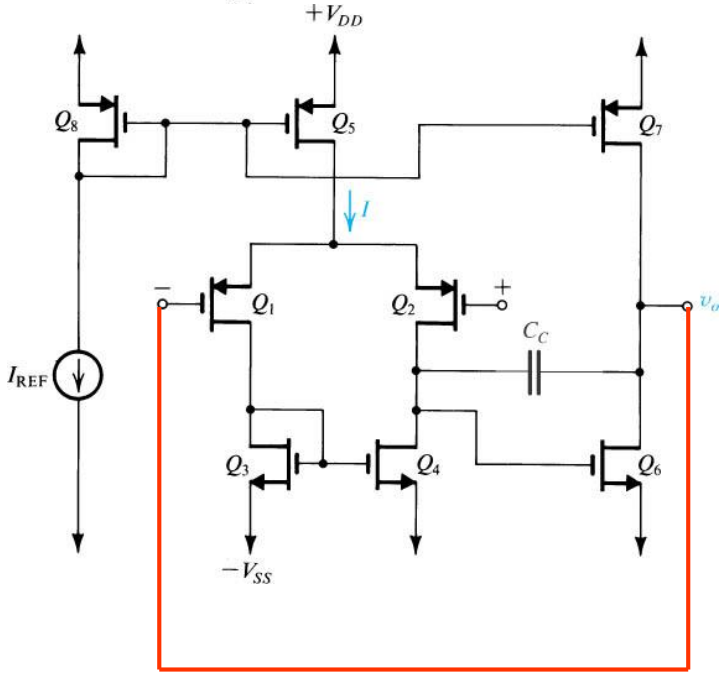
Slew Rate





Apply step input at v^+ ➔ $v_o(t)$=?

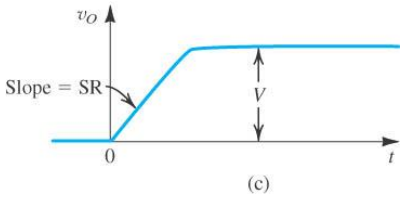
Slew Rate: $\left.\frac{dv_o(t)}{dt}\right|_{max}$



With step input

Q_2 off ➔ I through Q_1, Q_3 ➔ I through C_C

$$v_o(t) = \frac{I}{C_C}t$$



$$\left.\frac{dv_o}{dt}\right|_{max} = \frac{I}{C_C}$$