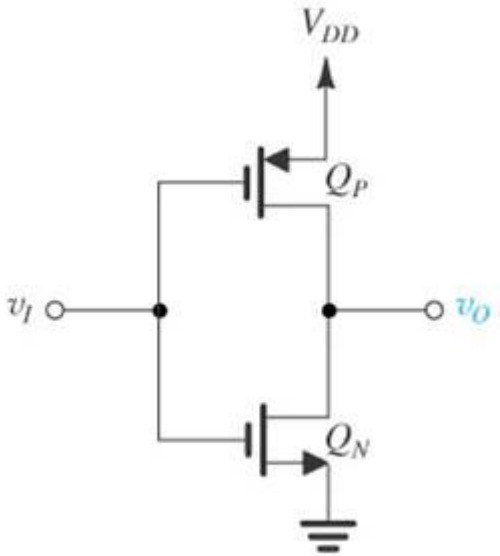
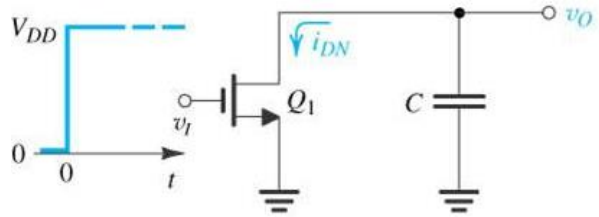
Lect. 24: CMOS Logic Gates (Razavi 15.3)

CMOS inverter

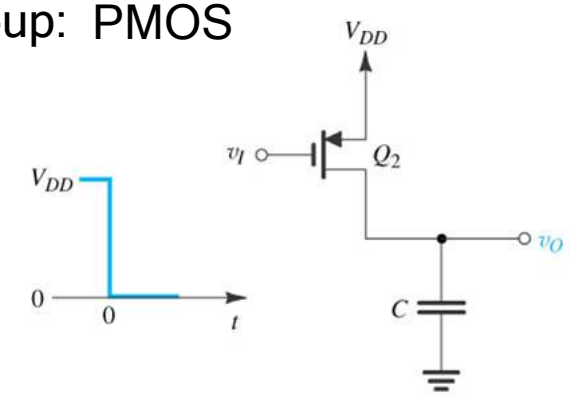
Different transistor acting for pull-down and pull-up operation



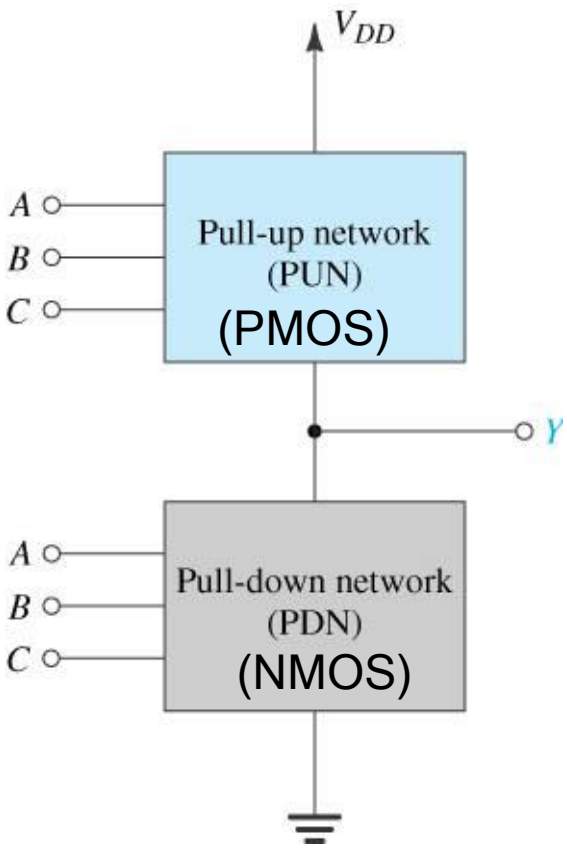
- Pull-down: NMOS



- Pull-up: PMOS



CMOS Logic Gates

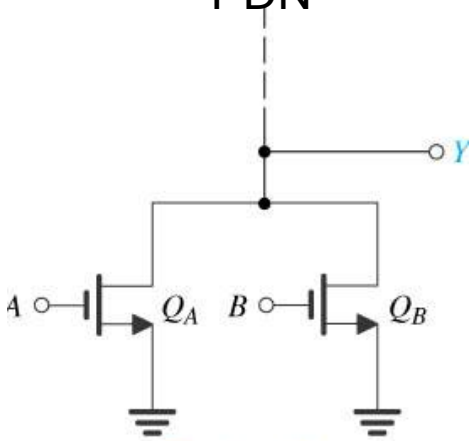


Y: L➔H

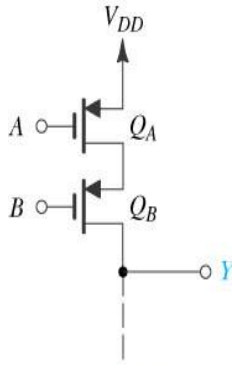
Y: H➔L

Lect. 24: CMOS Logic Gates

PDN



PUN



Y Pull-down,

Initially, Q_A OFF and Q_B OFF

(A LOW and B LOW)

Q_A ON or Q_B ON

(A HIGH or B HIGH)

Y Pull-up,

Initially, Q_A OFF or Q_B OFF

(A HIGH or B HIGH)

Q_A ON and Q_B ON

(A LOW and B LOW)

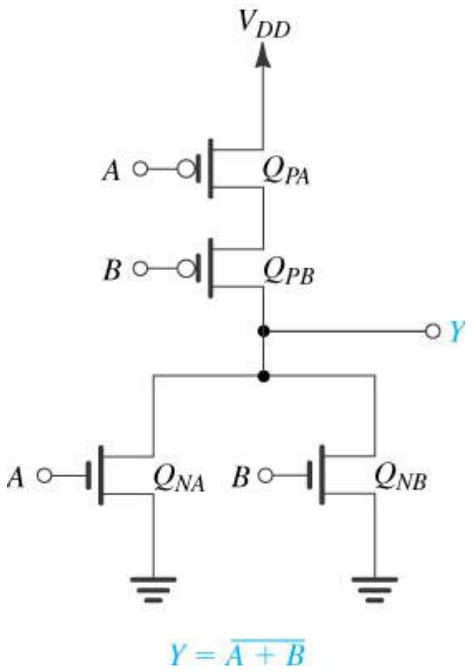
$$\bar{Y} = A + B$$

NOR Gate

$$Y = \bar{A}\bar{B}$$

Lect. 24: CMOS Logic Gates

CMOS NOR Gate

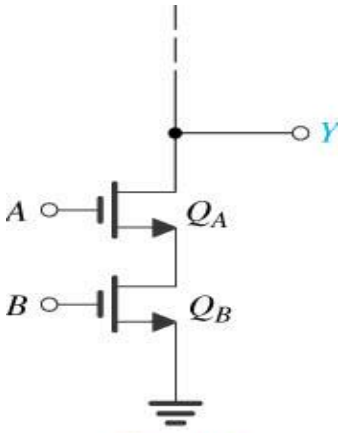


Structures of PUN and PDN have the duality property

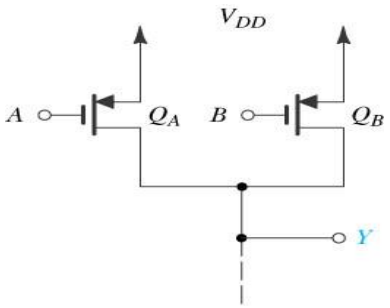
Three input CMOS NOR Gate?

Lect. 24: CMOS Logic Gates

PDN



PUN



Y Pull-down,

Initially, Q_A OFF or Q_B OFF

(A LOW or B LOW)

Q_A ON and Q_B ON

(A HIGH and B HIGH)

$\bar{Y} = AB$ ➔ NAND Gate

Y Pull-up,

Initially, Q_A OFF and Q_B OFF

(A HIGH and B HIGH)

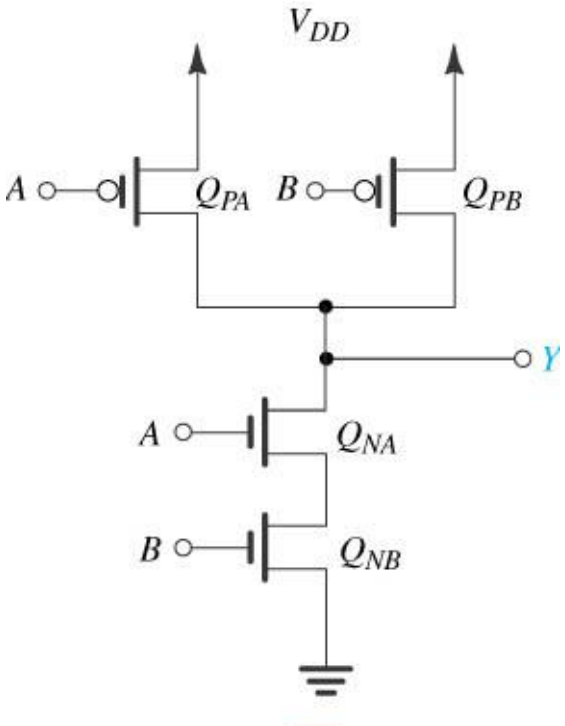
Q_A ON or Q_B ON

(A LOW or B LOW)

$Y = \bar{A} + \bar{B}$

Lect. 24: CMOS Logic Gates

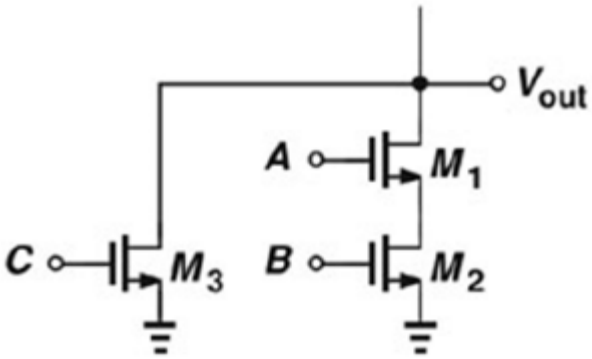
CMOS NAND Gate

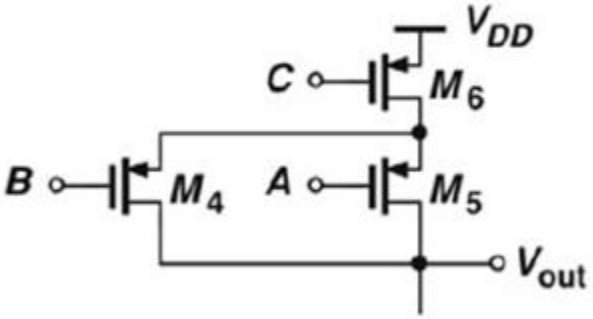


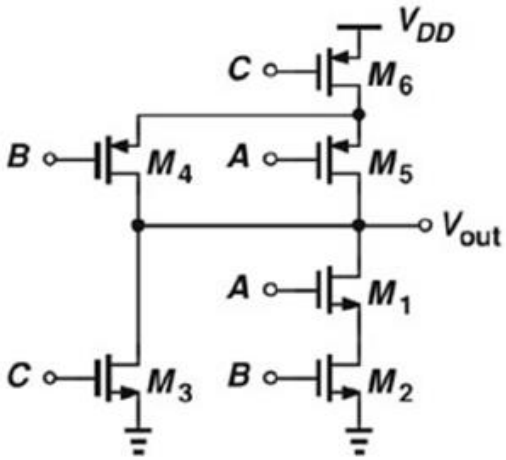
Three input CMOS NAND Gate?

Lect. 24: CMOS Logic Gates

Corresponding PUN?







Logic function?

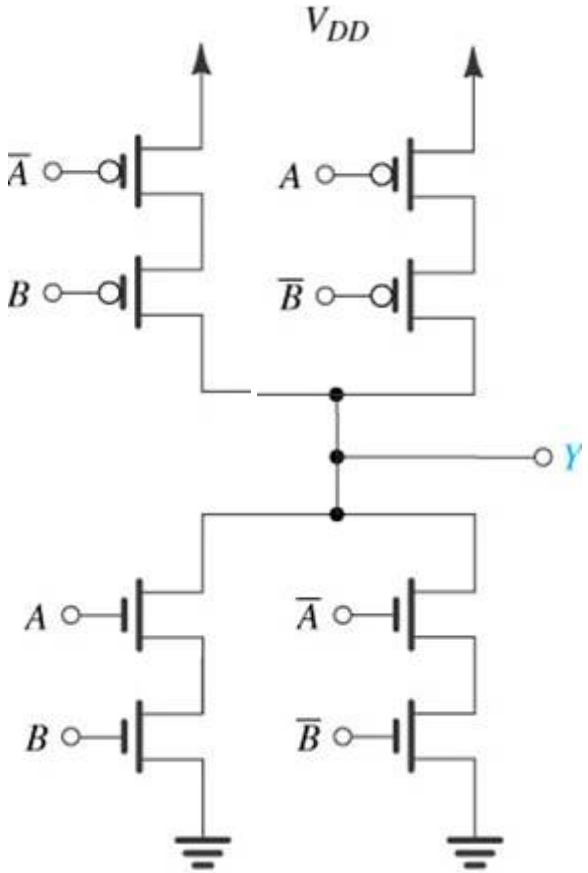
Lect. 24: CMOS Logic Gates

CMOS XOR (Exclusive OR)

A: 0 1 0 1
B: 0 0 1 1
XOR: 0 1 1 0

PDN: $\bar{Y} = AB + \bar{A}\bar{B}$

PUN: $Y = A\bar{B} + \bar{A}B$



Complicated digital logic gates can be realized by CMOS logic gates!