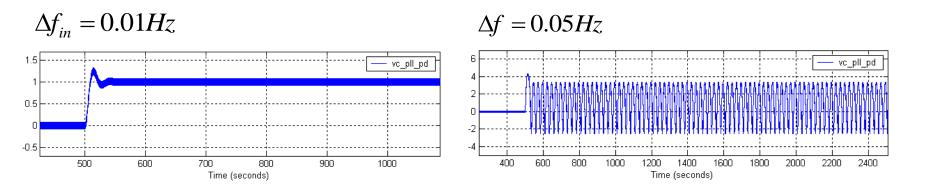


This type of PLL has very narrow locking range

Step response simulation:

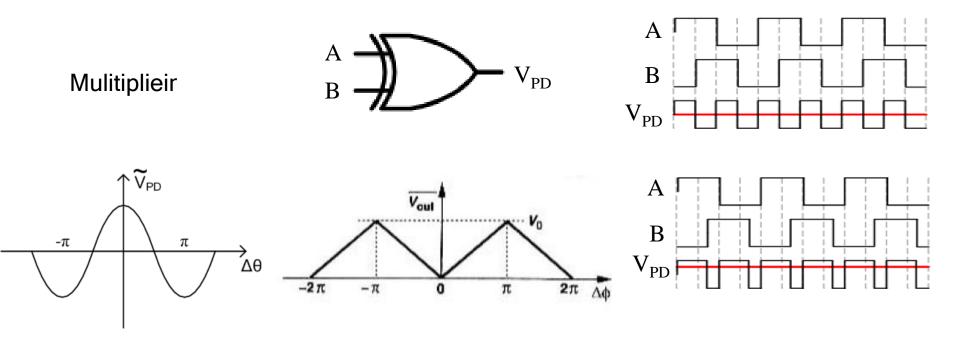
 $f_{in} = 1Hz, K_{PD} = 5V / rad, K_{VCO} = 2\pi \times 0.01 rad / s / V, and f_p = 0.032Hz$





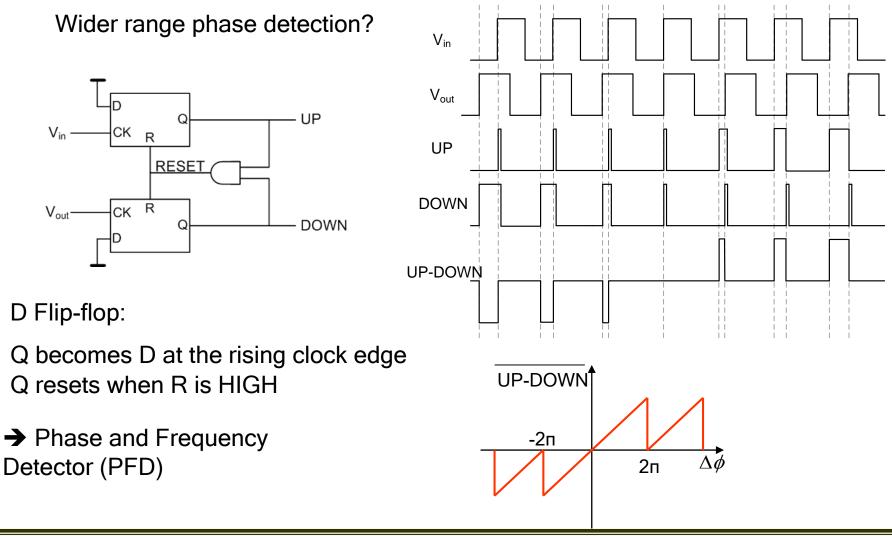
W.-Y. Choi

Limitation is due to narrow linear phase detection range



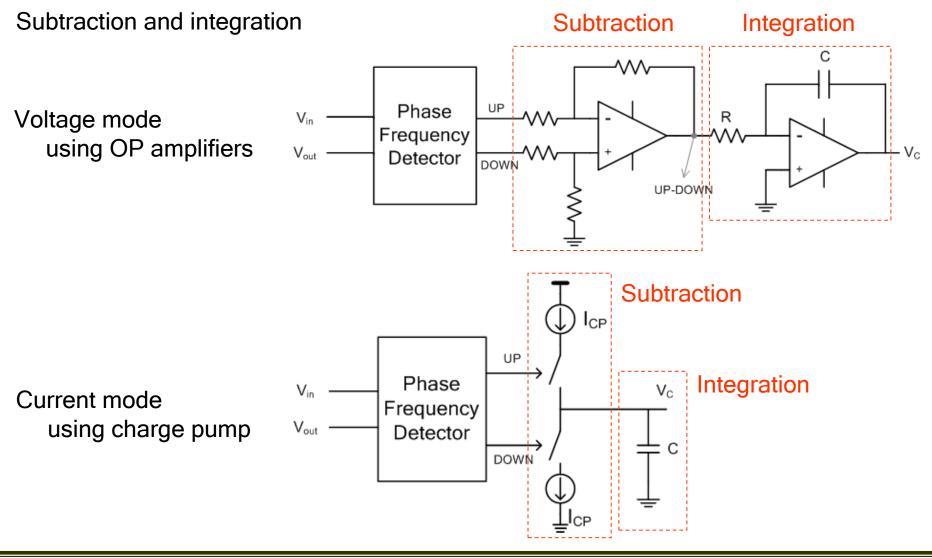
Electronic Circuits 2 (15/1)





Electronic Circuits 2 (15/1)

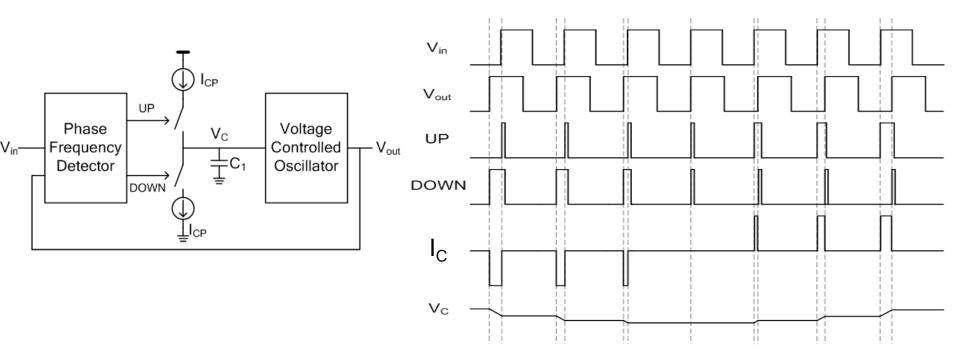




Electronic Circuits 2 (15/1)

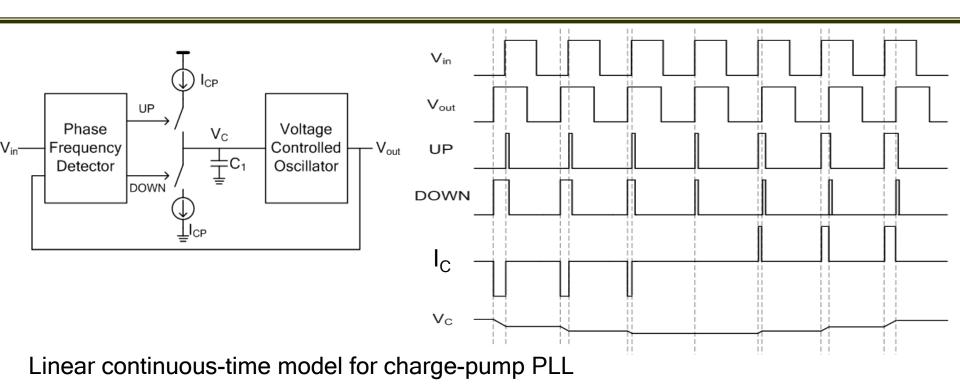


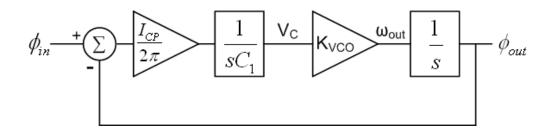




Electronic Circuits 2 (15/1)

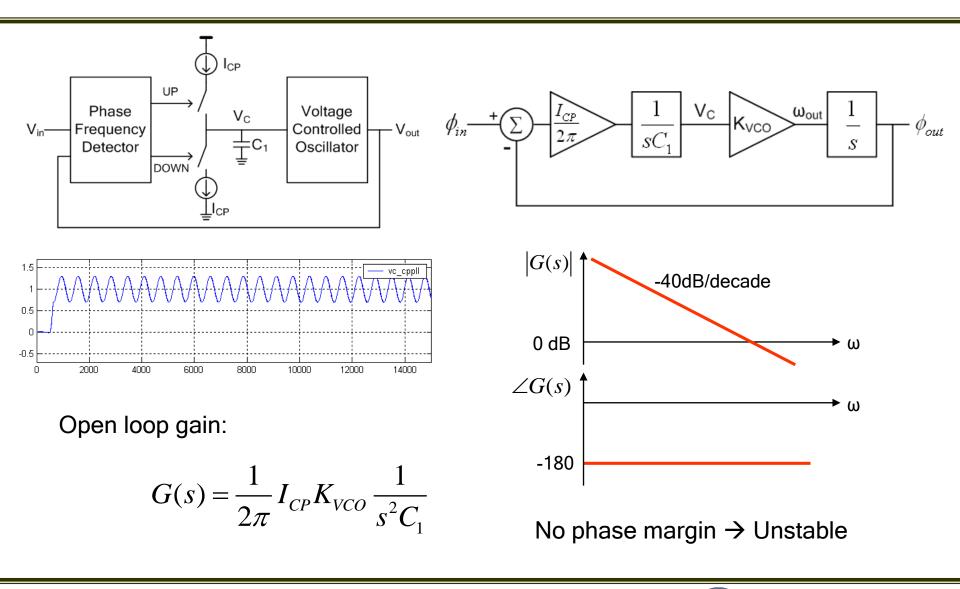




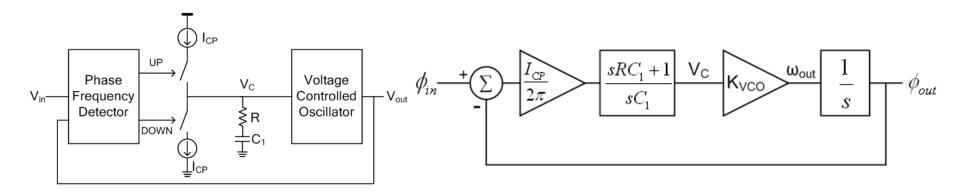


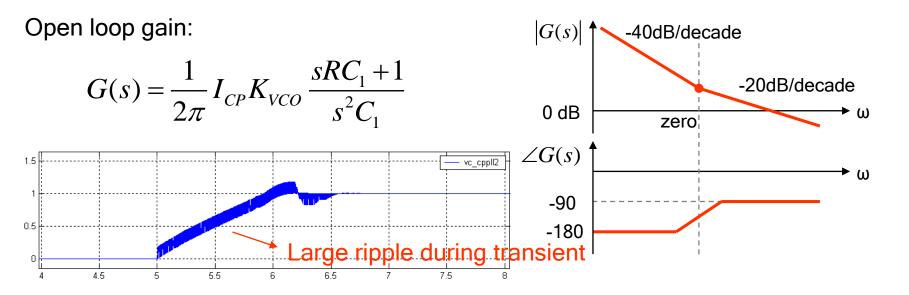




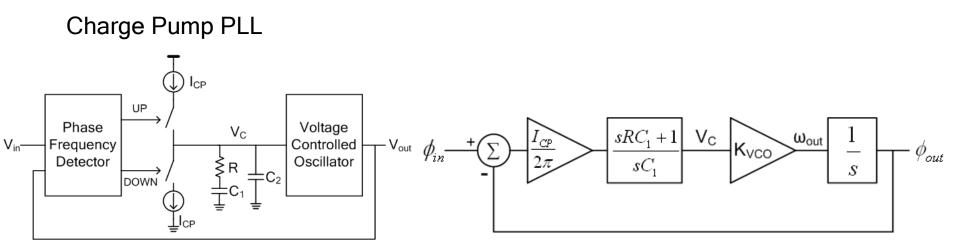


W.-Y. Choi

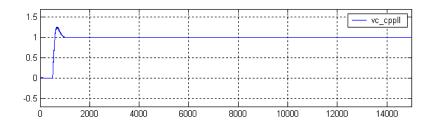




W.-Y. Choi



→ Ripple reduction with small C_2 (≈ $C_1/10$)



Open loop gain:

Simplification as 2nd-order system

$$G(s) \sim \frac{1}{2\pi} I_{CP} K_{VCO} \frac{sRC_1 + 1}{s^2 C_1}$$



W.-Y. Choi

$$G(s) = \frac{1}{2\pi} I_{CP} K_{VCO} \frac{sRC_1 + 1}{s^2 C_1}$$

Closed loop transfer function

$$H(s) = \frac{\frac{I_{CP}}{2\pi C_1} K_{VCO} (RC_1 s + 1)}{s^2 + \frac{I_{CP}}{2\pi} K_{VCO} Rs + \frac{I_{CP}}{2\pi C_1} K_{VCO}}$$

$$\omega_0 = \sqrt{\frac{I_{CP}K_{VCO}}{2\pi C_1}} \qquad Q = \frac{1}{R\sqrt{I_{CP}C_1K_{VCO}}}$$

Electronic Circuits 2 (15/1)



