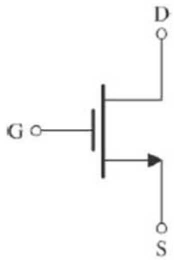
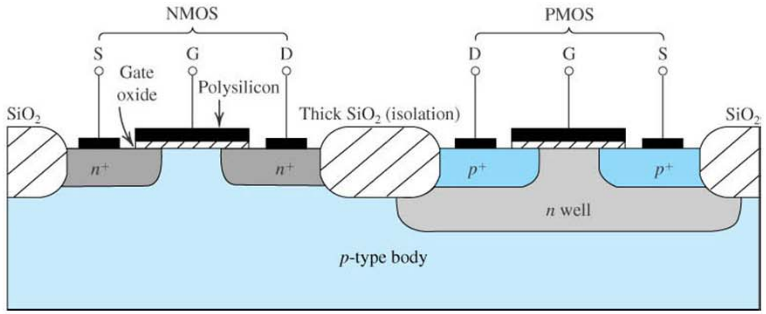
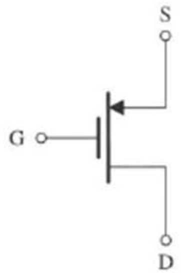
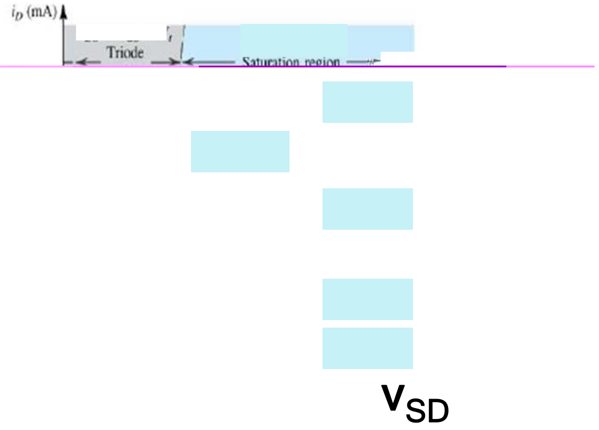
Lect. 3: MOS Transistors (2)









Cut-off : $i_D = 0$

Triode : $i_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left[2(v_{GS} - V_{TH})\cdot v_{DS} - v_{DS}{}^2\right]$

Saturation : $i_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(v_{GS} - V_{TH})^2$

Cut-off: $i_D \quad 0$

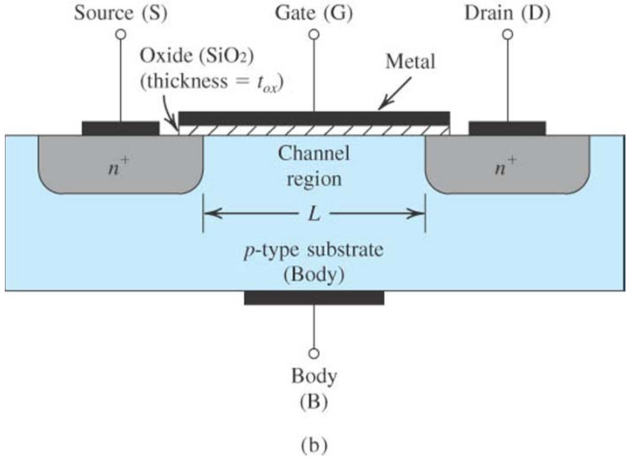
Triode: $i_D \quad \frac{1}{2} \quad {}_pC_{ox}\frac{W}{L} \quad 2(v_{SG} \quad |V_{TH}|) \; v_{SD} \quad v_{SD}{}^2$

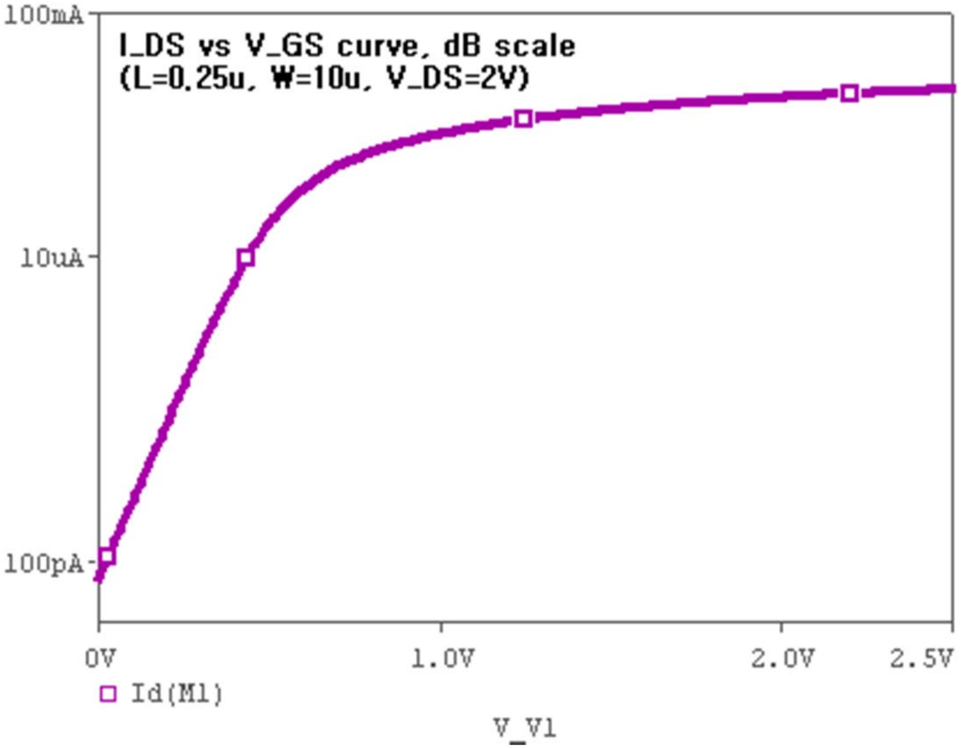
Saturation: $i_D \quad \frac{1}{2} \quad {}_pC_{ox}\frac{W}{L}(v_{SG} \quad |V_{TH}|)^2$

Lect. 3: MOS Transistors (2)

Deviation from the ideal model

1) I_D really zero in Cut-Off ?





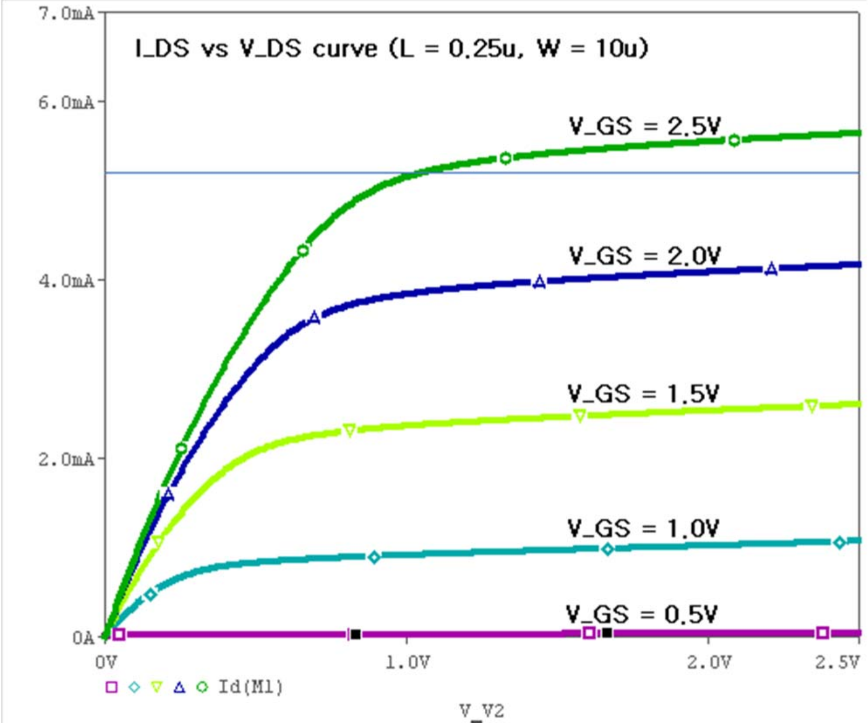
Leakage between S and D: more significant for smaller MOSFET

➔ Significant problem in modern digital circuits

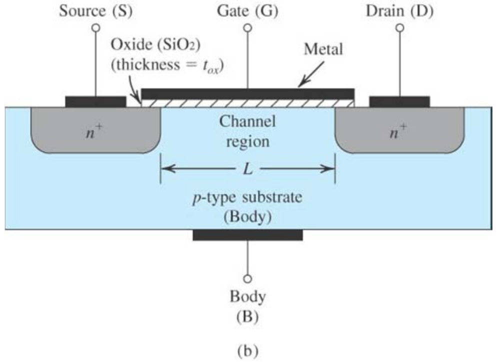
Lect. 3: MOS Transistors (2)

2) In saturation, $i_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(v_{GS} - V_{TH})^2$

➔ Should have no dependence on v_{DS}



But I_D increases with v_{DS} even in saturation



v_{DS} increase causes reduction in actual channel length

➔ Channel length modulation

$$i_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(v_{GS} - V_{TH})^2(1 + \lambda \cdot v_{DS})$$

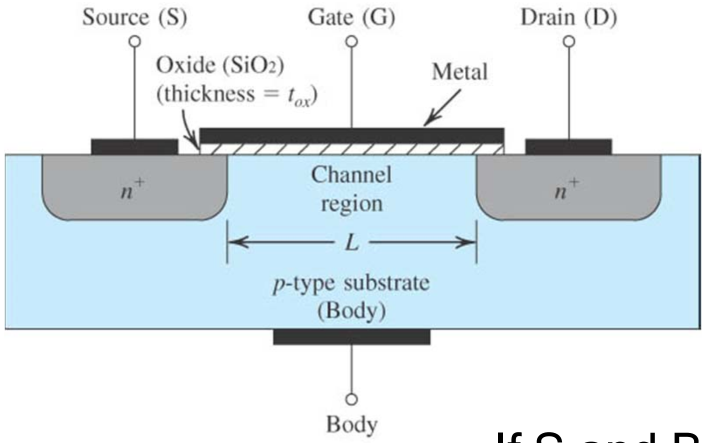
(Early effect in BJT)

Ideal current source

➔ Current source with parallel R

Lect. 3: MOS Transistors (2)

3) Body effect: Voltage applied to B causes change in threshold voltage

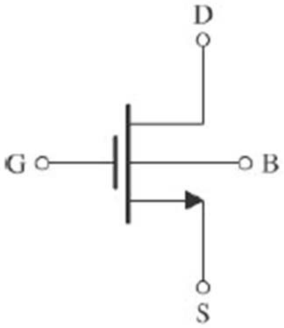


$$i_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(v_{GS} - V_{TH})^2$$

$$\mathbf{V}_{TH} = \mathbf{V}_{THO} + \gamma[\sqrt{2\phi_f + \mathbf{V}_{SB}} - \sqrt{2\phi_f}\,]$$

$$\mathbf{V}_{TH} = \mathbf{V}_{THO} \ \textbf{when} \ \mathbf{V}_{SB} = 0$$

ϕ_f and γ : process-dependent parameters



If S and B can be tied, no body effect.

But in IC, B is shared among many transistors

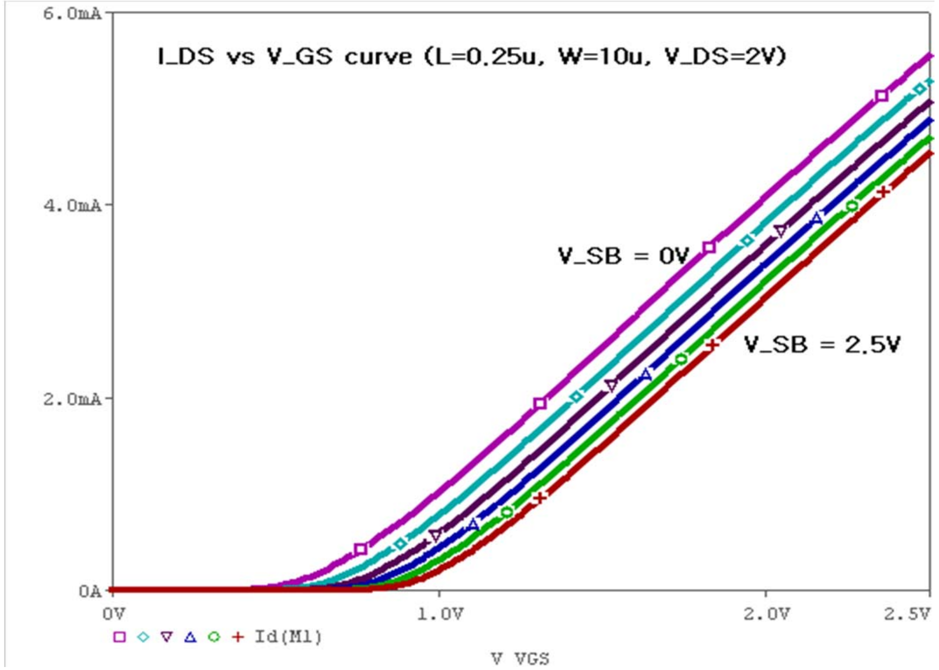
B is connected to
- the most negative supply voltage (NMOS)
- the most positive supply voltage (PMOS)

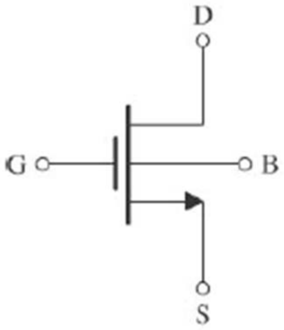
➔ V_{TH} depends on V_S

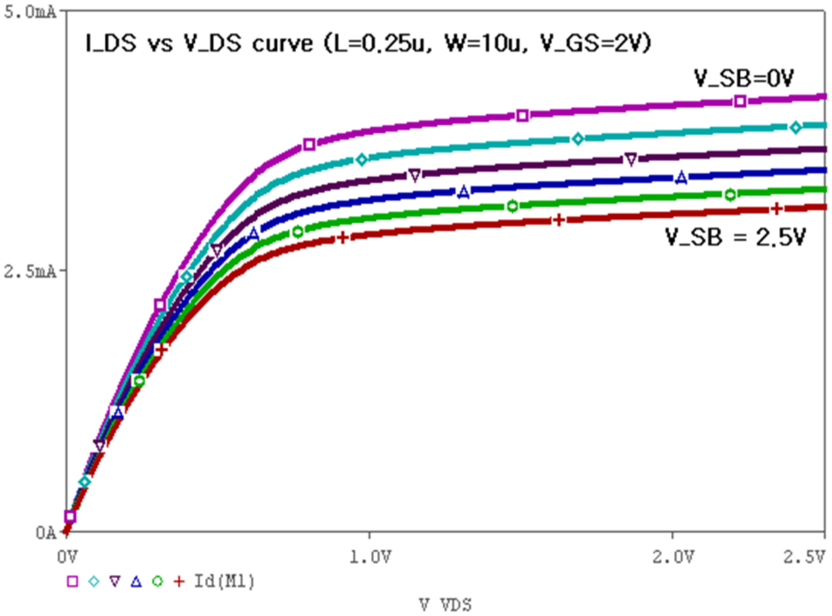
Difficult to model analytically ➔ Simulation

Lect. 3: MOS Transistors (2)

Body effect: Voltage applied to B causes a change in threshold voltage.

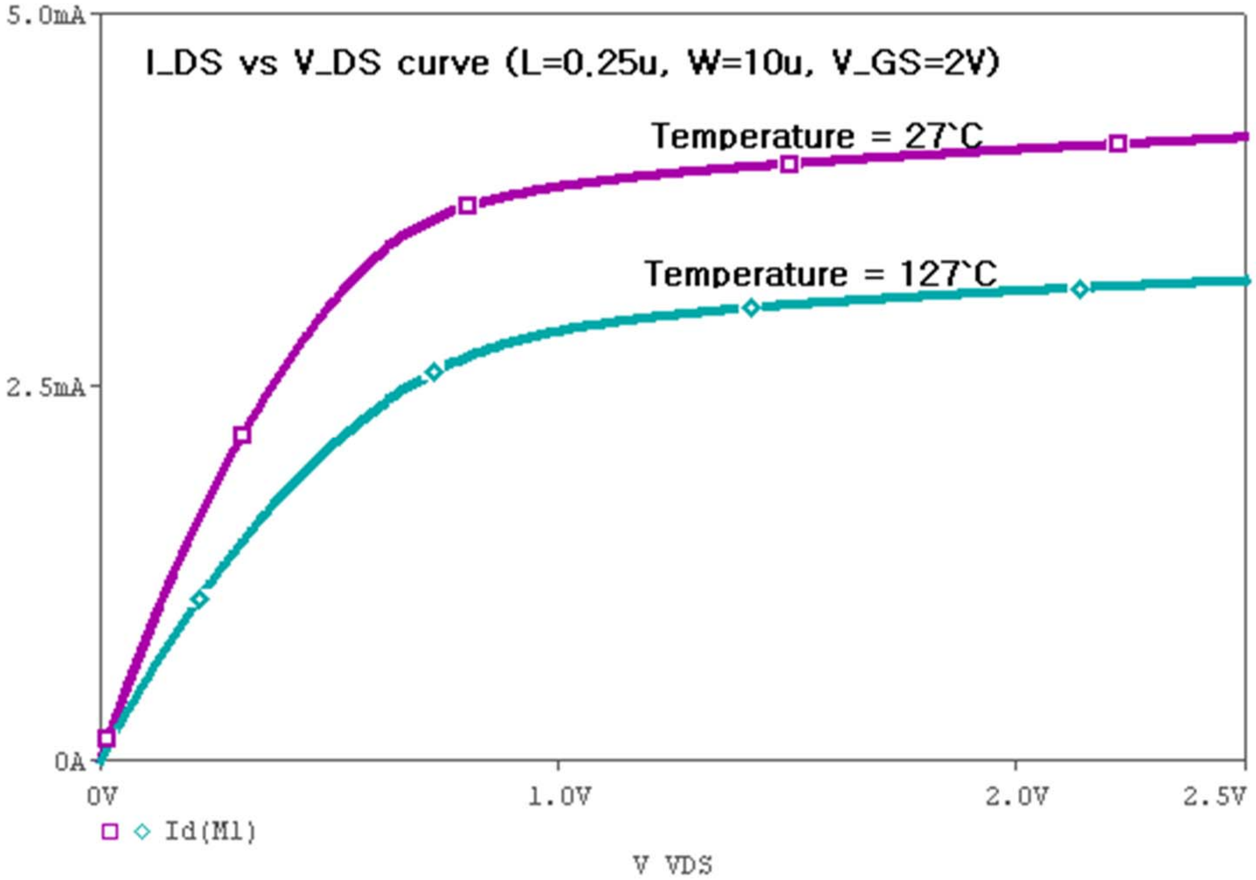






Lect. 3: MOS Transistors (2)

4) Temperature effect: Many MOSFET parameters are temperature dependent



Higher temperature causes reduction in I_D

Lect. 3: MOS Transistors (2)

- Modern transistors are very complicated in their structure.

- Many parameters are needed to model their characteristics accurately in SPICE

- SPICE parameters for 0.25μm NMOS are shown on the right

- Although complicated, they can precisely model the transistor characteristics

➔Two-track approach:

- Simple, easy-to-use models for analysis
- Complicated, accurate models for simulation

```
MODEL orbit2L2N NMOS (                              LEVEL   = 7
+TNOM    = 27             TOX     = 5.6E-9
+XJ      = 1E-7           NCH     = 2.3549E17      VTH0    = 0.3654765
+K1      = 0.4732214      K2      = 7.994532E-4    K3      = 1E-3
+K3B     = 3.0713494      W0      = 1E-7           NLX     = 1.617898E-7
+DVT0W   = 0              DVT1W   = 0              DVT2W   = 0
+DVT0    = 0.455178       DVT1    = 0.6258687      DVT2    = -0.5
+U0      = 280.4589023    UA      = -1.607126E-9   UB      = 2.806549E-18
+UC      = 3.290051E-11   VSAT    = 1.07496E5      A0      = 1.8770435
+AGS     = 0.3310181      B0      = -3.173524E-8   B1      = -1E-7
+KETA    = -8.69841E-3    A1      = 8.317145E-5    A2      = 0.6592347
+RDSW    = 200            PRWG    = 0.4477477      PRWB    = 0.0208175
+WR      = 1              WINT    = 0              LINT    = 1.392558E-10
+DWG     = -2.28419E-8
+DWB     = -6.95781E-10   VOFF    = -0.0910963     NFACTOR = 1.202941
+CIT     = 0              CDSC    = 2.4E-4         CDSCD   = 0
+CDSCB   = 0              ETA0    = 5.0732E-3      ETAB    = 6.262008E-5
+DSUB    = 0.0310034      PCLM    = 1.5101091      PDIBLC1 = 0.897659
+PDIBLC2 = 2.924029E-3    PDIBLCB = 0.0651312      DROUT   = 1
+PSCBE1  = 7.017738E8     PSCBE2  = 2.271109E-4    PVAG    = 8.531511E-3
+DELTA   = 0.01           RSH     = 4.6            MOBMOD  = 1
+PRT     = 0              UTE     = -1.5           KT1     = -0.11
+KT1L    = 0              KT2     = 0.022          UA1     = 4.31E-9
+UB1     = -7.61E-18      UC1     = -5.6E-11       AT      = 3.3E4
+WL      = 0              WLN     = 1              WW      = 0
+WWN     = 1              WWL     = 0              LL      = 0
+LLN     = 1              LW      = 0              LWN     = 1
+LWL     = 0              CAPMOD  = 2              XPART   = 0.5
+CGDO    = 4.59E-10       CGSO    = 4.59E-10       CGBO    = 5E-10
+CJ      = 1.78338E-3     PB      = 0.99           MJ      = 0.4661295
+CJSW    = 4.154041E-10   PBSW    = 0.9563049      MJSW    = 0.3162462
+CF      = 0              PVTH0   = -9.648921E-3   PRDSW   = -10
+PK2     = 3.534961E-3    WKETA   = 0.0120981      LKETA   = -3.31688E-3    )
```

Lect. 3: MOS Transistors (2)

Homework
(Due on 3/9 before TA session for those who are familiar with PSPICE.
For those who are not, due on 3/11 before lecture.)

- Simulate I-V characteristics of NMOS and PMOS transistors using PSPICE model provided in the course web. Use $L=0.25\mu m$ and $W=10\mu m$.