Common-Source Stage 2

- Lecture 39

1. Input/Output Impedances of Degenerated Common Source Stage
2. Biasing Technique
3. Self-biased Common Source Stage

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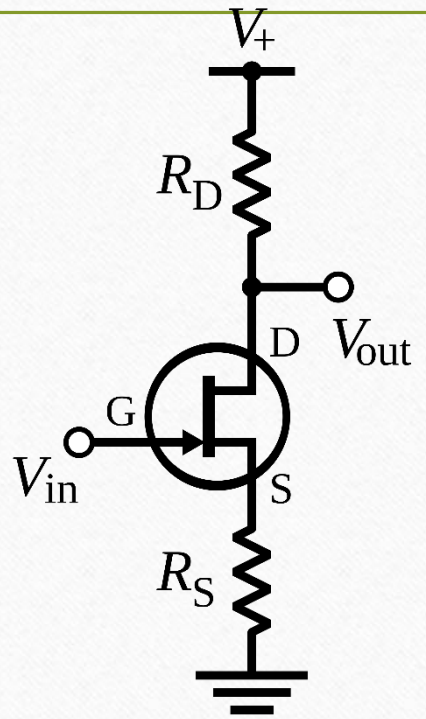
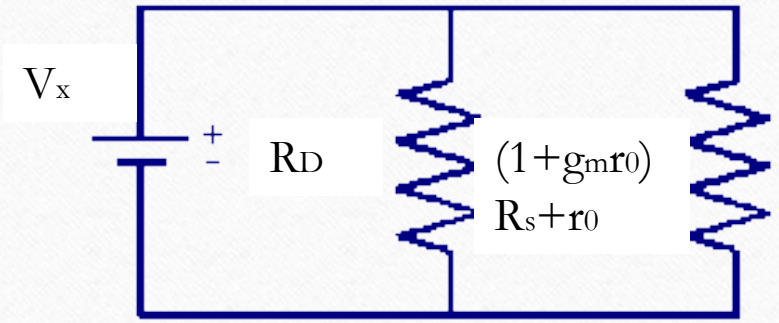
Input/Output Impedances of Degenerated CS Stage



R_{in} = infitiny

At low frequencies

(input current =0)



$R_{out} = R_D // (1+g_m r_0)R_s + r_0$

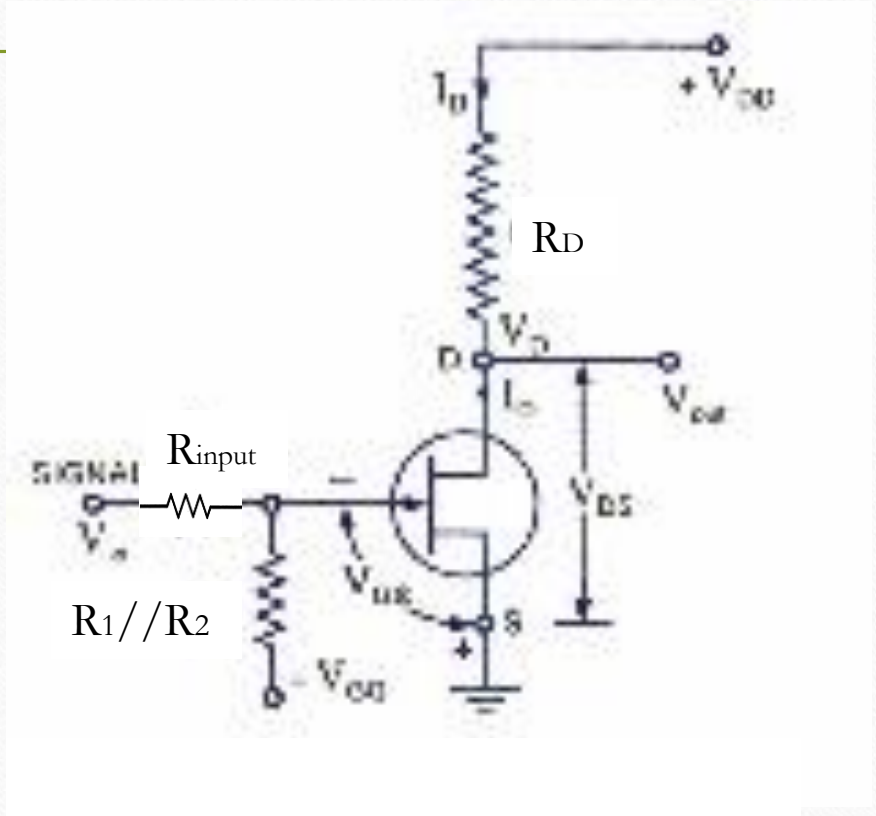
Biasing Technique($\lambda = 0$)

1. Gain when there is a input …

$$\text{Gain} = \frac{Vx}{Vin}\frac{Vout}{Vx}$$

$$= \frac{R1//R2}{(R1//R2) + Rinput}(-g_m R_D)$$

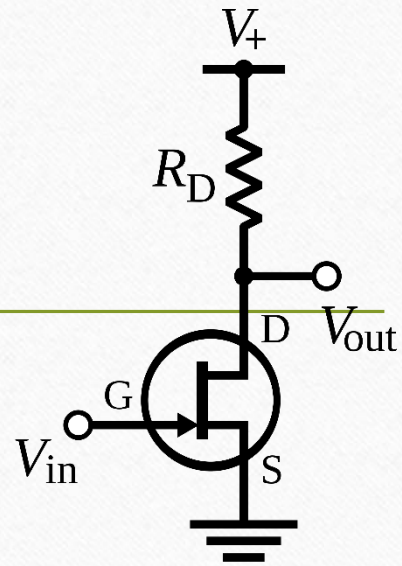
Choose $R_1//R_2 >> Rinput$



2. To stay SATURATION

$V_{DD} - I_D R_D > V_{in} - V_{Th}$

$$\frac{V_{DD} - V_{in} + V_{Th}}{I_D} > R_D$$



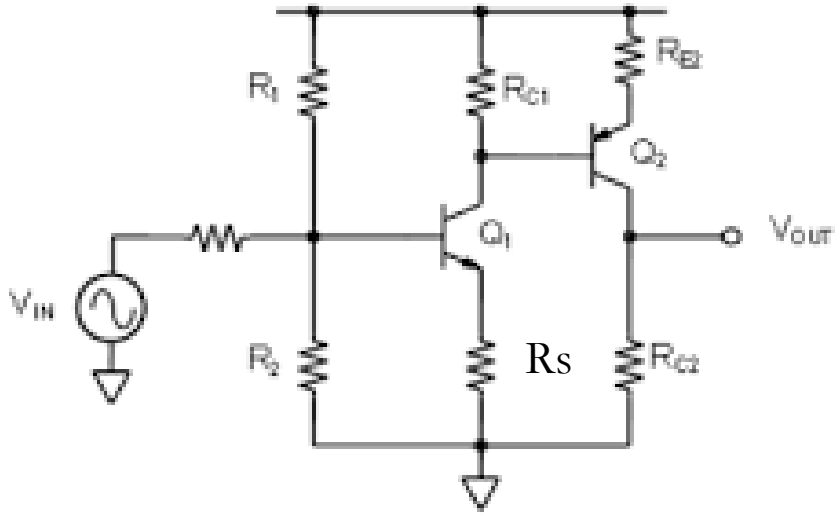
3. Apply capacitor between two CS stage

To isolate DC current level from each other

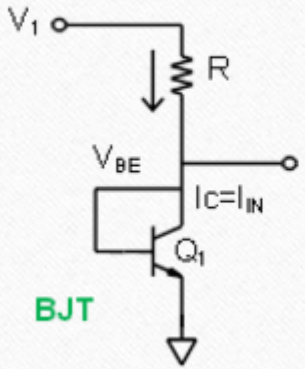
4. I_D is sensitive to V_{DD}, Temperature , $\mu C_{ox}(W/L)$

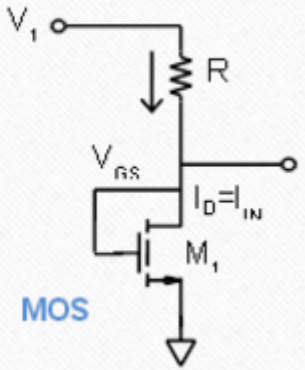
5. Reduce sensitivity with degenerated CS stage

$$V_{DD}\frac{R2}{R1+R2} = V_{GS} + I_D R_S$$



Self-biased CS stage





V_{Th} increases → I_D increases

Drain voltage = Gate voltage = $V_{DD} - I_D R_D$

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{DD} - I_D R_D - V_{Th}\right)^2$$