Lesson32: Common Gate Stage 1

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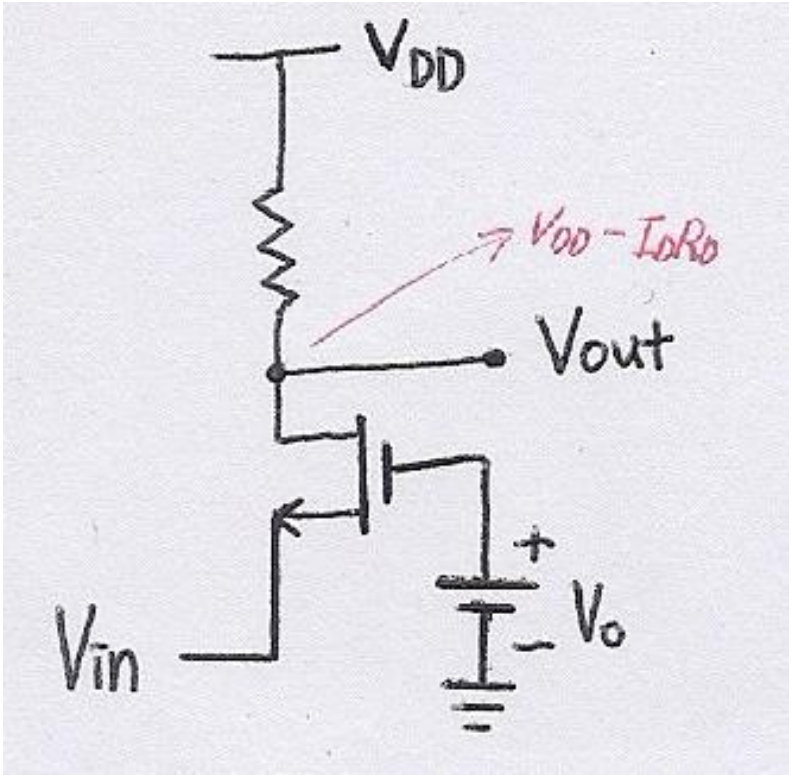
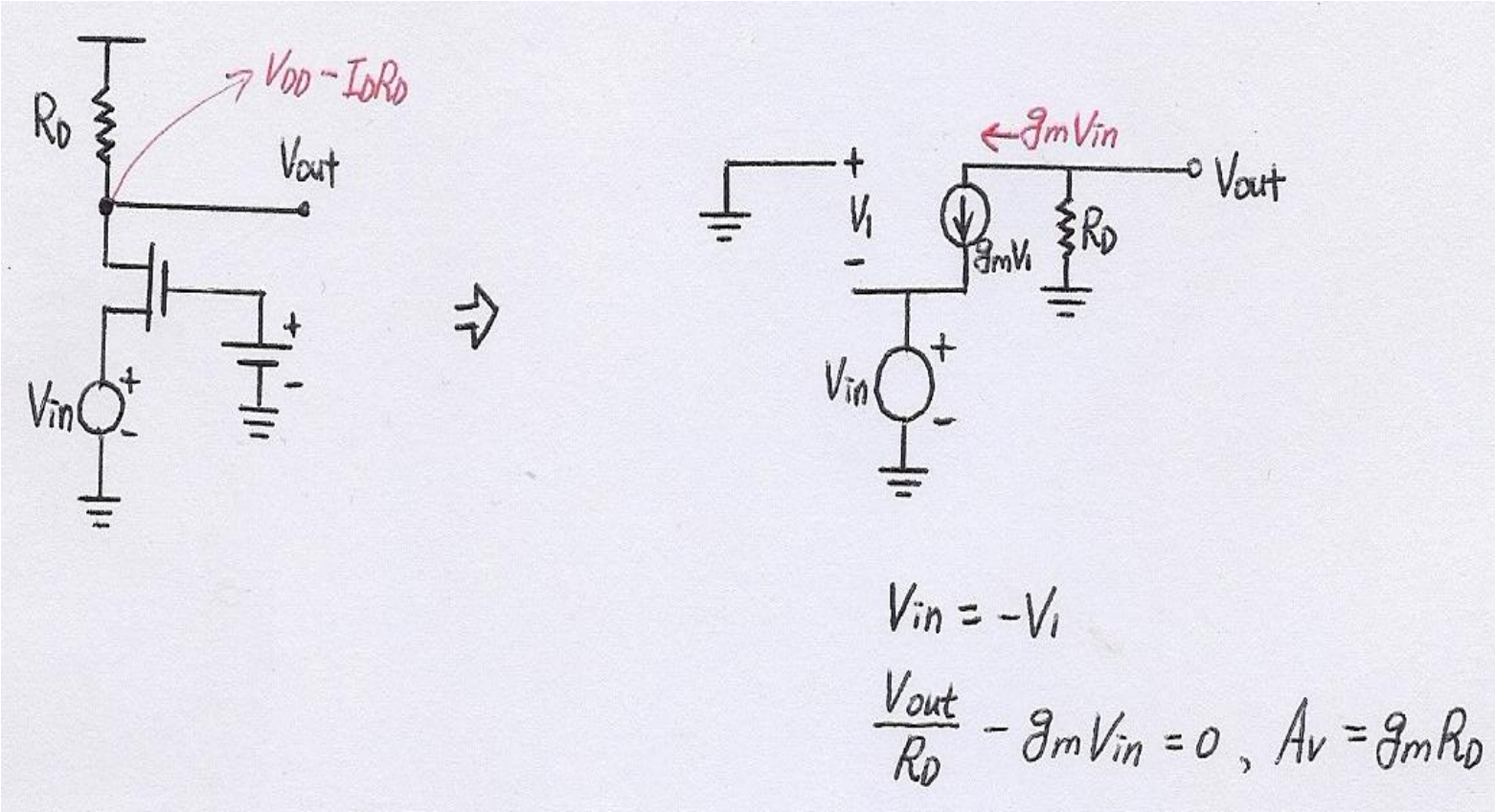
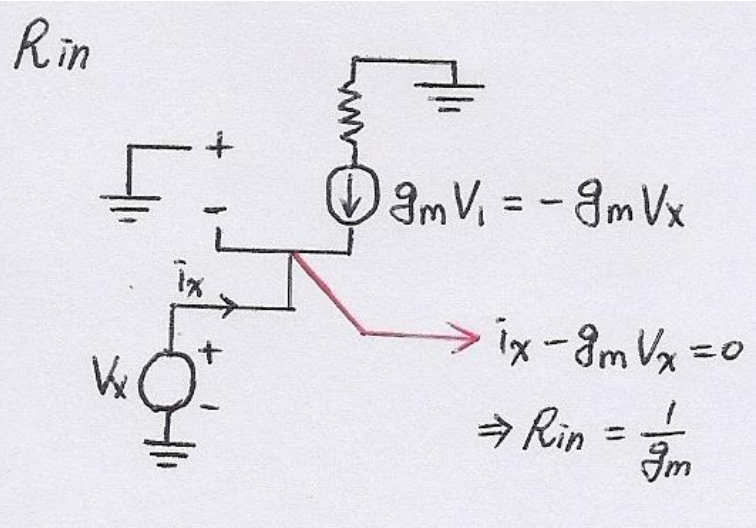
Common-gate topology

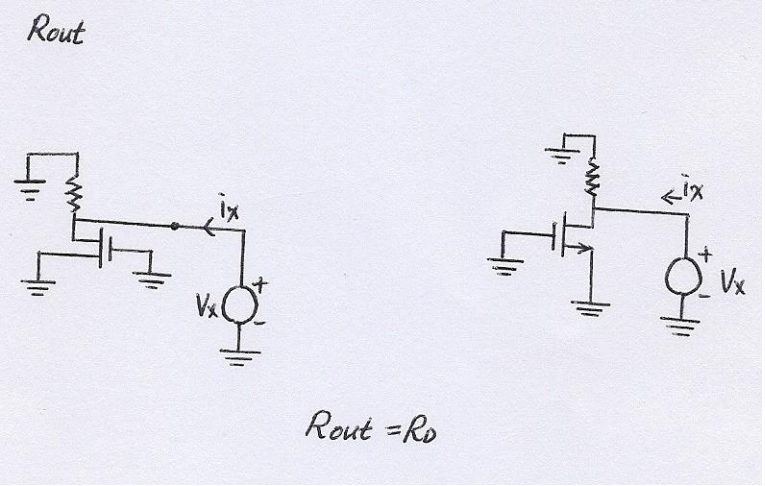


- **Small signal properties**

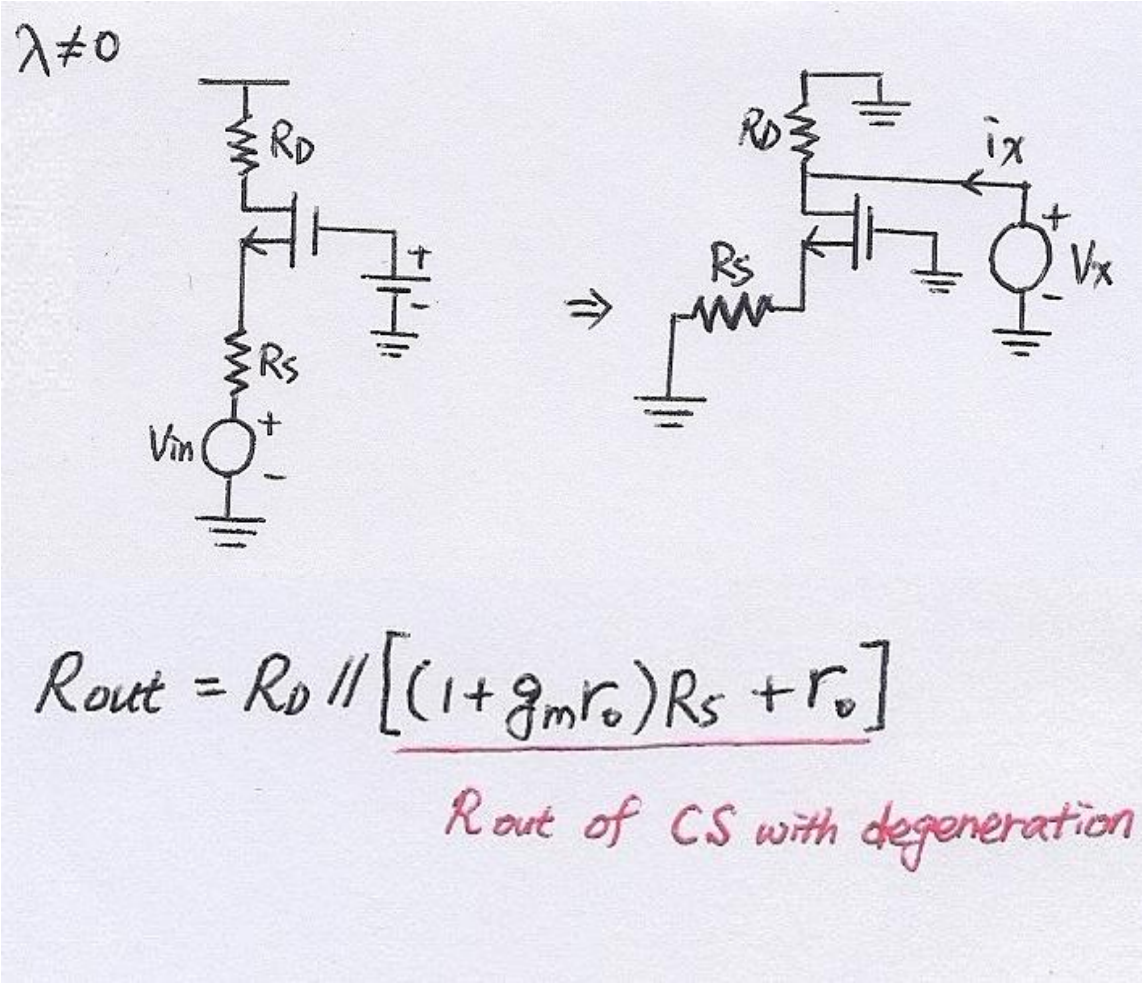


- Input and output impedances

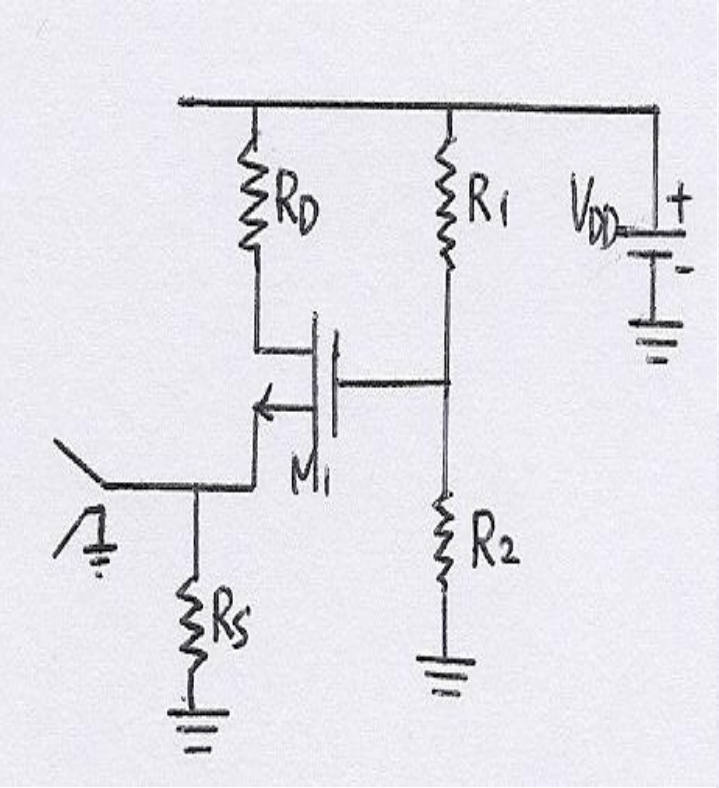


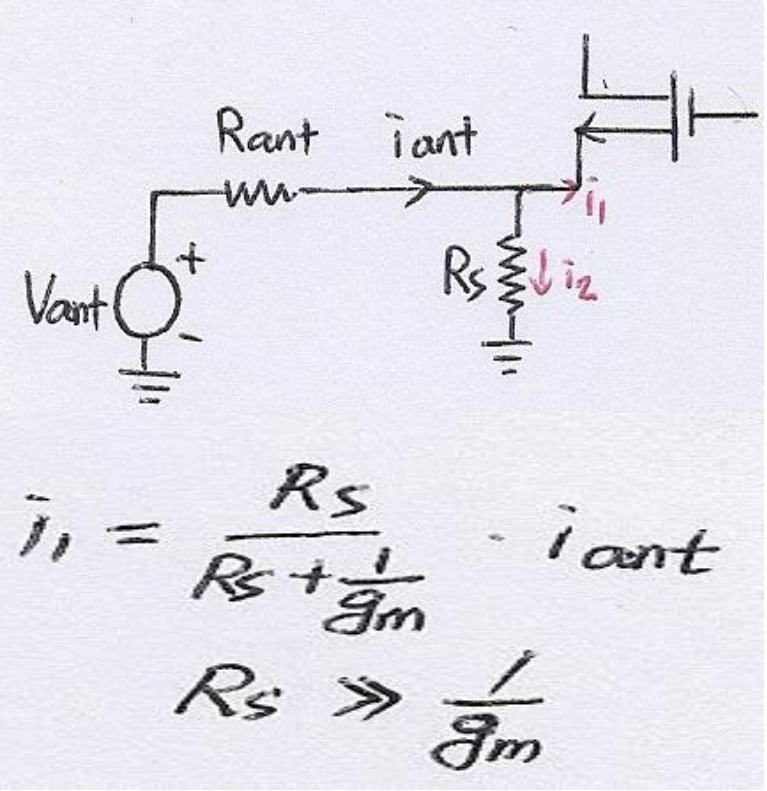


- Output resistance of CG stage in a special case



- Bias design

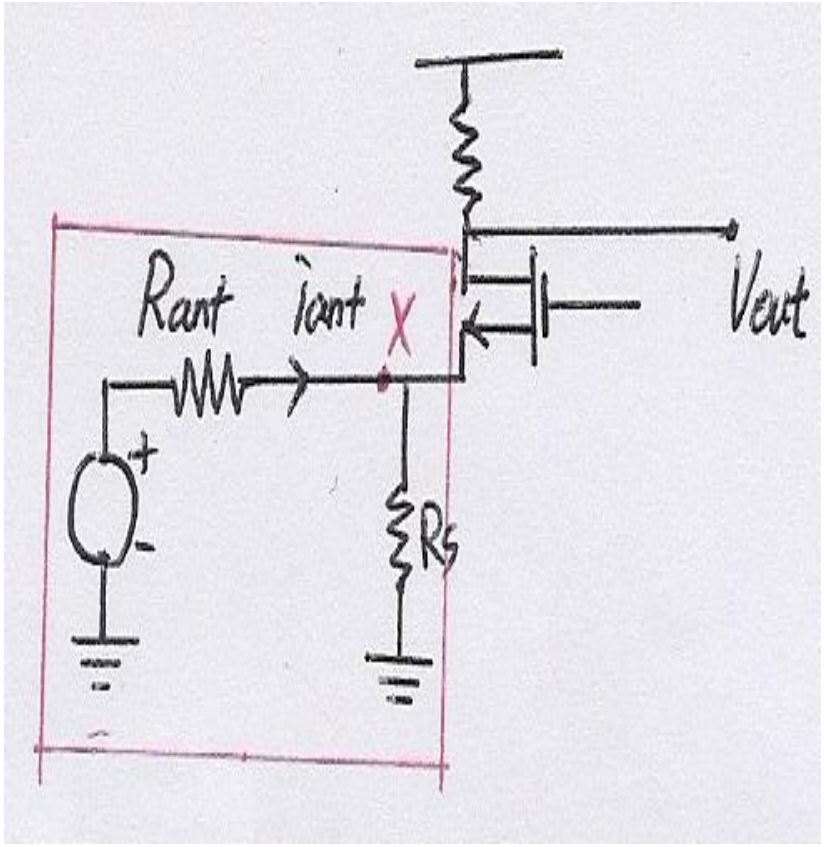


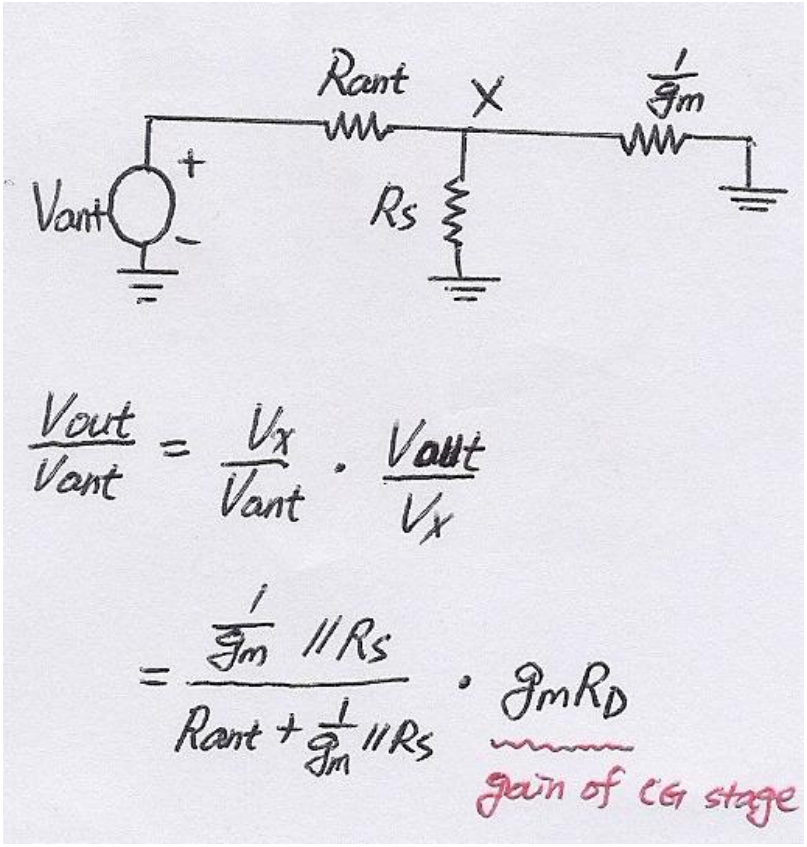


$$i_1 = \frac{R_S}{R_S + \frac{1}{g_m}} \cdot i_{ant}$$

$$R_S \gg \frac{1}{g_m}$$

- Bias design


Rant
iant
X
Vout
Rs


Rant
X
1/gm
Vant
Rs
Vout/Vant = Vx/Vant · Vout/Vx
= 1/gm // Rs / (Rant + 1/gm // Rs) · gmRD
gain of CG stage