Quiz for Lesson 28 and 29

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Electronic Circuits 1
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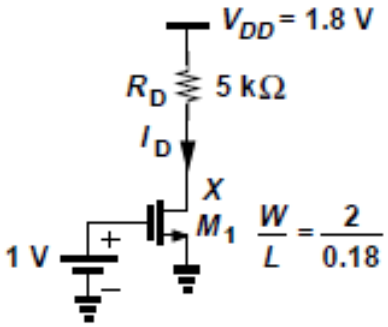
Name: _____ Student ID: _____

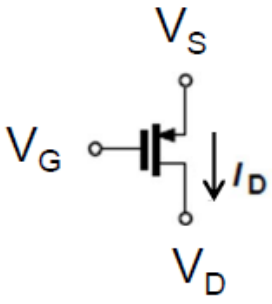
Prob. 1

Determine the small signal model of the following circuit when a small-signal voltage input (v_{in}) is added between 1V source and the gate terminal. Use $\mu_n C_{ox}$ = 100μA/V^2, V_{TH} = 0.4V, and λ = 0.1 V^{-1}. Provide numerical values for your small-signal circuit parameters. Include the channel-length modulation effect only for the small-signal analysis, not for the large-signal analysis.



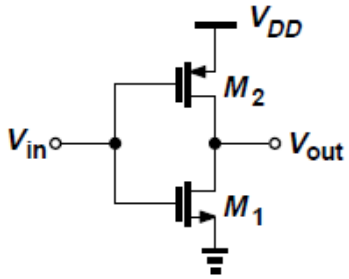
Prob. 2

Plot I_D vs V_{SD} for the PMOS shown below with $\mu_p C_{ox}$ = 30μA/V^2, (W/L)=20/0.18, V_{SG}= 1V, V_{TH} = -0.4V, λ = 0 V. Give numerical values for the voltage where the transistor becomes saturated and the saturated drain current.



Prob. 3

Draw the structure of the following CMOS circuit realized on a P-type Si substrate. In your drawing, clearly indicate where V_{in}, V_{out}, V_{DD}, and the ground terminals are.



Prob. 4

In the above CMOS circuit, both DC input (V_{in}) and DC output (V_{OUT}) is half of V_{DD} and both transistors are in saturation with the same drain currents. Determine the condition required for $(W/L)_1$ and $(W/L)_2$. Assume $|V_{TH,1}| = |V_{TH,2}|$ and $\lambda_1 = \lambda_2$, and $\mu_n = 3\mu_p$.

Prob. 5

Draw the small-signal model for the circuit shown in Prob. 4 with the conditions given in Prob. 5 when a small-signal voltage input is added in series with the DC bias input. Simplify your small-signal circuit as much as possible.