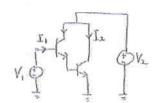
Nov. 12, 2015 Electronic Circuits 1 Prof. Woo-Young Choi

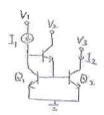
## Prob. 1 (20)

Determine the ratio of  $I_1$  and  $I_2$  ( $I_2$  /  $I_1$ ) in each of following circuits. Assume all BJT transistors in the forward active region and have the same value of  $\beta$ . Ignore the Early effect.





(b)(10)

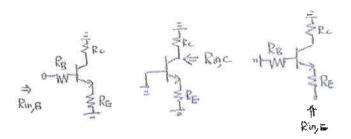


## Prob. 2(20)

We want to determine input resistances of an NPN transistor in the forward active region in various conditions. Express your answers in terms of small-signal parameters and  $\beta$ .

(a)(5) Determine  $R_{in,B}$ ,  $R_{in,C}$ ,  $R_{in,E}$  in the following circuits without the Early effect.

- (b)(5) Do the same as in (a) with the Early effect using  $r_0$ .
- (c)(5) Determine  $R_{\text{in,B}}$ ,  $R_{\text{in,C}}$ ,  $R_{\text{in,E}}$  when some resistors are added as shown below. Do not consider the Early effect.



(d)(5) Determine  $R_{in,C}$  in Prob. 1(c) with the Early effect using  $r_{o}$ .

## Prob. 3(30)

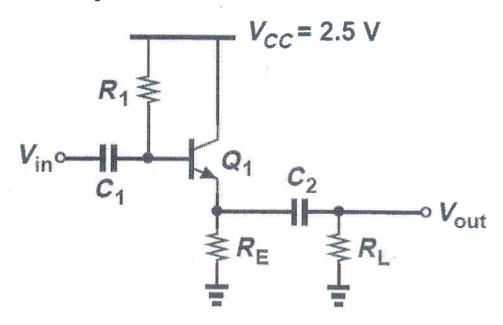
Consider the following amplifier in which CE stage is cascaded with CB stage. Assume the bias is achieved with an ideal current  $(I_1)$  and a voltage source  $(V_{b1})$  so that both transistors are in the forward active region and have the identical bias condition. The Early effect for both transistors can be modeled with the same resistance  $r_0$ . Determine the small-signal voltage gain  $(v_{out}/v_{in})$  in the following steps.

$$V_{\text{b1}} \sim V_{\text{out}}$$
 $V_{\text{in}} \sim Q_1$ 

- (a)(5) Determine the input resistance of the CB stage in the above circuit.
- (b)(5) Determine the voltage gain of the CE stage  $(v_X/v_{in})$ , where  $v_X$  is the voltage of  $Q_1$  emitter.
- (c)(5) Determine the voltage gain of the CB stage  $(v_{out}/v_X)$ .
- (d)(5) Determine the total voltage gain  $v_{\text{out}}/v_{\text{in}}.$
- (e)(10) Determine output resistance of the above amplifier.

## Prob. 4(30)

We want to design the bias circuit for the following EF circuit so that it can deliver voltage gain of 0.8 to a load having  $R_L = 50~\Omega$ . The transistor has  $I_s = 6 \times 10^{-16} A$ ,  $\beta = 100$ , and a large Early voltage so that the Early effect can be ignored. Assume  $V_T = 25 \text{mV}$  and the capacitors are selected so that they are open for bias and short for small signals.



(a)(10) Assuming  $R_{\text{E}}$  is much larger than  $R_{\text{L}}$ , determine the collect current that provides the desired gain.

(b)(10) What is required value for  $R_1$ ? Assume  $R_E = 250 \Omega$ .

(c)(10) Estimate the minimum value of  $C_1$  that allows delivery of input signals into the amplifier. Assume the lowest frequency for input signals is 100MHz. Use  $R_E=250~\Omega$ .