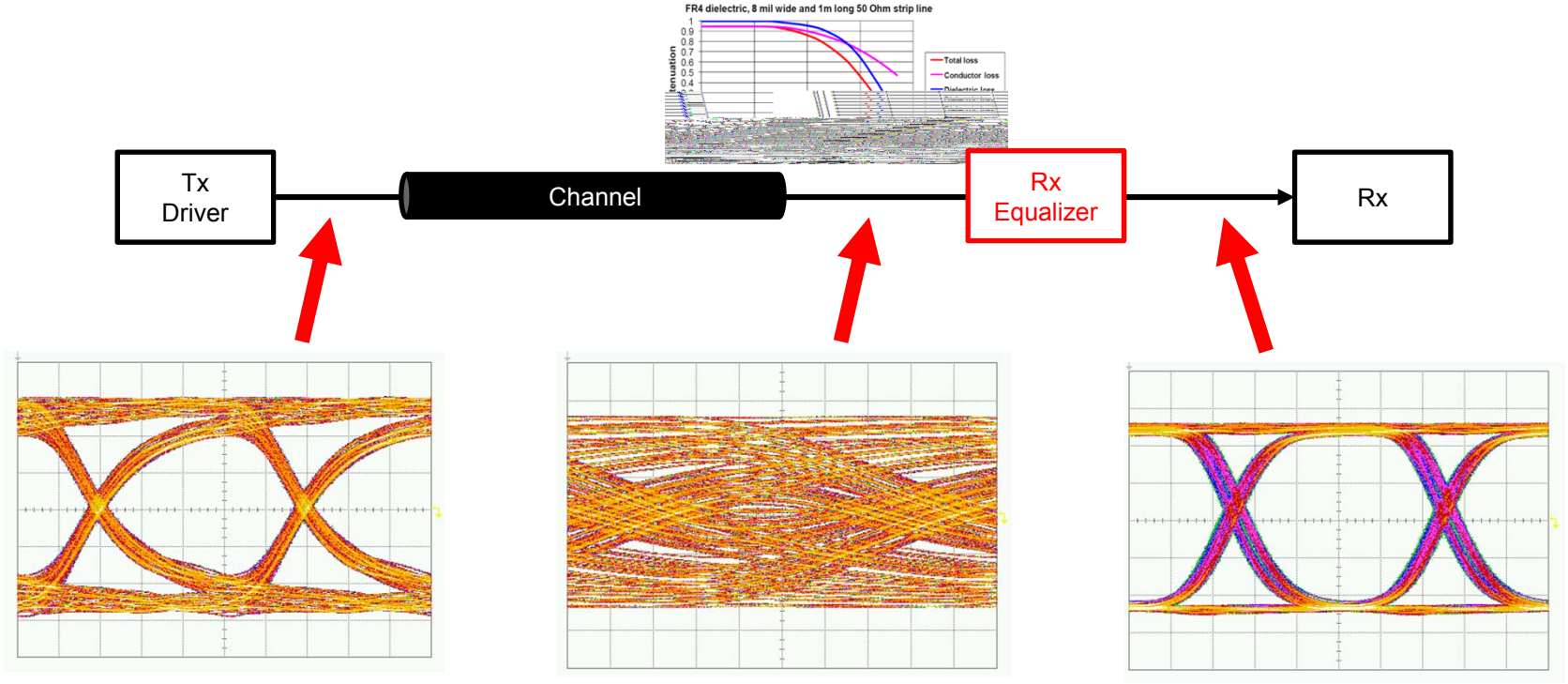
High-speed Serial Interface

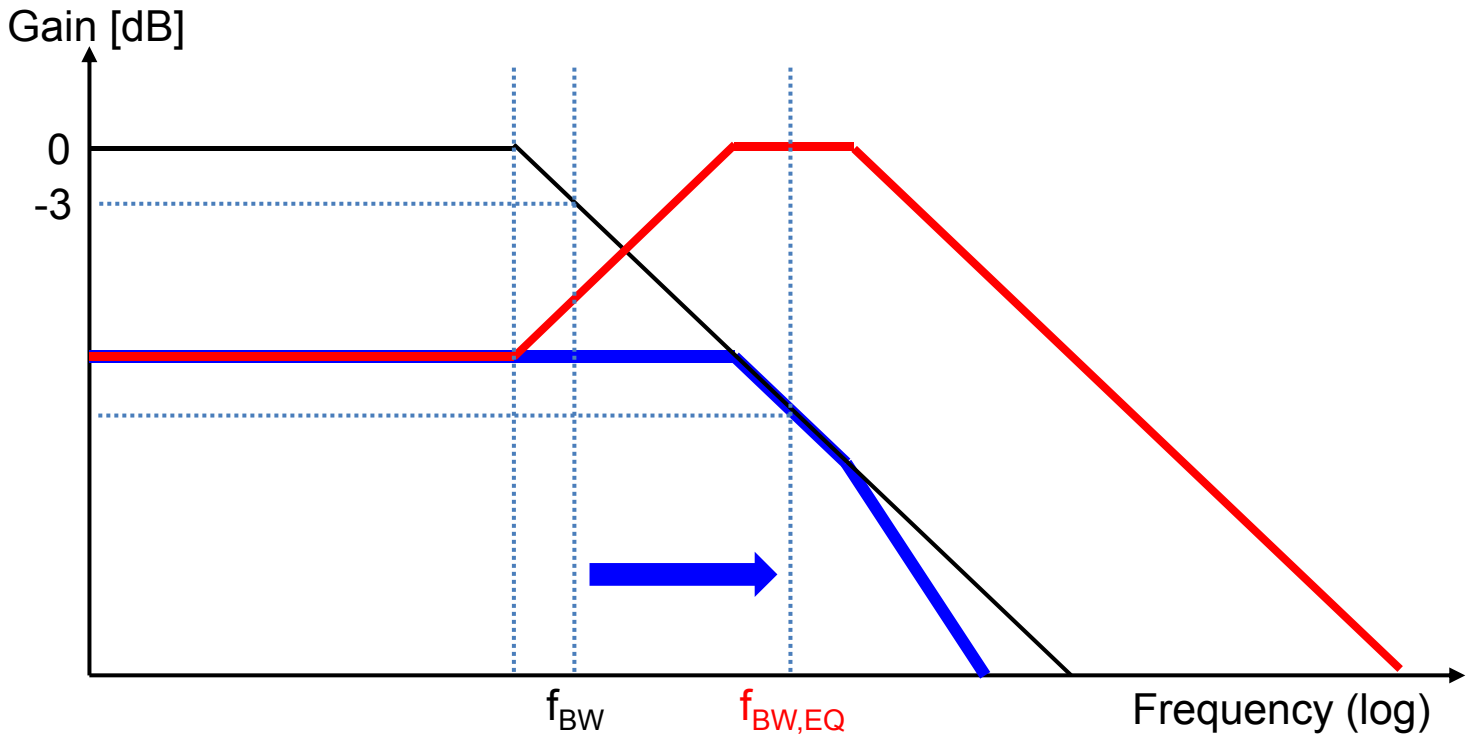
Lect. 9: Equalizers

Why equalization?

- Intersymbol interference (ISI) caused by frequency-dependent loss of channel



Linear Equalizer



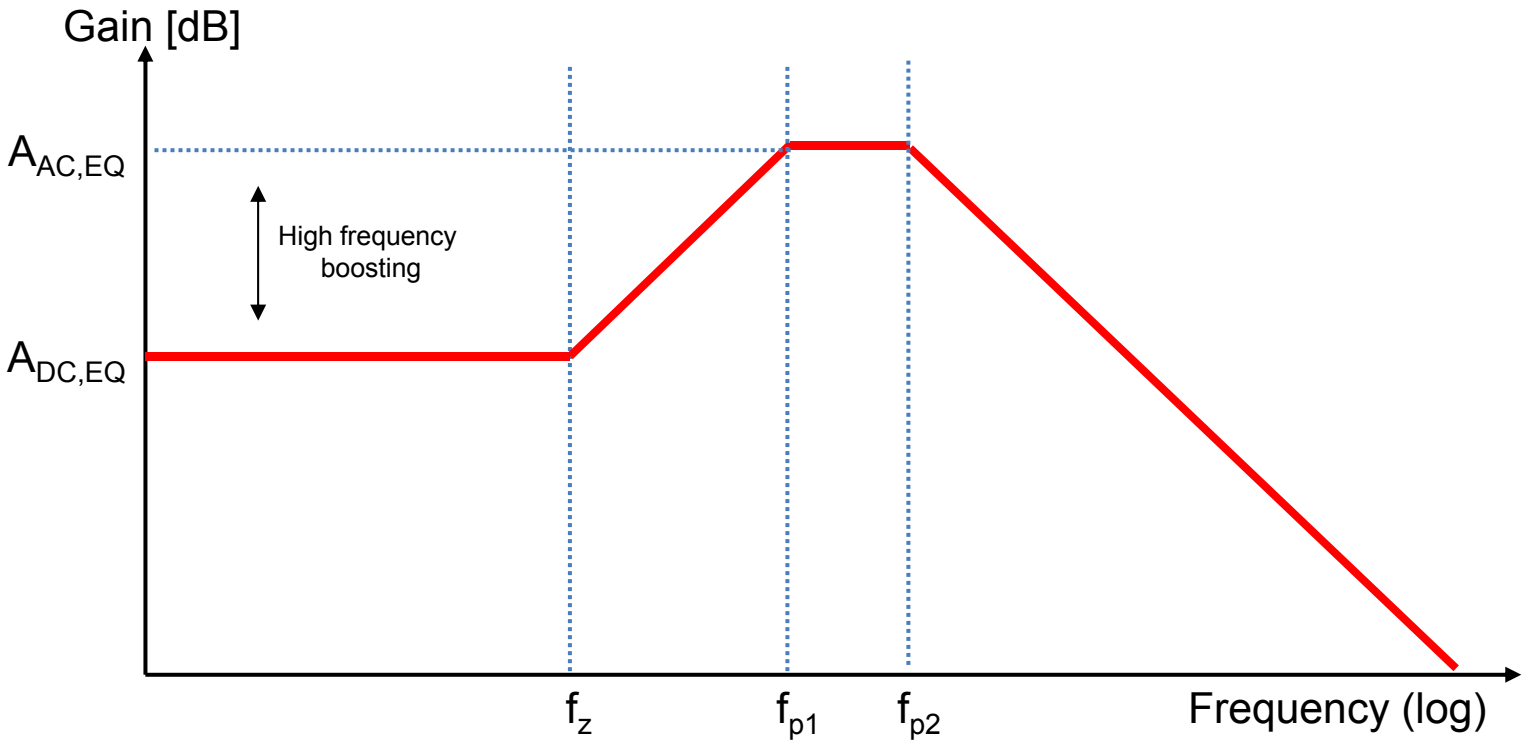
High-pass filter / High-frequency boosting

➔ Continuous Time Linear Equalizer (CTLE)

CTLE Frequency Response

Assuming channel has one pole,

CTLE should provide 1 zero and 2 poles



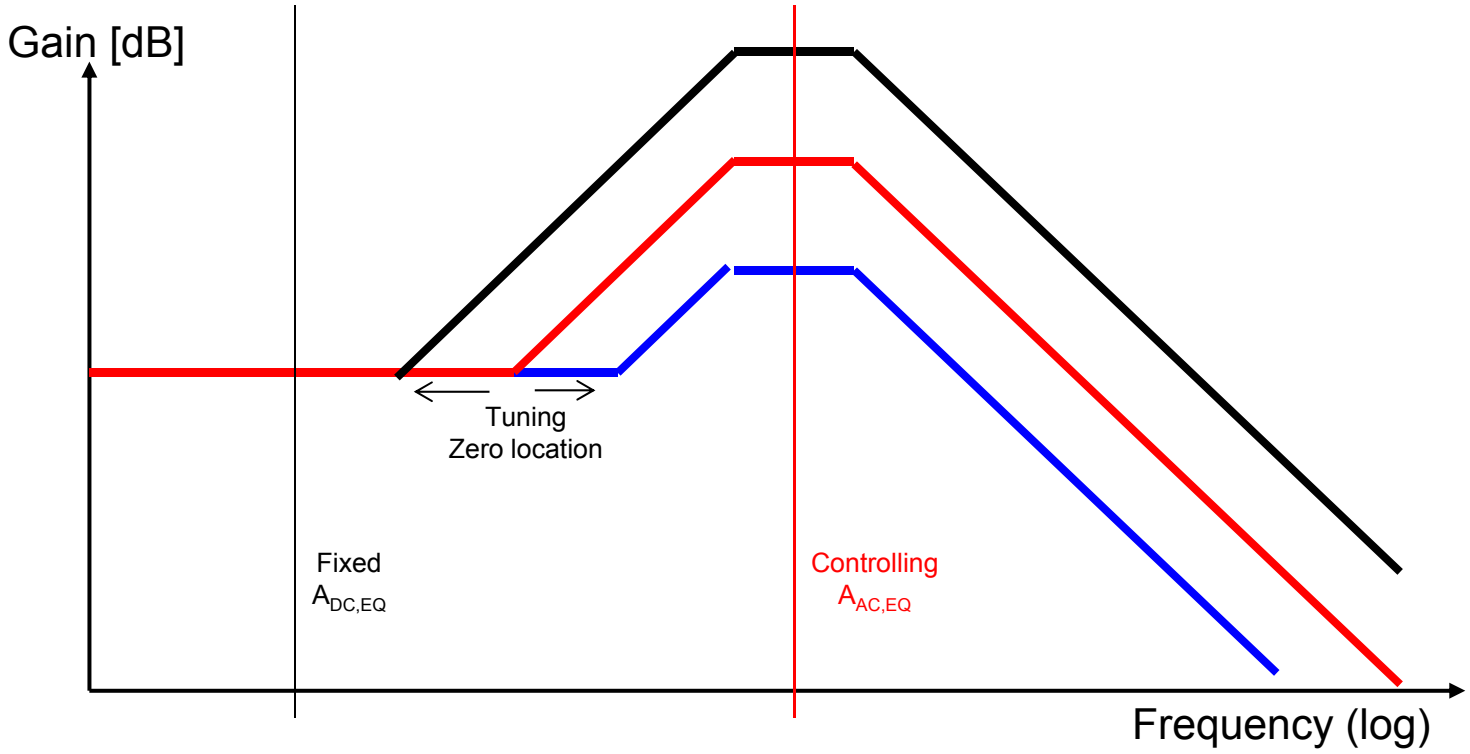
Tunability

- CTLE should be tunable
  - Channel variation
    - Variations in channel fabrication
    - Uncertainty in channel modeling
    - Channel degradation/defect after usage
  - PVT variation of equalizer

➔ Tunability is a must

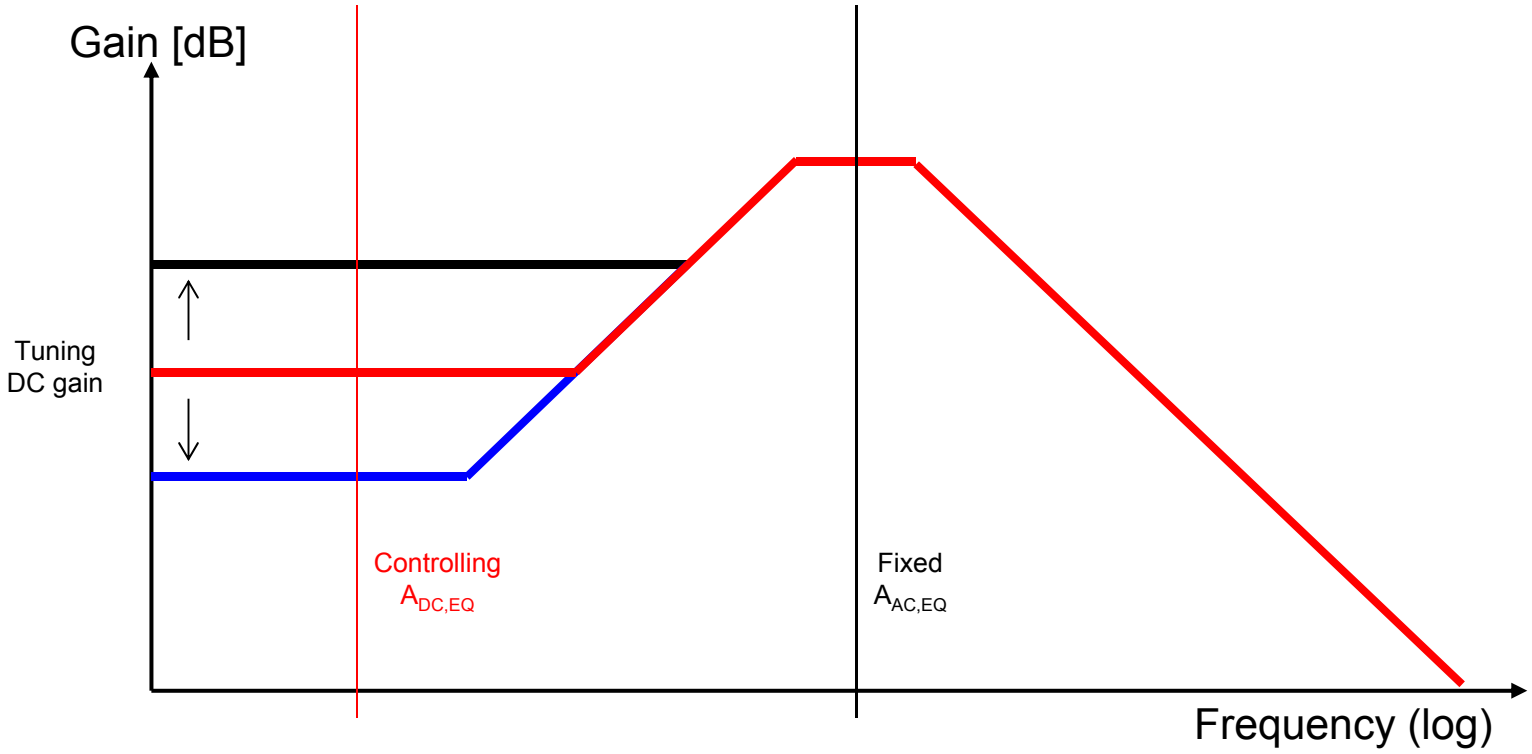
Tunability

- Tuning for pole/zero locations



Controllability

- Tuning DC gain



Passive CTLE

– Various passive high-pass filters available

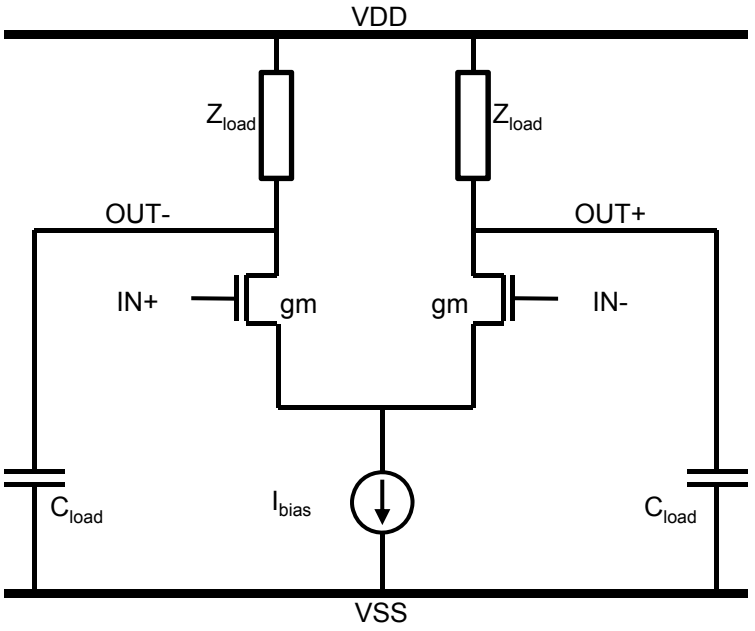
No power consumption
But
- Lossy
- PVT dependent
- Difficult to achieve 50-ohm matching
- Difficult to tune
- Often large size

Active CTLE

- Differential amplifier
  - Basic differential amp. has
    1 pole from load capacitance

$$|H(j\omega)| \sim A_{DC}\left(\omega_{-3dB} \;//\; \frac{1}{j\omega C_{load}}\right)$$

$$\text{or} \quad \frac{A_{DC}}{\left(j\omega C_{load} R_{load} \frac{1}{\omega_{-3dB}}\right)}$$



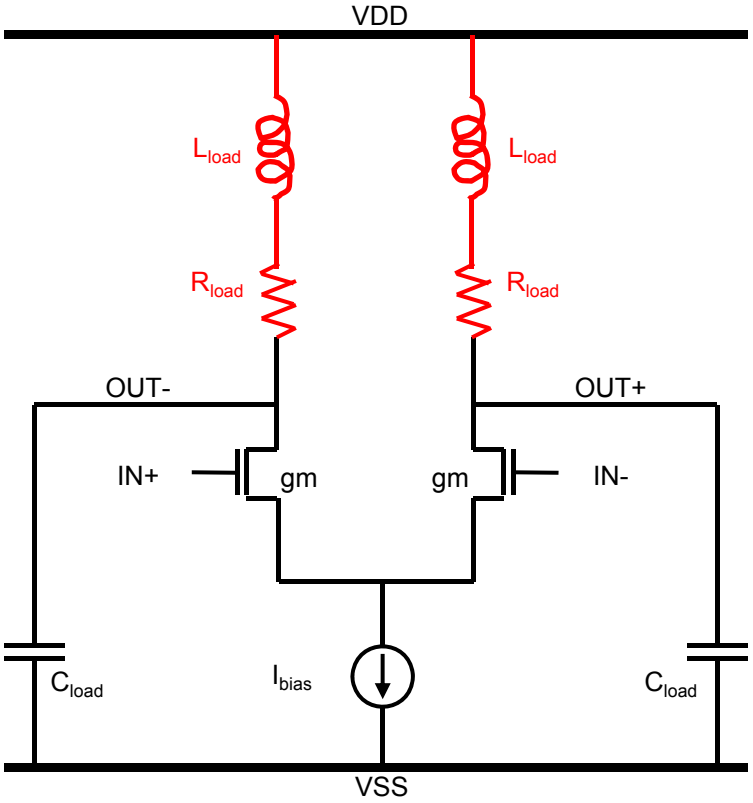
Active CTLE

- Inductive load
  - Shunt inductor provides a pole/zero pair

$$|H(j\omega)| \sim g_m \left(\omega_{zero} \;//\; \frac{1}{j C_{load}} \right)$$

$$\approx \frac{g_m}{\left(j C_{load} + \frac{1}{j L_{load} + R_{load}} \right)}$$

$$\approx \frac{g_m \left(j L_{load} + R_{load} \right)}{\left(-\omega^2 L_{load} C_{load} + j \omega R_{load} C_{load} + 1 \right)}$$



Source Degeneration for CTLE

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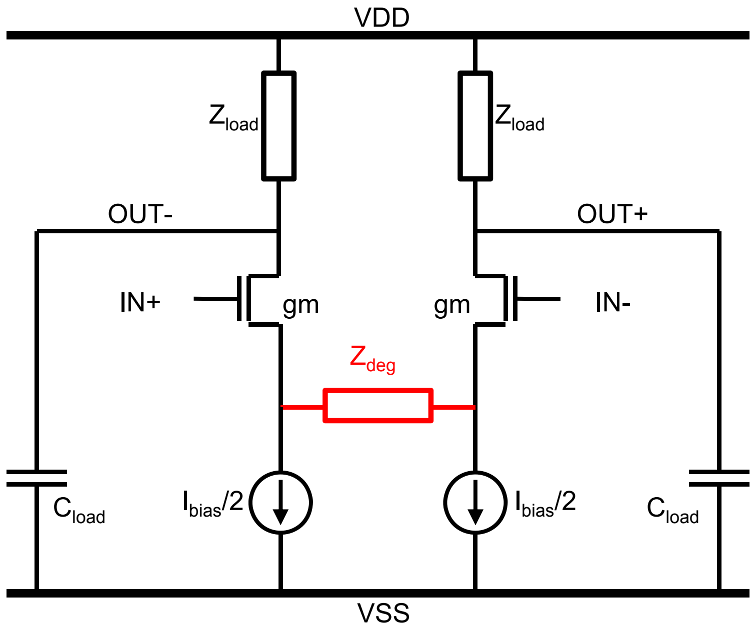
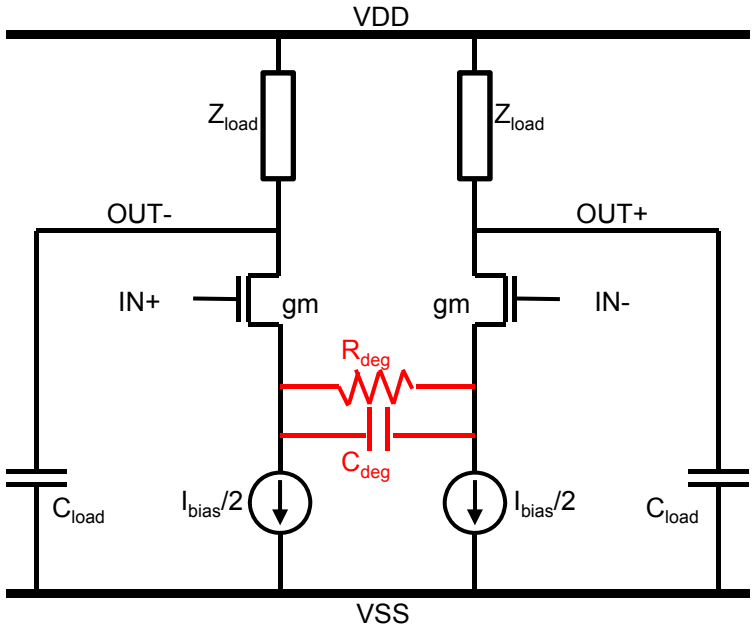


Source Degeneration for CTLE

– Capacitive generation provides high-frequency boosting since a capacitor has lower impedance at high frequency

$$\frac{V_{out}}{V_{in}} \approx \frac{g_m}{1 + g_m \frac{1}{2}\left(R_{deg} \,//\, \frac{1}{sC_{deg}}\right)}$$

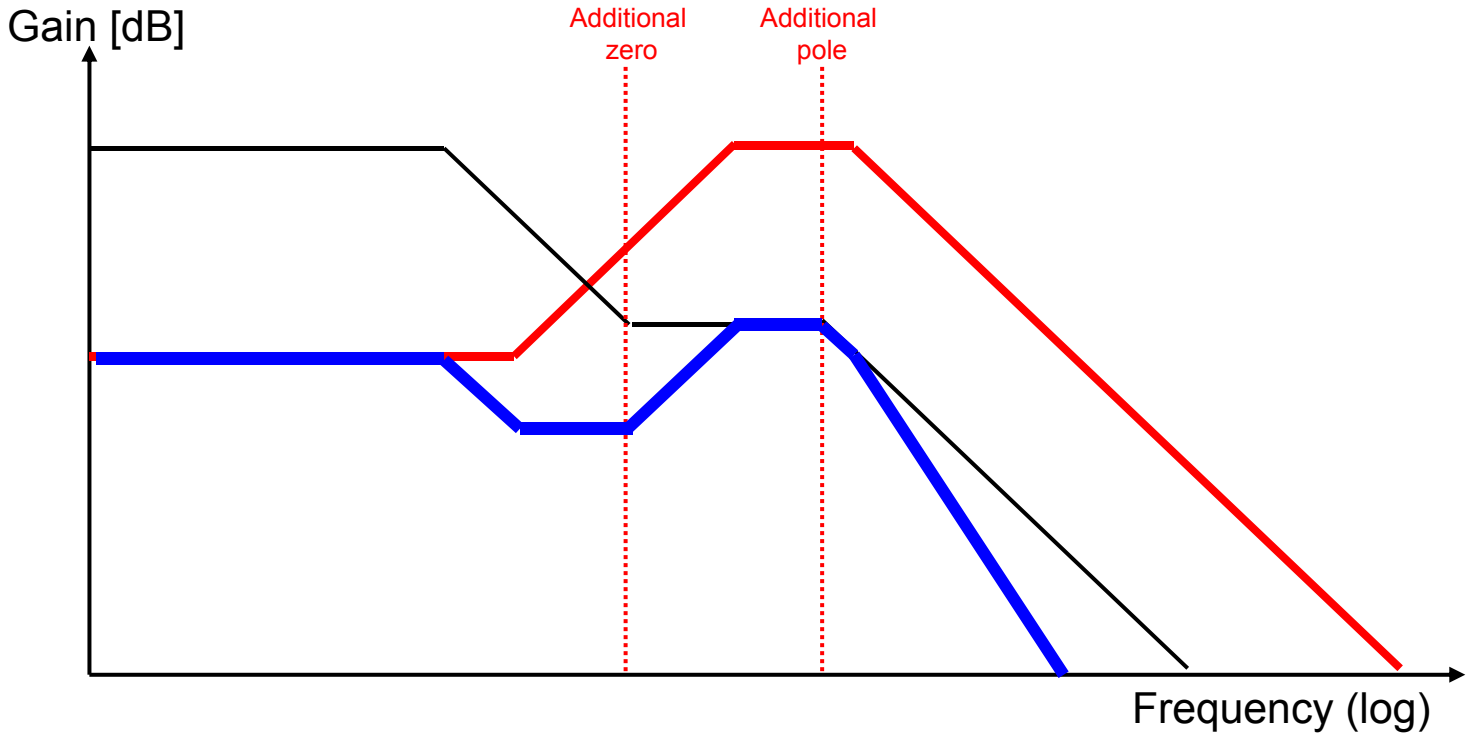
$$\frac{V_{out}}{V_{in}} \approx \frac{g_m}{C_{deg}} \frac{\left[s + \frac{1}{R_{deg}C_{deg}}\right]}{\left[s + \frac{1}{R_{deg}\frac{C_{deg}}{2}}\right]\left[s + \frac{1}{R_{deg}C_{load}}\right]}$$



➔ Design Exercise

Limitations of CTLE

- Channels may not be properly modeled with one pole



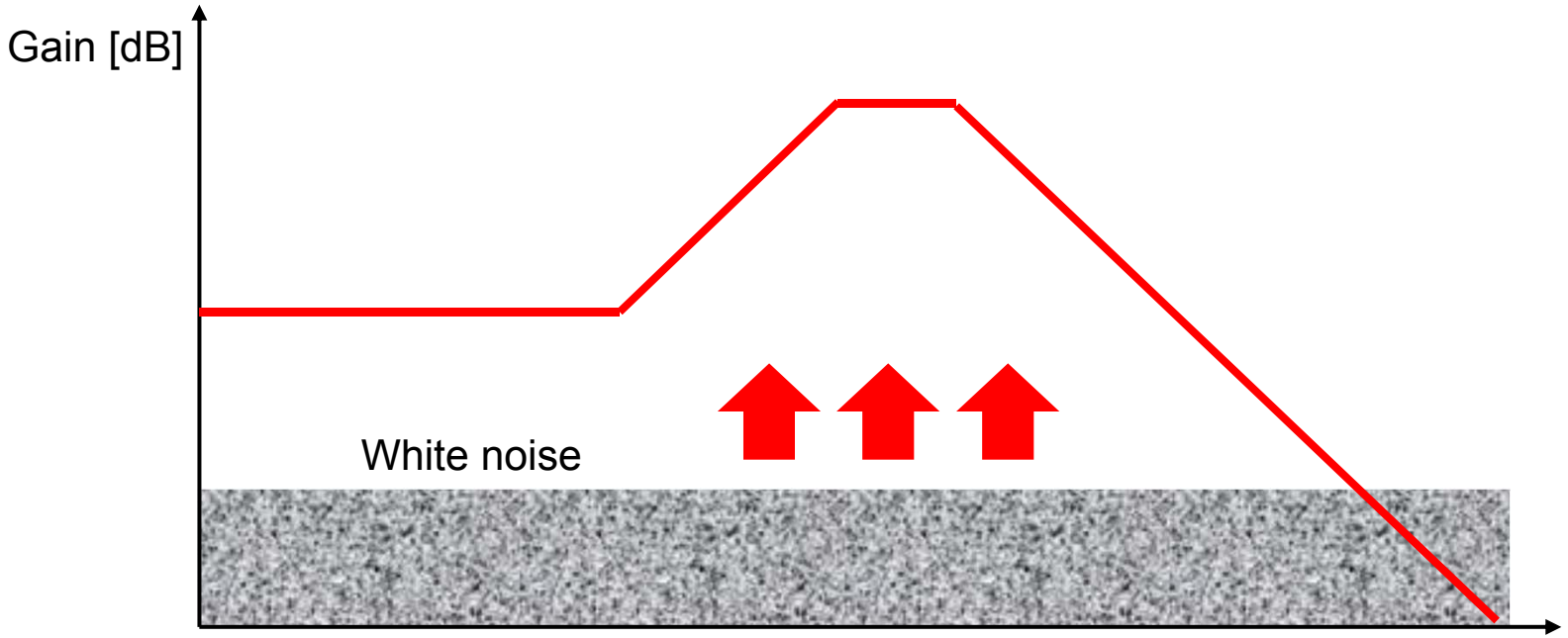
Limitations of CTLE

- Applicable to only ISIs due to linear frequency-dependent loss

- Other causes for ISI are;
  - Impedance mismatching
  - Differential offset
  - Cross-talk
  - Parasitic poles and zeros (ex: package parasitic)

Limitations of CTLE

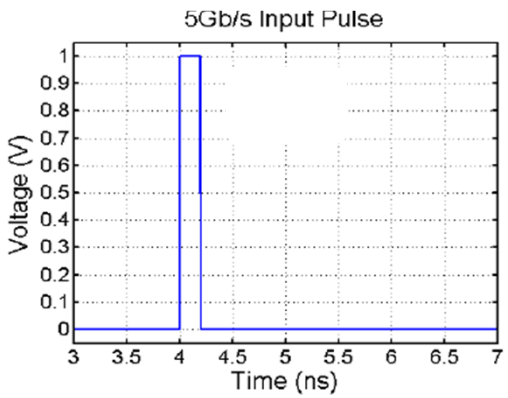
- High-frequency Noise boosting

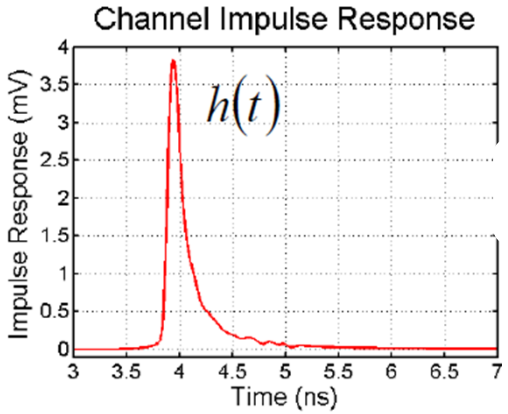


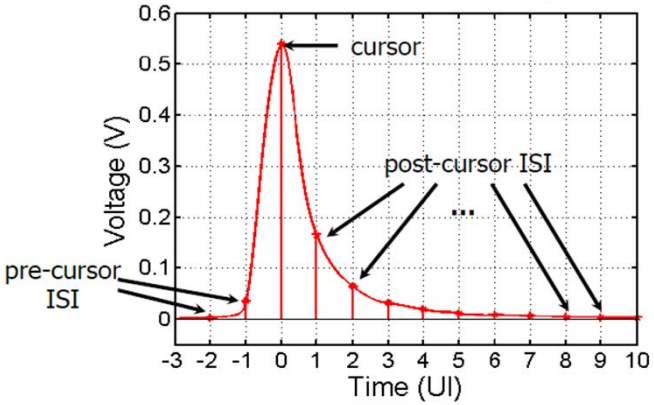
Time-Domain Analysis

– Frequency-Domain Analysis
  - Freq. Response of Input x Freq. Response of Channel x Equalizer
    = Freq. Response of Output

– Time-Domain Analysis





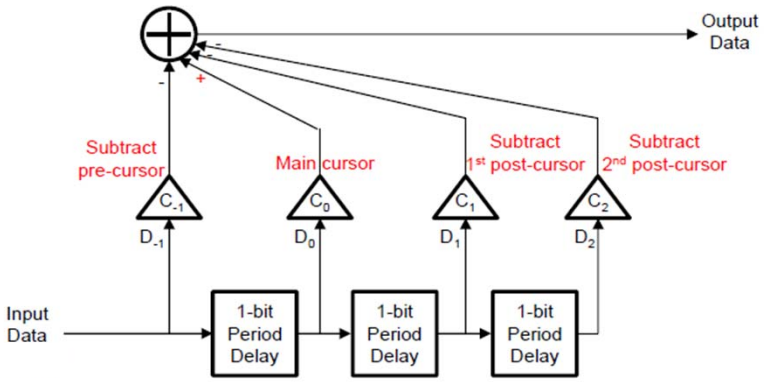


- Equalization: Force pre- and post-cursors to zero

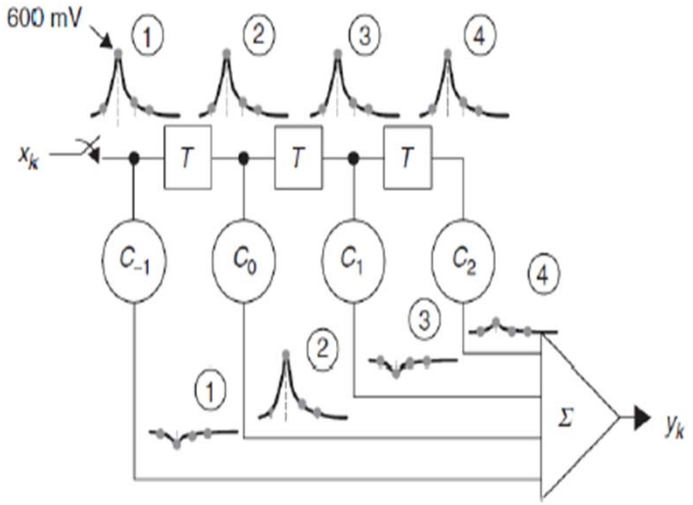
FIR Filter

- Any CTLE filter can be converted into a discrete-time domain filter

- IIR (Infinite Impulse Response) ➔ FIR (Finite Impulse Response)



Tap and Delay

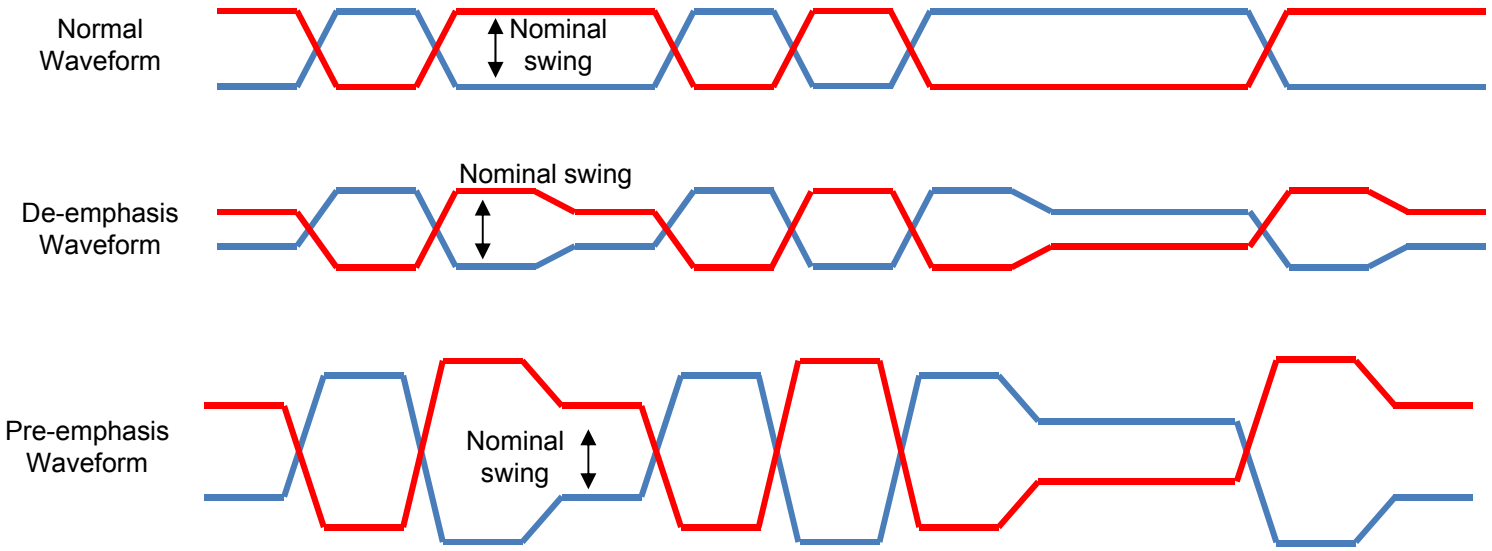


- Hard to implement Rx FIR filter because the precise amount of delay (clock period) is not available in Rx

➔ Tx FIR filter

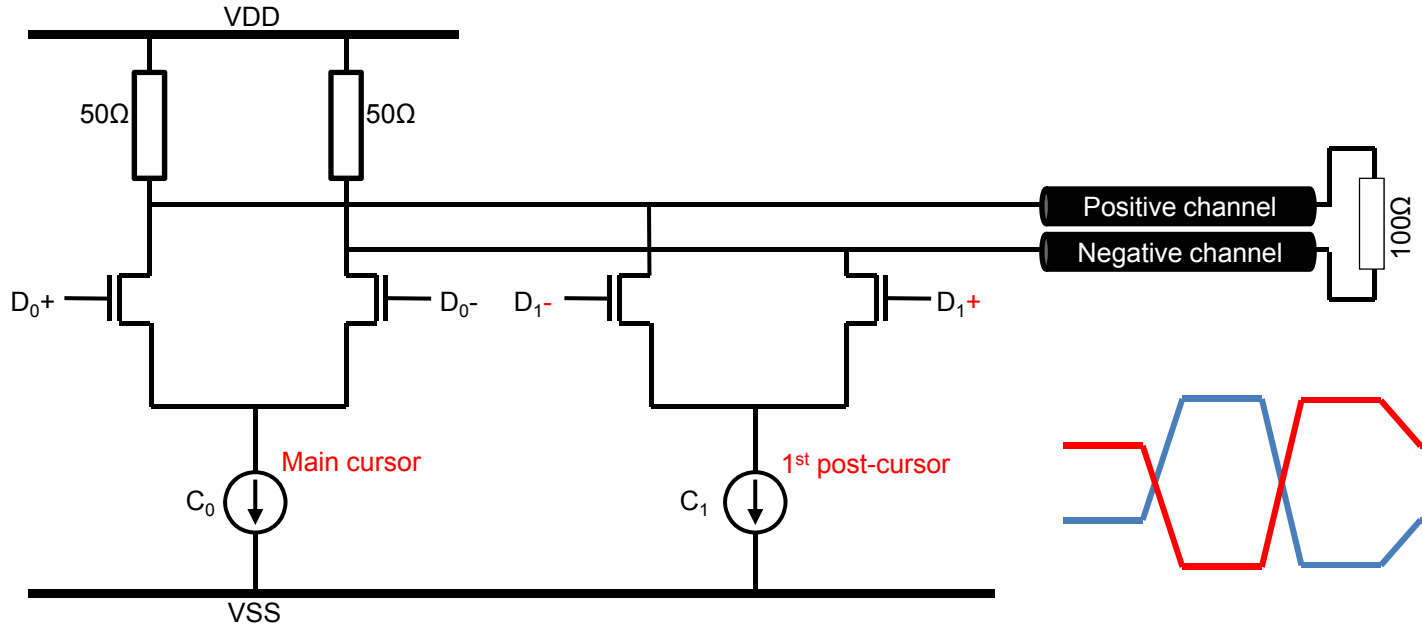
Pre-/De-Emphasis

– Tx FIR is also called Feed-Forward Equalizer (FFE) or Pre-/De-Emphasis
  - Pre-emphasis: to enhance high-frequency components
  - De-emphasis: to reduce low-frequency components



Circuit implementation

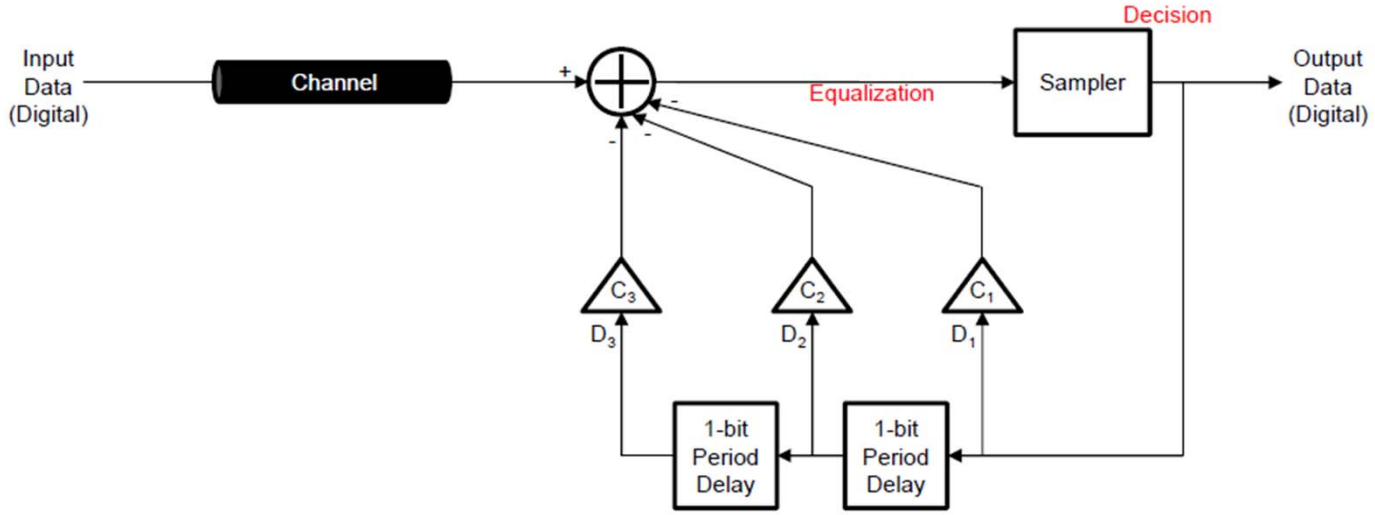
- Current-mode drivers can be easily used for pre-/de-emphasis
  - $D_1=D_0 \rightarrow V_{out,diff} = +/-50 \times (C_0-C_1)/2$
  - $D_1 \neq D_0 \rightarrow V_{out,diff} = +/-50 \times (C_0+C_1)/2$
  - Level difference is defined as sum and subtract



➔ Design Exercise

Decision Feedback Equalizer (DFE)

- Non-linear equalization based on sampling



- Complicated but can provide high-performance equalization
- Requires clock signals for sampling
- Often used with CTLE