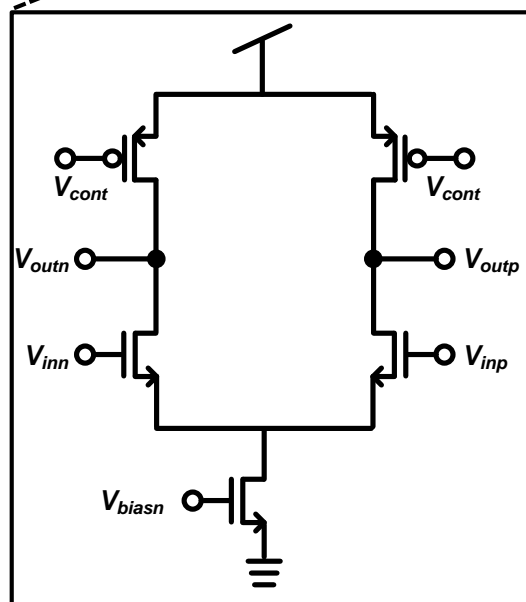
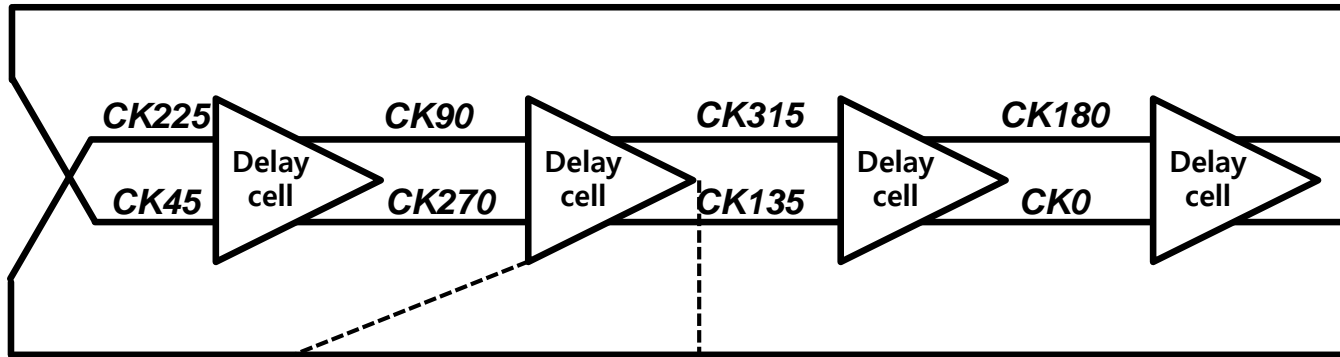


High-Speed Serial Interface Circuits and Systems

Design Exercise2 – Ring Voltage Controlled Oscillator (VCO)

Oscillator Structure

- ✓ 4-stage Ring VCO using differential delay cell



$$\omega_0 = \frac{1}{RC}$$

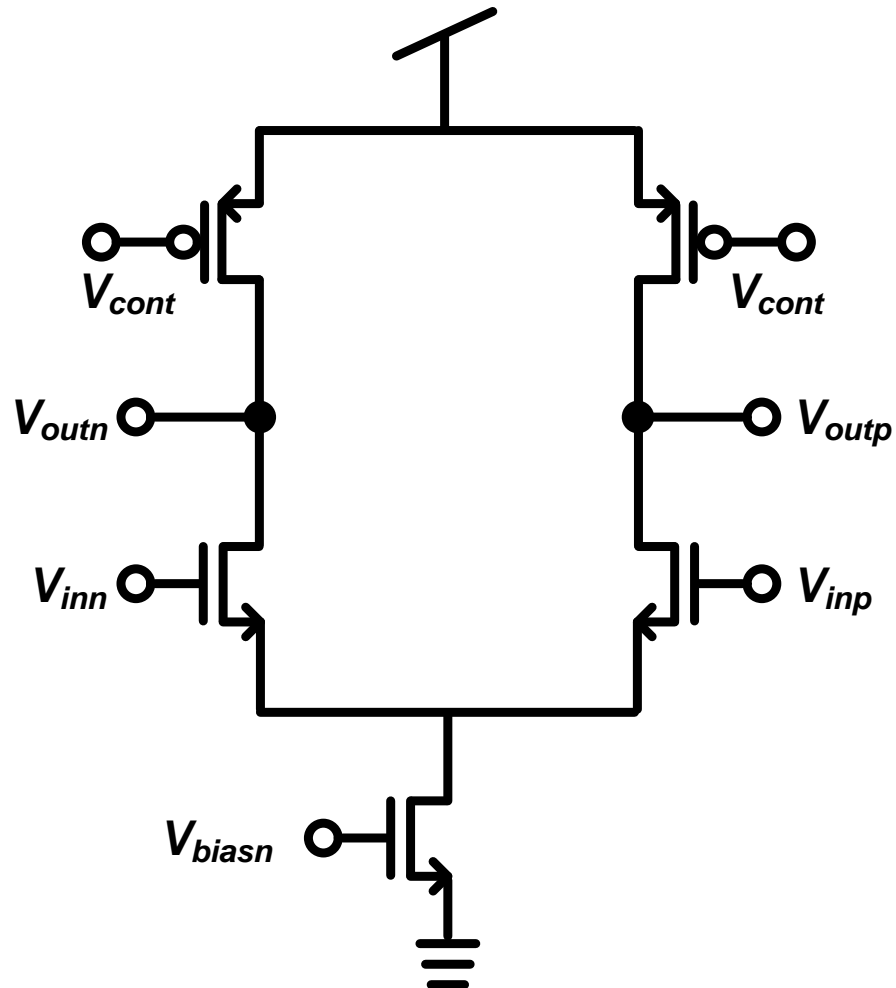
$$R_{on} = \frac{1}{\mu_n C_{ox} W/L (V_{gs} - V_{th})}$$

Design Example

- ✓ 8-phase, 4-stage voltage controlled oscillator (VCO)
 - Supply voltage: 1.8V
 - Minimum voltage swing: 300mV
 - Frequency tuning range: 100 ~ 200-MHz
with range of V_{cont} as 0~0.5V
 - Oscillation frequency @ $V_{cont}=0.4V$: 700~800-MHz

Details of Delay Cell

✓ Differential type delay cell



► PMOS

- Length : 1u
- Width : 40u (finger : 4)

► INPUT NMOS

- Length : 0.180u
- Width : 20u (finger : 2)

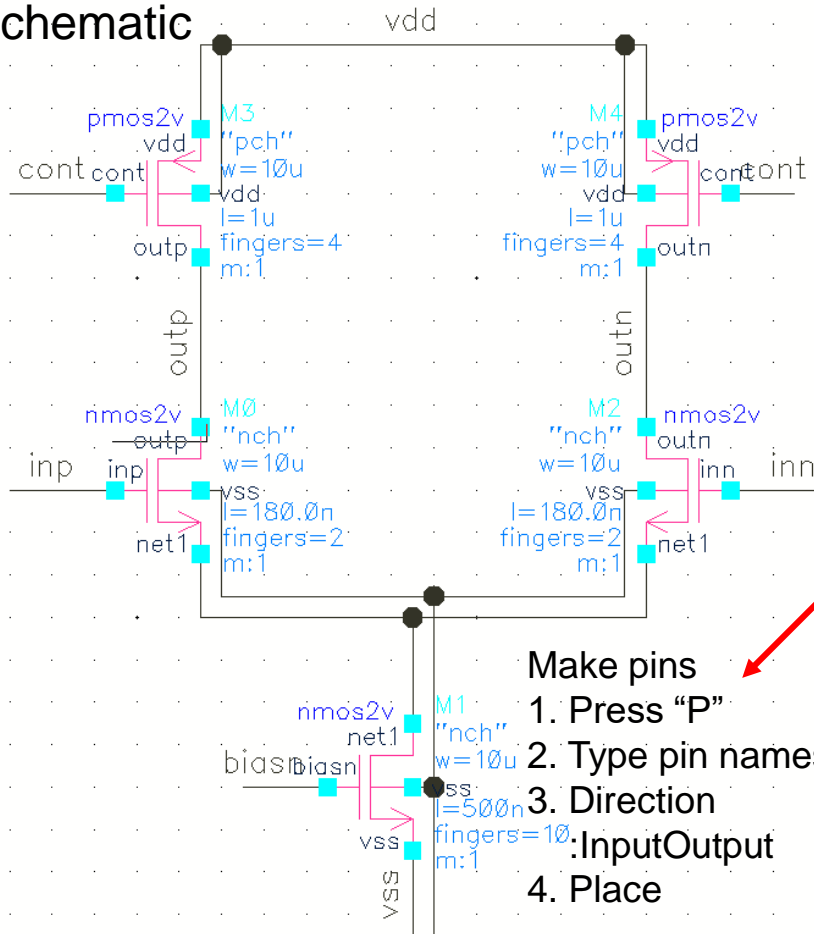
► Source NMOS

- Length : 0.500u
- Width : 100u (finger : 10)

► $V_{biasn} = 600 \text{ mV}$

Schematic & Symbol of Delay Cell

① Schematic



Pins

vdd
vss

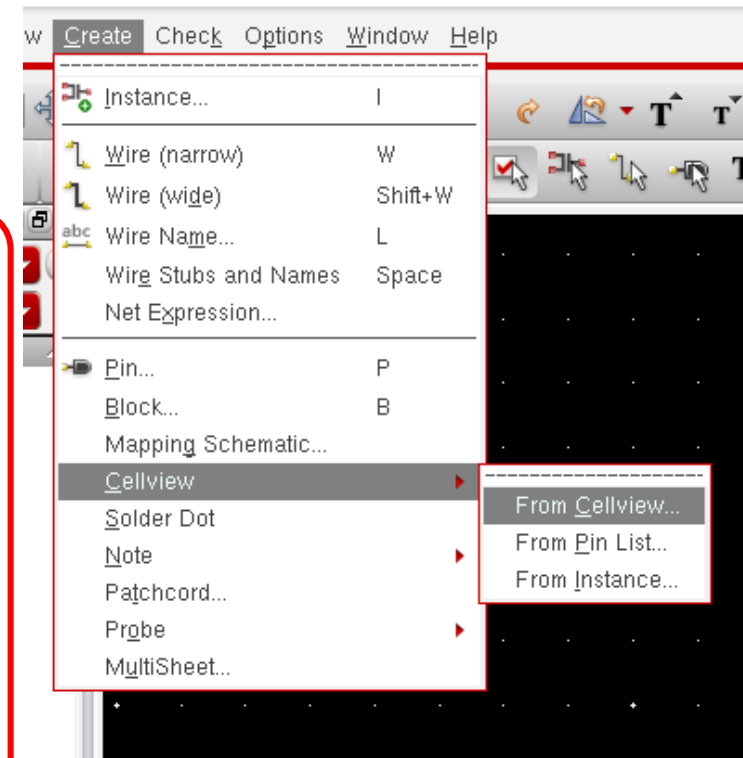
inp
inn

outp
outn

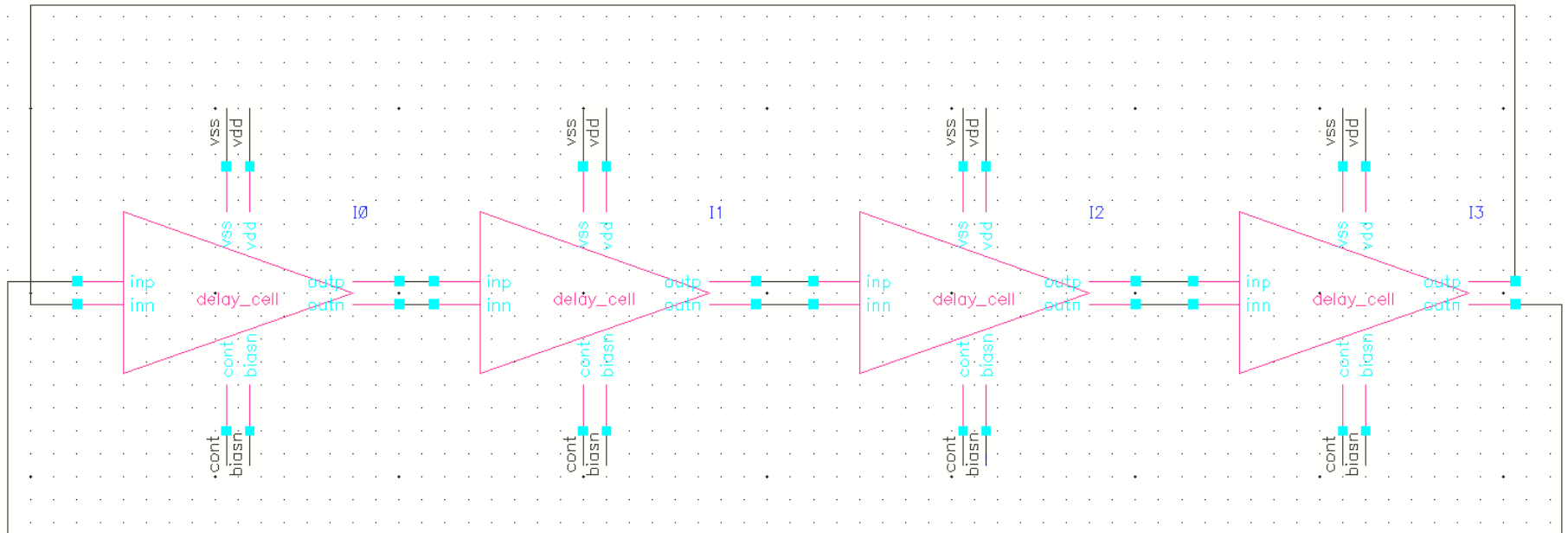
cont
biasn

② Make symbol of schematic

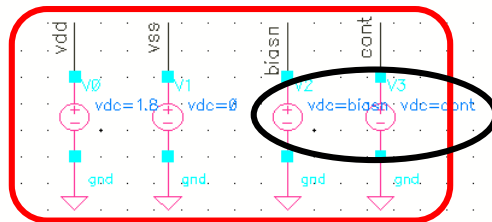
tor L Editing: Week2_pre delay_cell schematic



Simulation Testbench Schematic



Sources

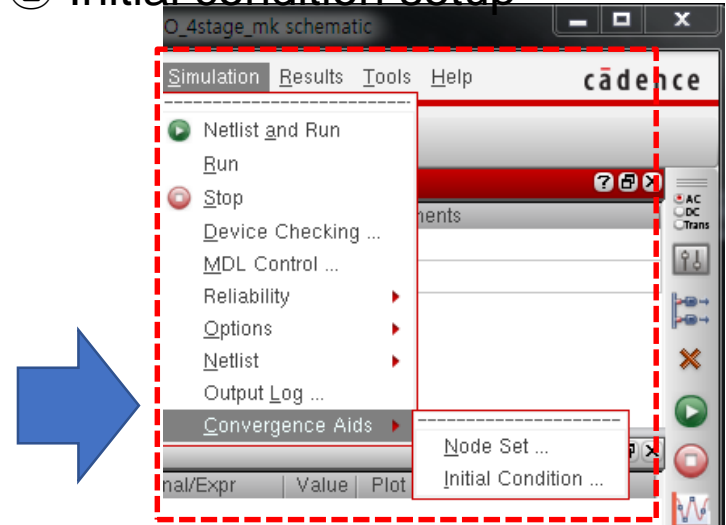
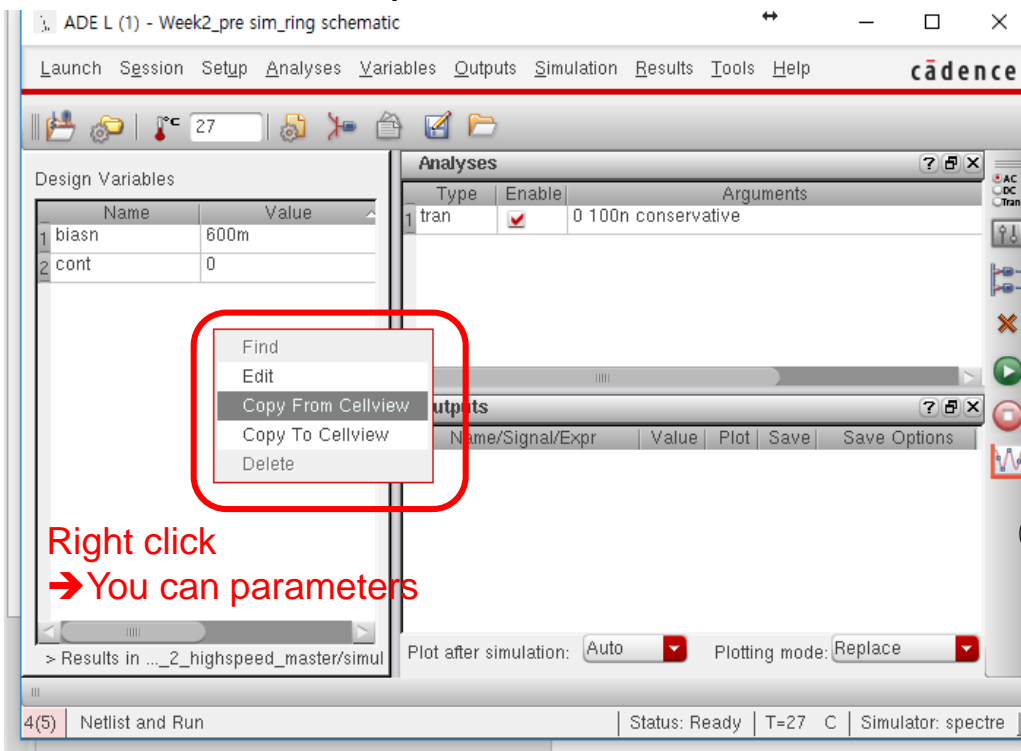


You can parameterize values
using text for your convenience

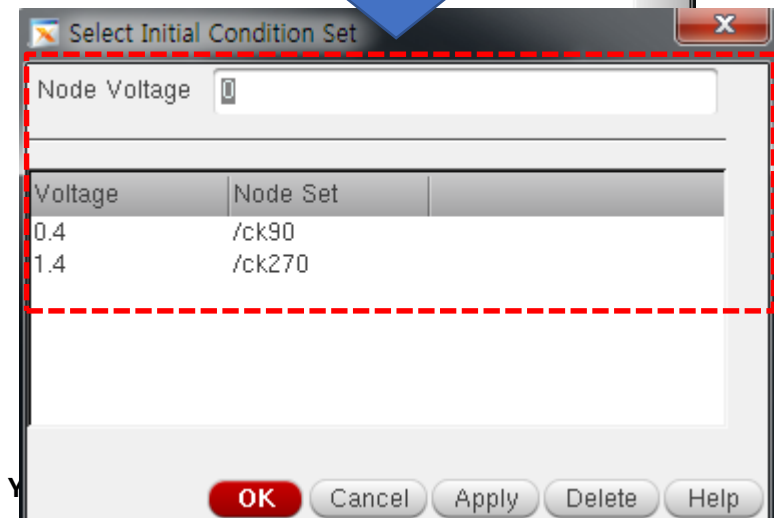
Transient Simulation

② Initial condition setup

① Simulation setup

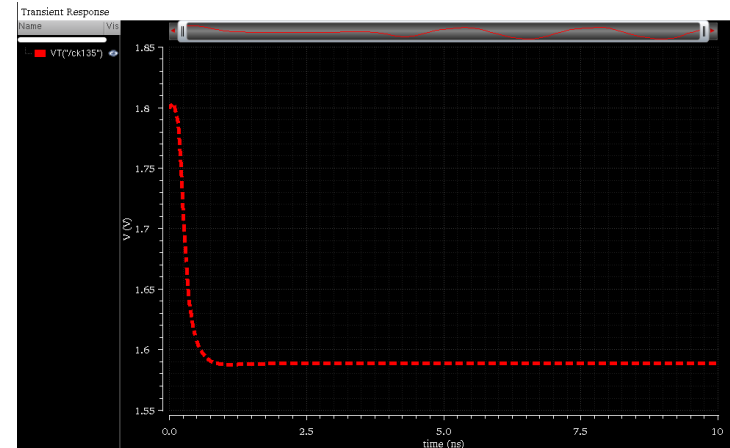
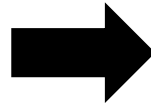
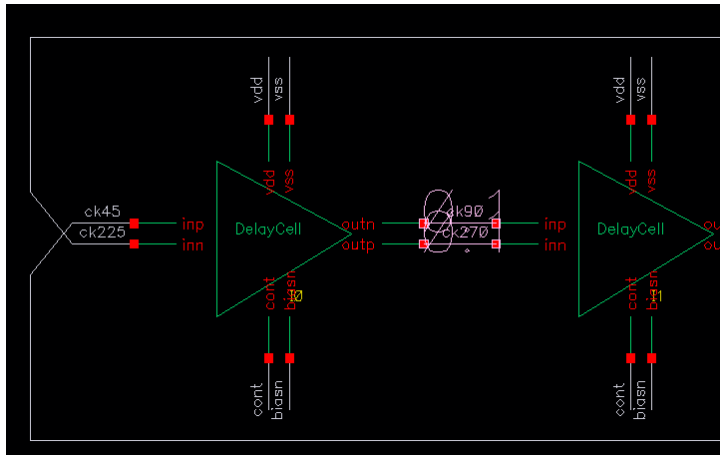


③ Initial condition

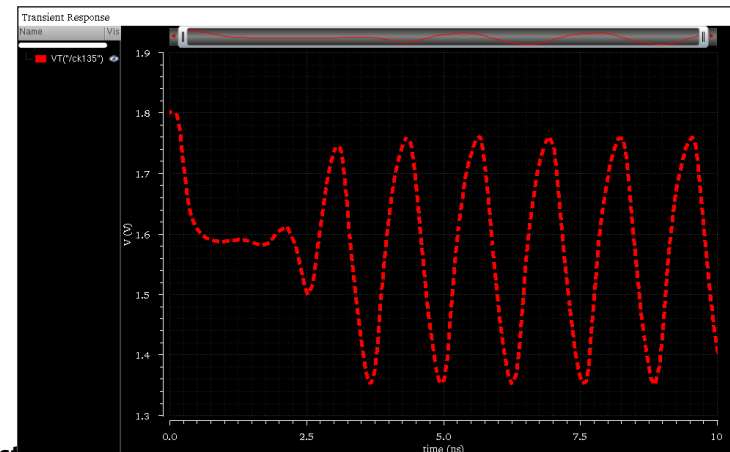
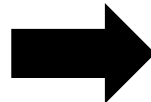
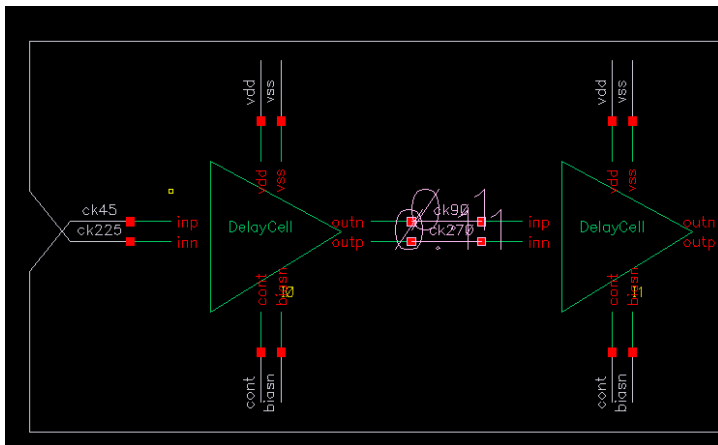


Initial Condition Value Examples

- ✓ Initial condition change
 - CK90 : 0.1V & CK270 0.1V

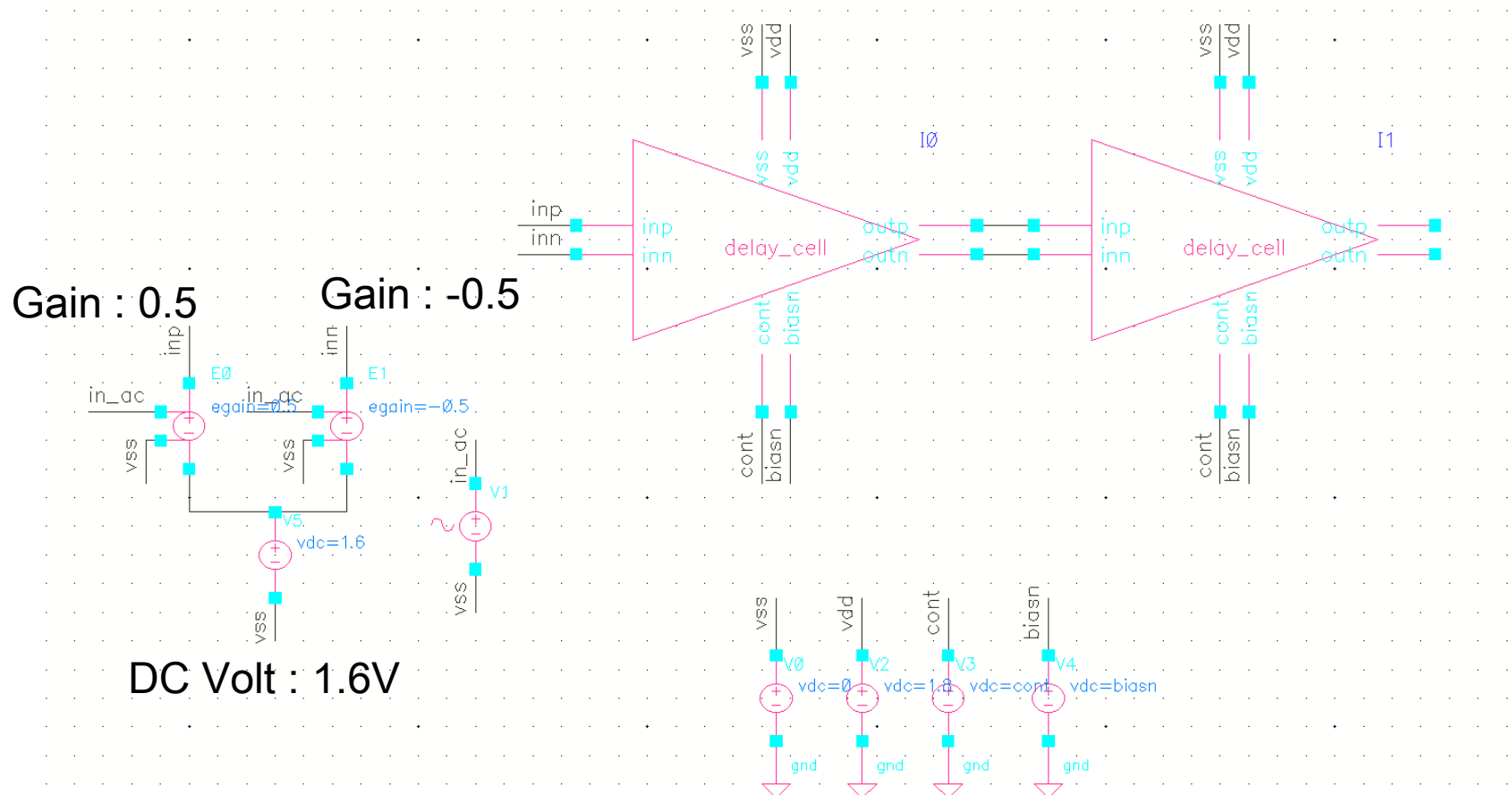


- CK90 : 0.1V & CK270 0.11V

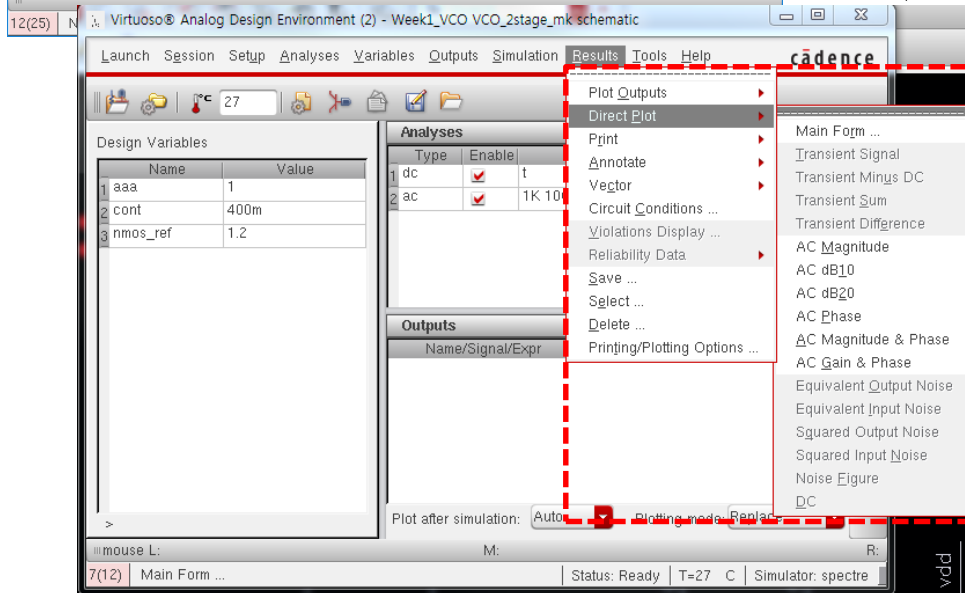
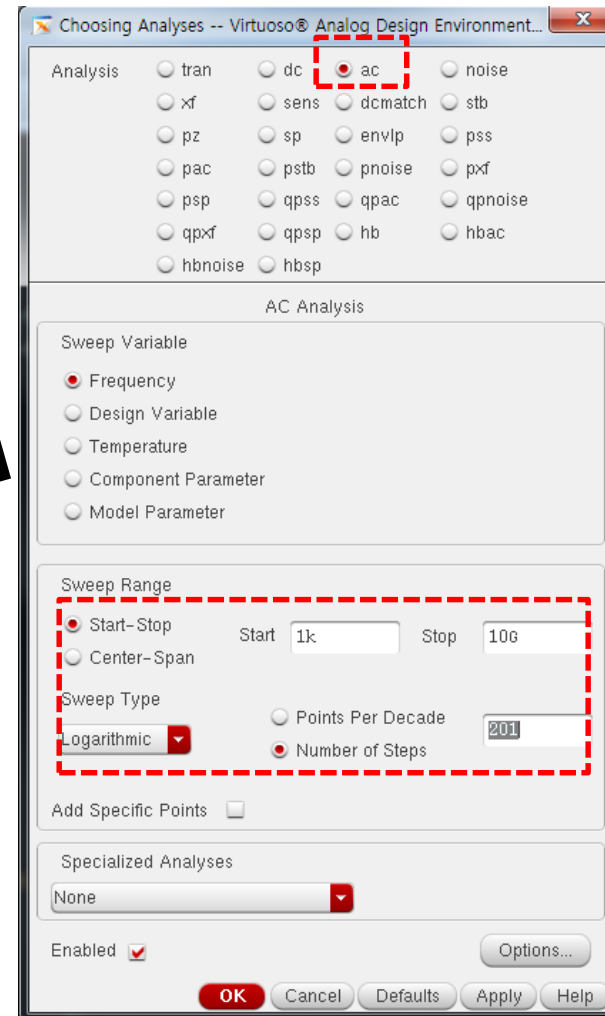
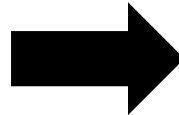
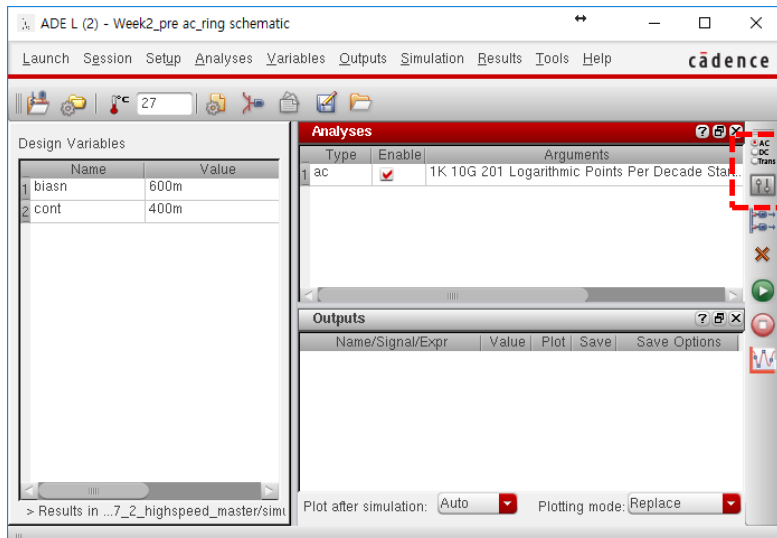


Small-Signal Simulation (AC)

- ✓ Schematic design
 - 2-stage delay cell 구성
 - Vsin source 이용 (AC magnitude 1)



AC Simulation



Oscillation Frequency Estimation

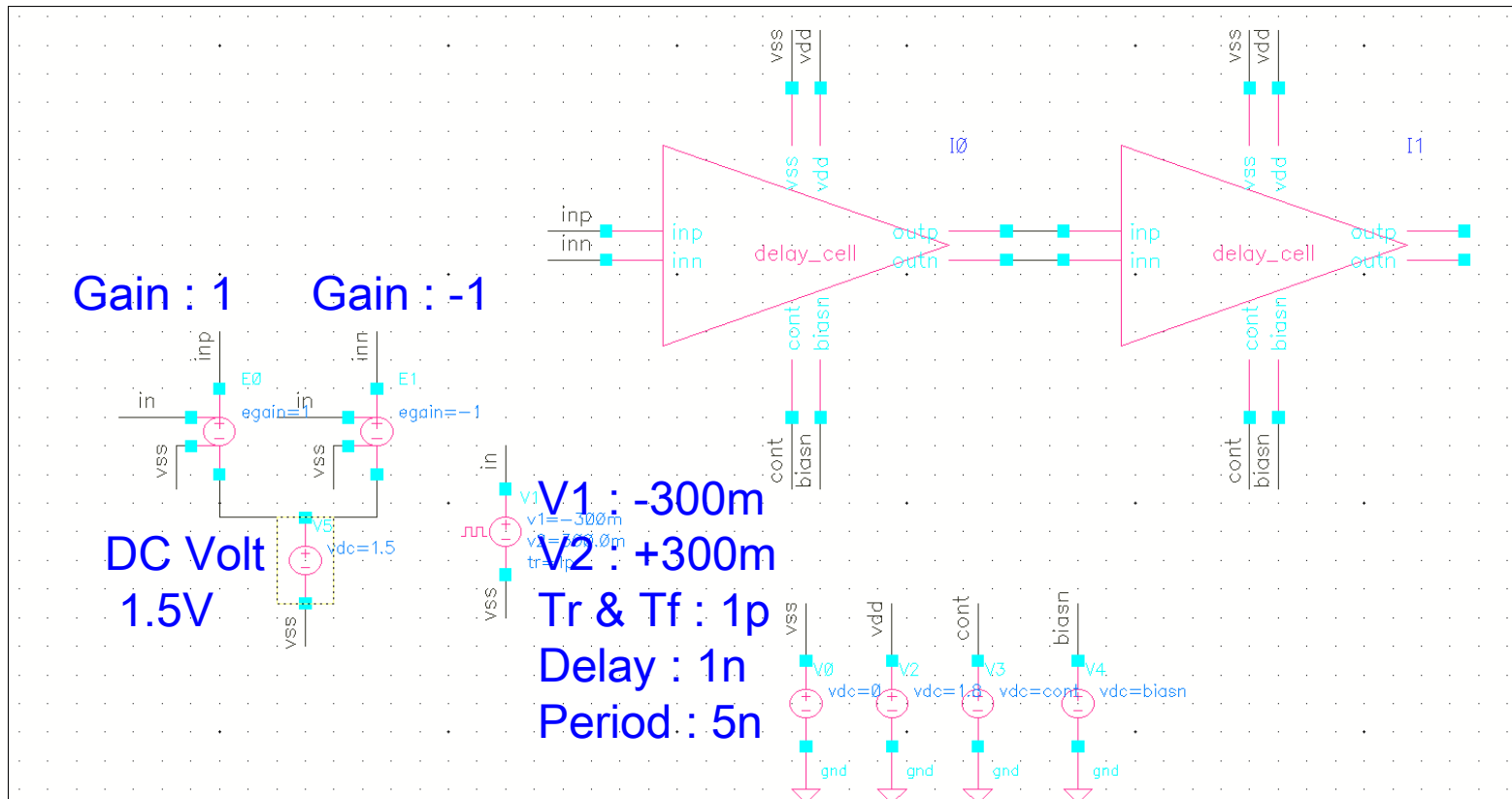
- Open loop & closed-loop analysis

- $H(s) = \frac{A_0^4}{\left(1 + \frac{s}{\omega_0}\right)^4} \quad / \quad \tan^{-1} \frac{\omega_{osc}}{\omega_0} = 45^\circ$

- ➔ $\omega_{osc} = \omega_0 (A_0 = \sqrt{2})$

Pulse Response Simulation

- ✓ Schematic design
 - 2-stage delay cell 구성
 - Vpulse source 이용



Parameter Sweep

The screenshot shows the Cadence Virtuoso Analog Design Environment. The main window displays the 'Design Variables' table and the 'Analyses' table. The 'Parametric Analysis' dialog is open, showing the variable 'nmos_ref' being swept from 0 to 1.2 in linear steps of 0.3. A large black arrow points from the main window to the dialog.

Design Variables

| Name | Value |
|------------|-------|
| 1 nmos_ref | 1.2 |
| 2 cont | 400m |

Analyses

| Type | Enable | Value |
|--------|-------------------------------------|-------|
| 1 tran | <input checked="" type="checkbox"/> | 0.50n |
| 2 dc | <input type="checkbox"/> | t |

Parametric Analysis - spectre(1): Week1_VCO VCO_4stage_mk schematic

File Analysis Help

Ready

Run Mode: Sweeps & Ranges

| Variable | Value | Sweep? | Range Type | From | To | Step Mode | Step Size |
|----------|-------|-------------------------------------|------------|------|-----|--------------|-----------|
| nmos_ref | 1.2 | <input checked="" type="checkbox"/> | From/To | 0 | 1.2 | Linear Steps | 0.3 |

Homework

- ✓ Verify and plot 8-phase output of VCO, and derive K_{VCO} by changing V_{cont} from 0V to 0.5V
- ✓ Compare and analyze frequency of oscillator with small-signal analysis (pole, phase response) and large-signal analysis (pulse response) and transient simulation result.
- ✓ Due: 18 Sep. in class (Hardcopy)