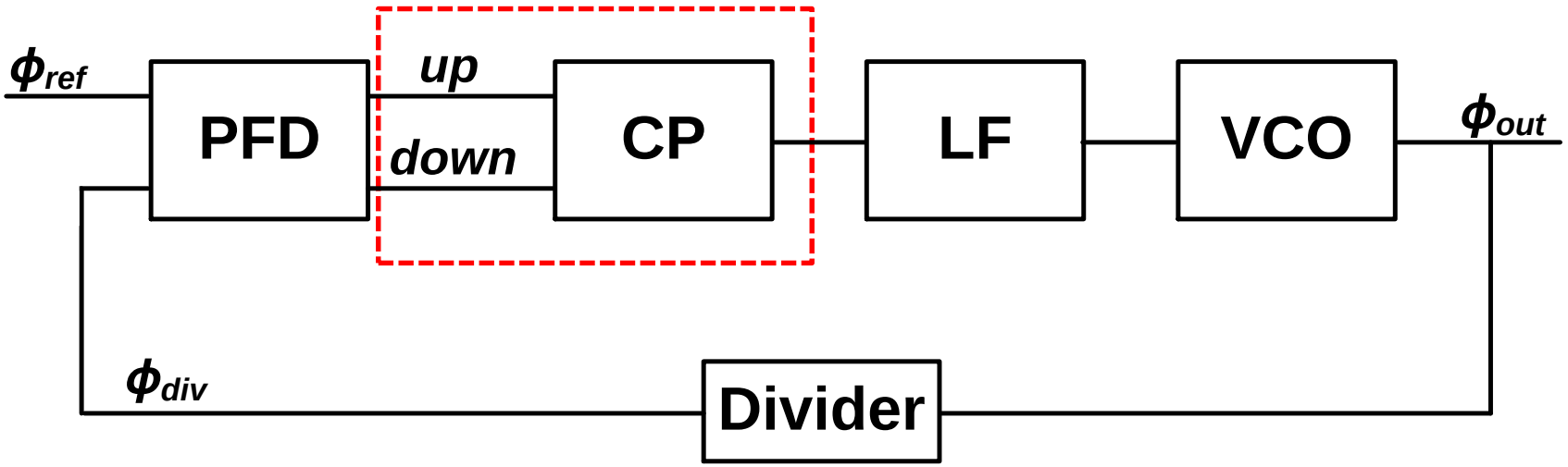
High-Speed Serial Interface Circuits and Systems

Design Exercise4 –

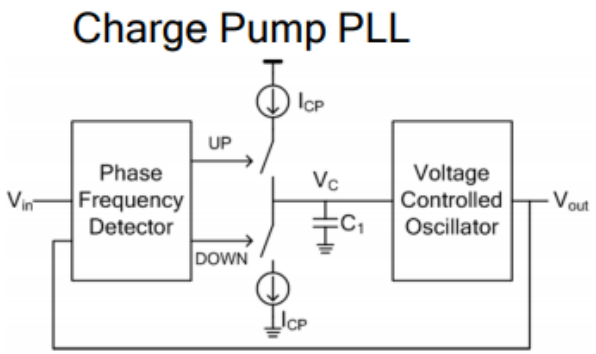
Charge Pump

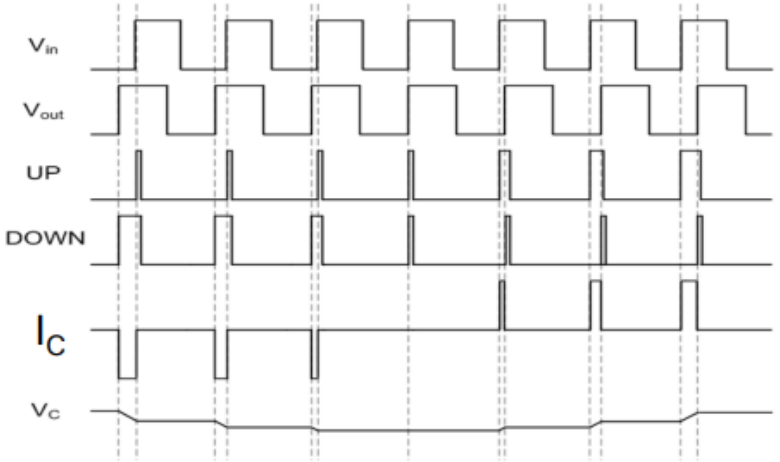
Charge Pump PLL



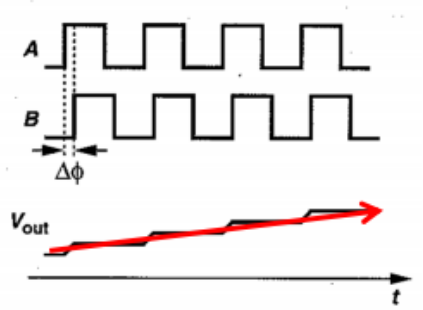
- Converts PFD phase error pulse (digital) to charge (analog).
- Charge is proportional to PFD pulse widths.
  - $Q_{cp} = I_{up} * t_{up} - I_{down} * t_{down}$
- Q_{cp} is filtered and integrated in low-pass filter.

Review of Charge Pump PLL





- Linear continuous-time model for charge-pump PLL?
- Charge pump operation is not continuous but discrete
- But make an approximation



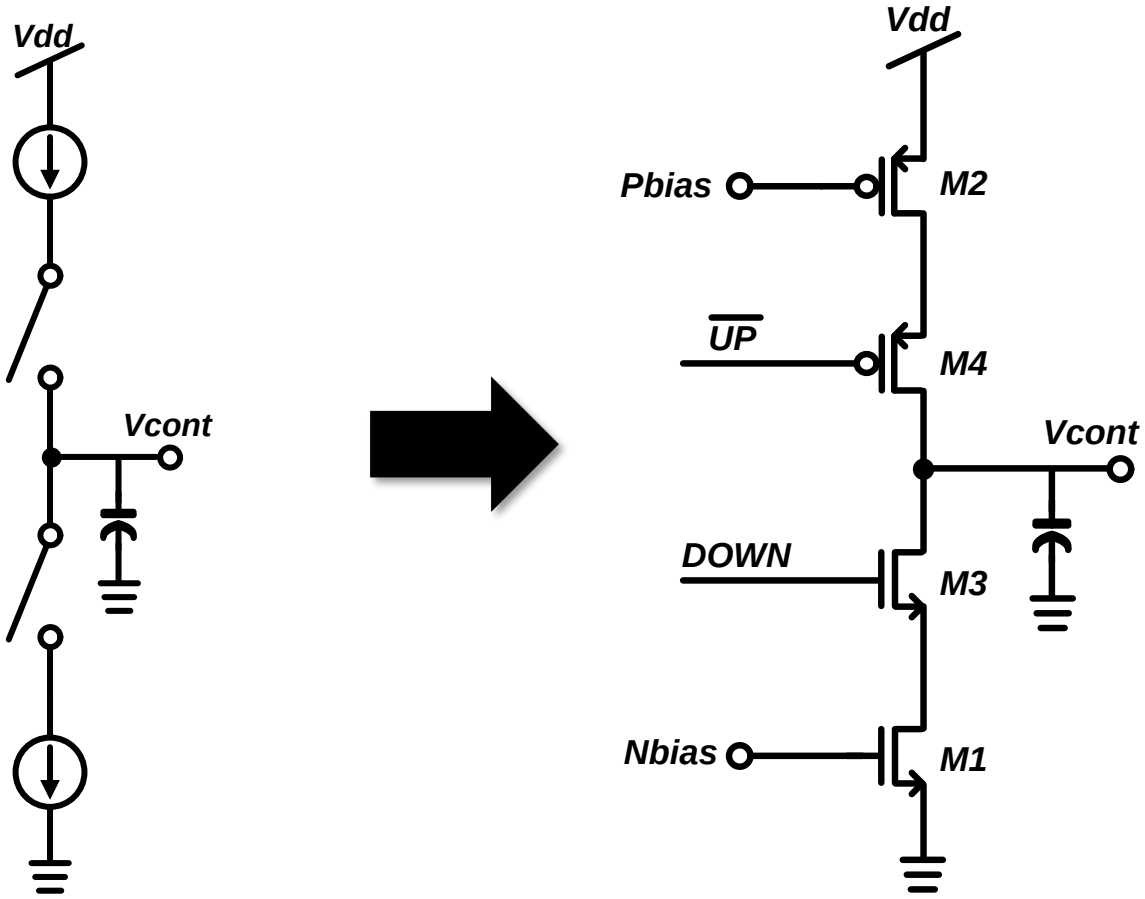
Transfer function for PFD + Charge Pump:

Max $\Delta\phi$: 2π ➔ $V_C(s)$: $I_{CP}\dfrac{1}{sC_1}$

For any $\Delta\phi$: $V_C(s) = \dfrac{\Delta\phi}{2\pi} I_{CP}\dfrac{1}{sC_1}$

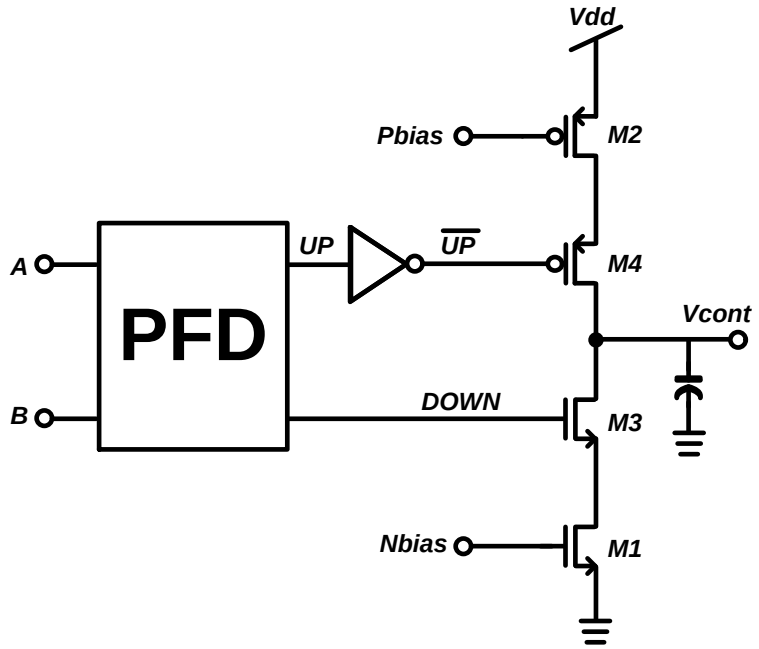
$$T(s) = \frac{V_C}{\Delta\phi}(s) = \frac{I_{CP}}{2\pi}\frac{1}{sC_1}$$

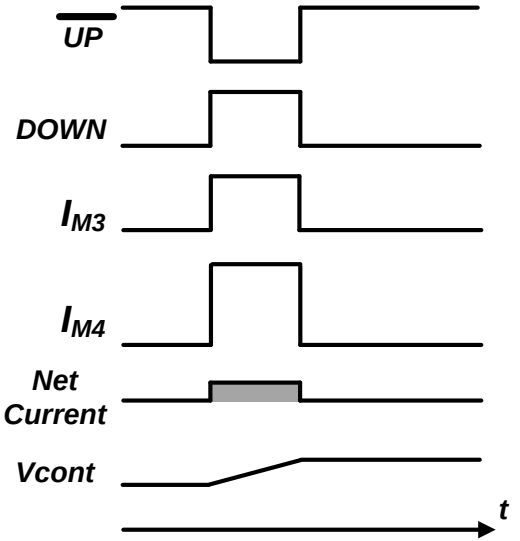
Basic Charge Pump



– Charge pump circuit consists of 2 current sources and 2 switches.

Current Mismatch



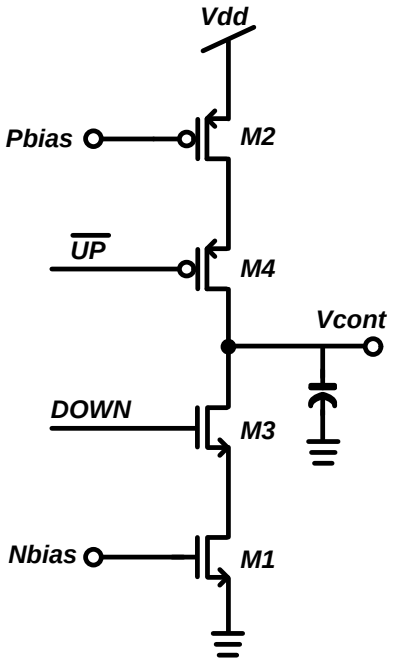


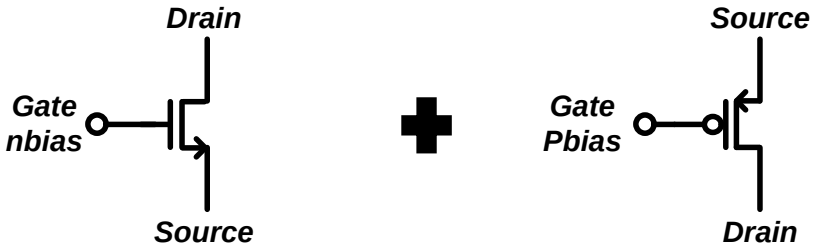
– Up & down current should be same.

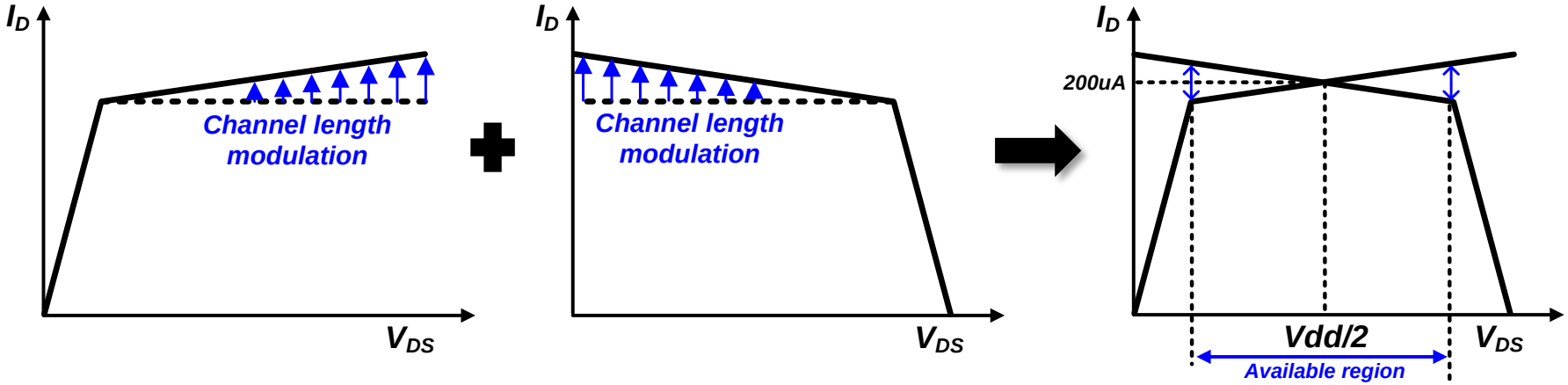
– Current mismatch results in static phase offset, which results in periodic ripple on the control voltage.

Current Mismatch

- Vcont is changed according to locking voltage.
- Current mismatch is caused by channel length modulation.
- Equal nmos and pmos current over entire Vcont range.
  - Reduce phase error.

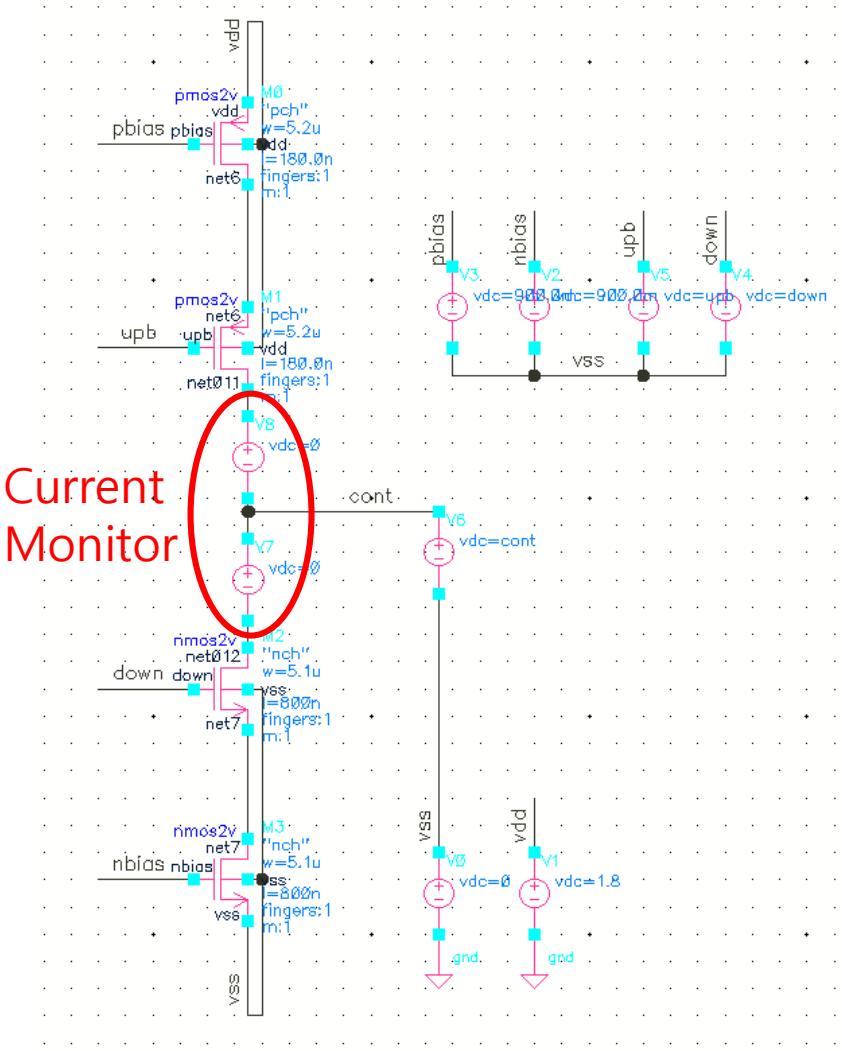






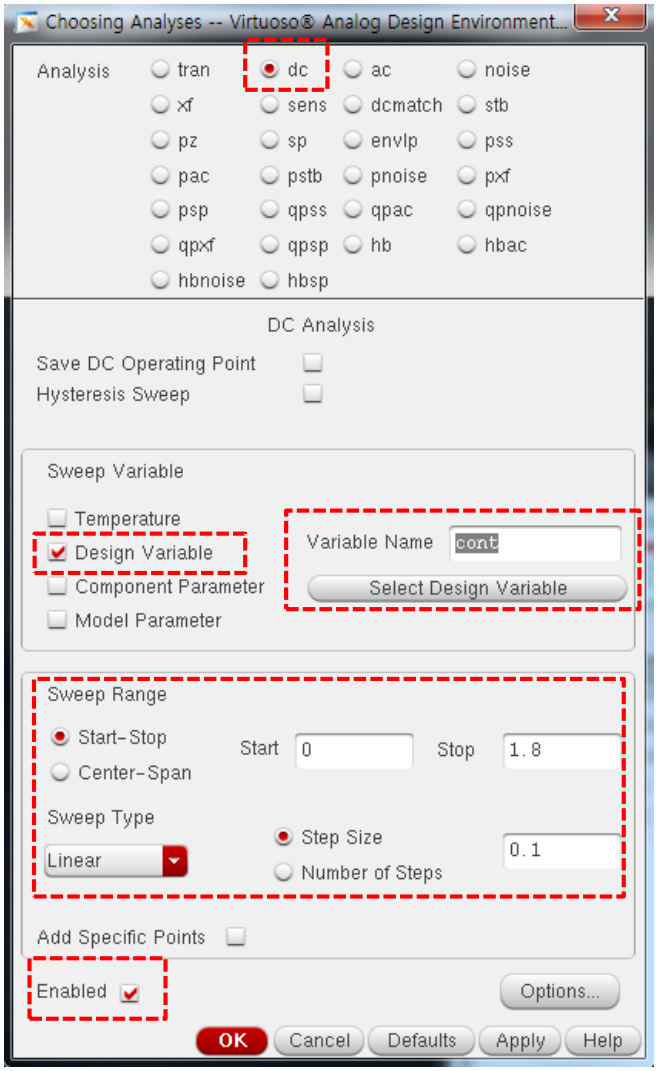
Basic CP Simulation

- PMOS size (2개 동일)
  - Length : 180 nm
  - Width : 5.2 um
- NMOS size (2개 동일)
  - Length : 800 nm
  - Width : 5.1 um
- Nbias
  - Voltage : 0.9 V
- Pbias
  - Voltage : 0.9 V
- Target charge pump current
  - Current : 200 uA



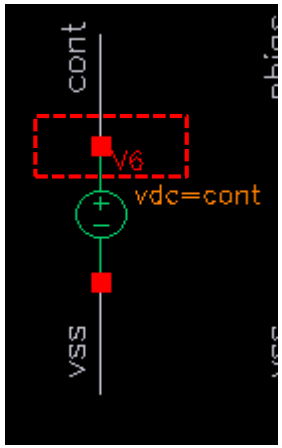
Simulation Condition

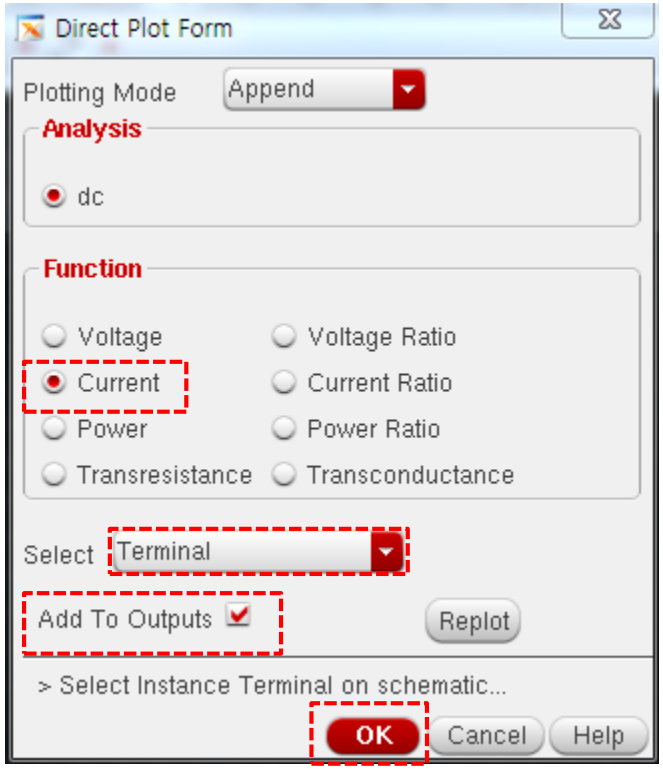
- Simulation condition setting
  - Choose analysis
  - Analysis : DC
  - Design variable : cont
  - Sweep range : 0 ~ 1.8
    - Sweep type : Linear
    - Step size : 0.1
  - Enabled check
  - OK



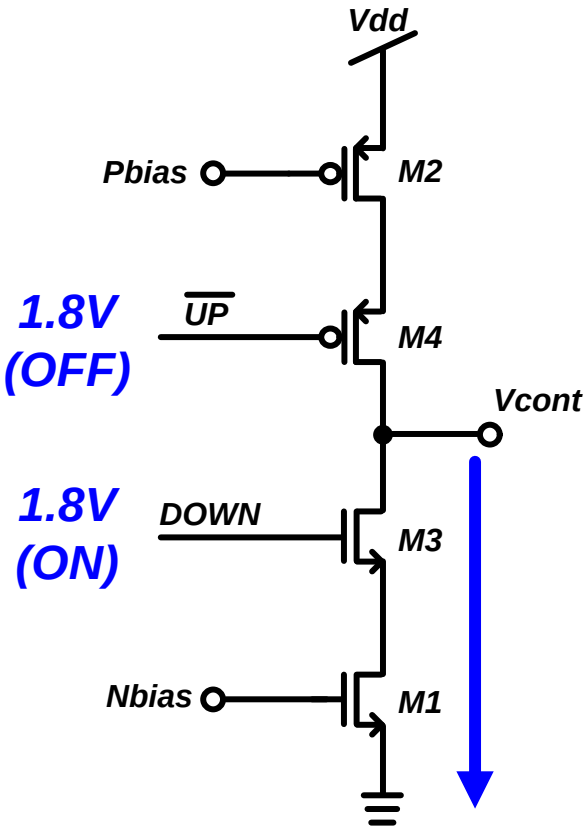
Simulation Results

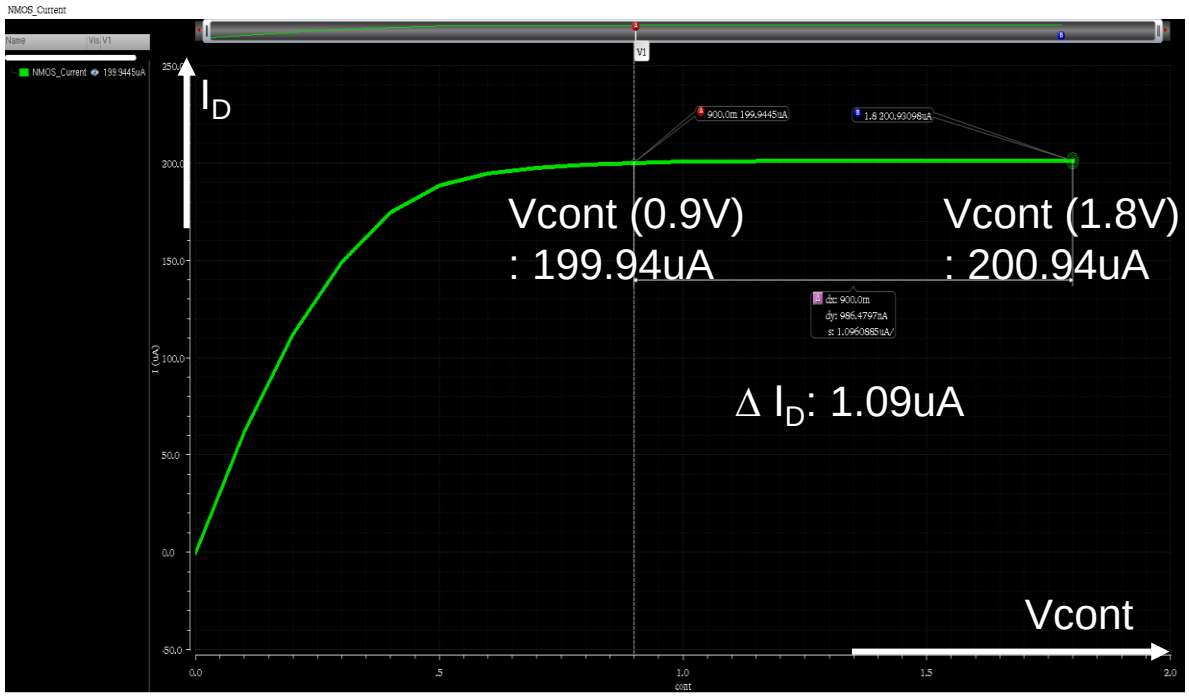
- Plot simulation results (Current)
  - Results → Direct Plot → Main Form
  - Function : current
  - Select : terminal
  - Add to outputs check
  - Schematic node choice
    - DC symbol (+) node click
  - OK



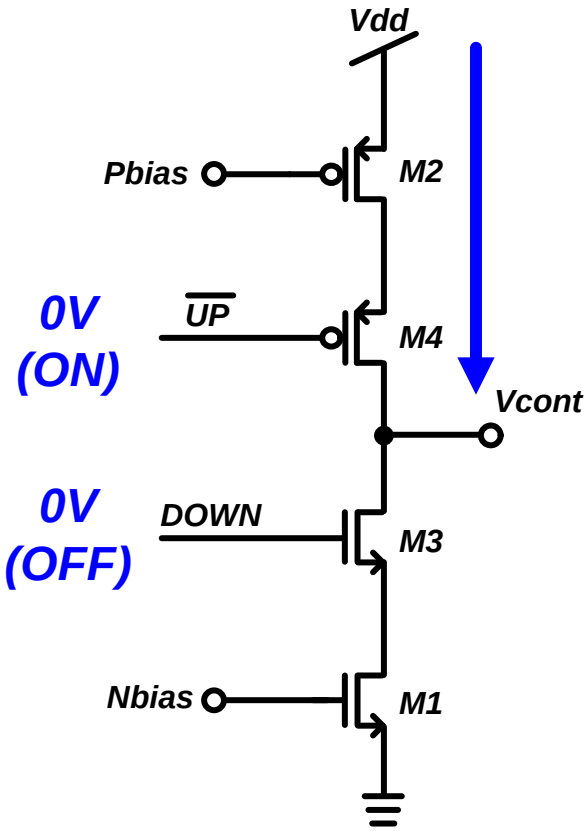


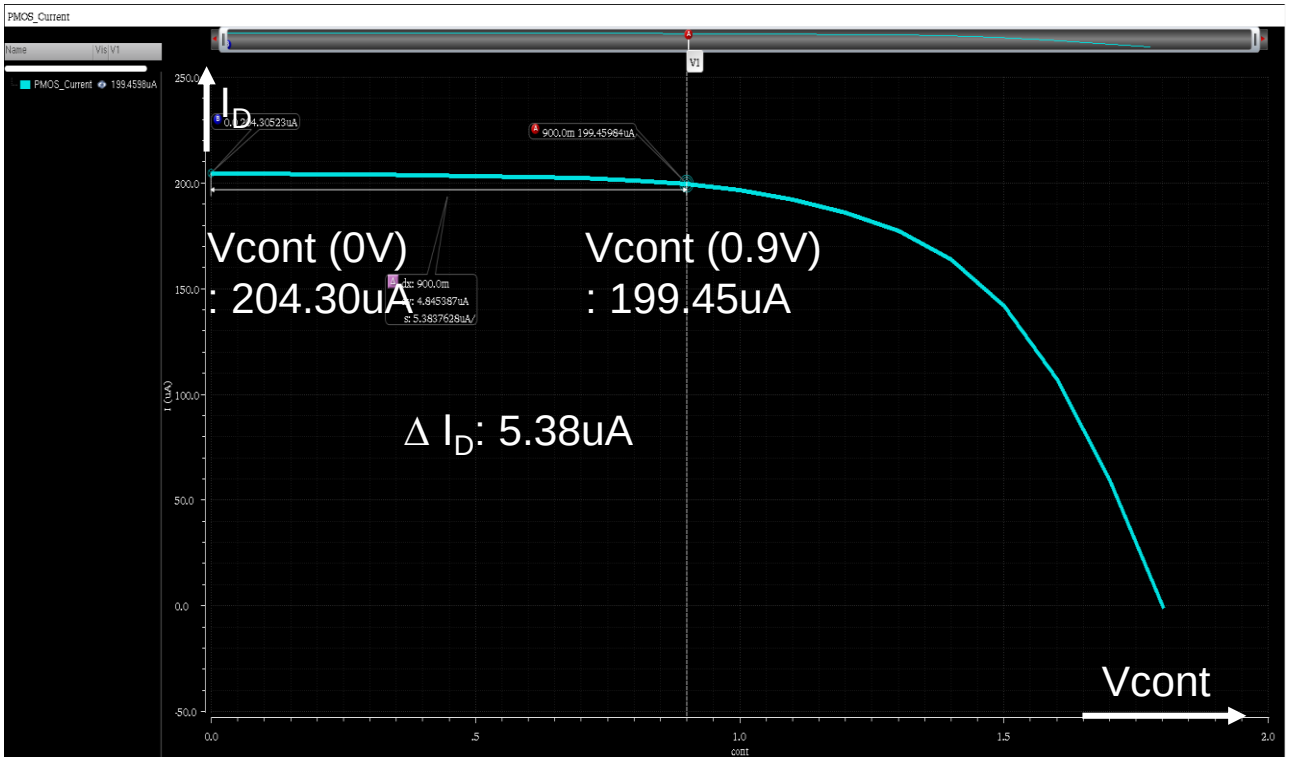
NMOS Current



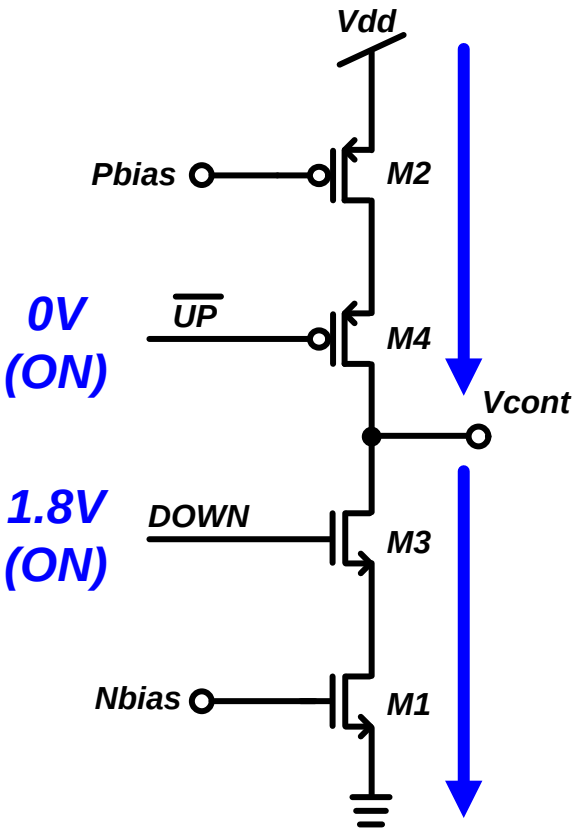


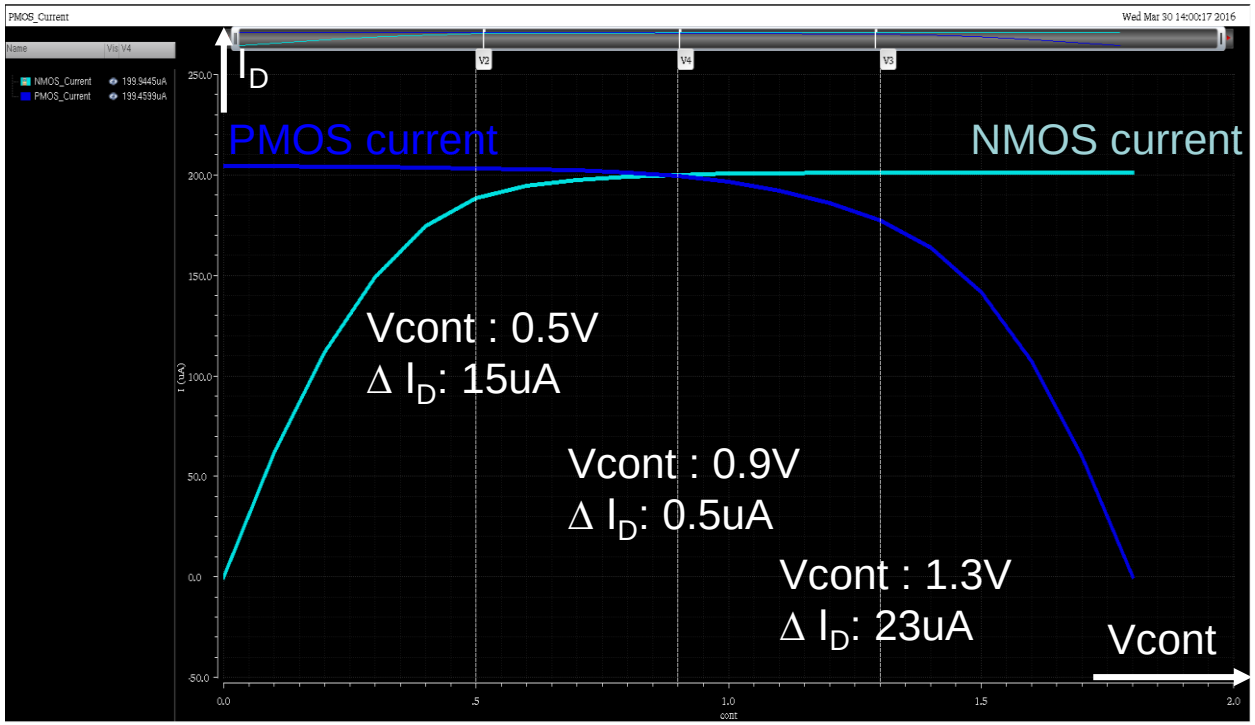
PMOS Current



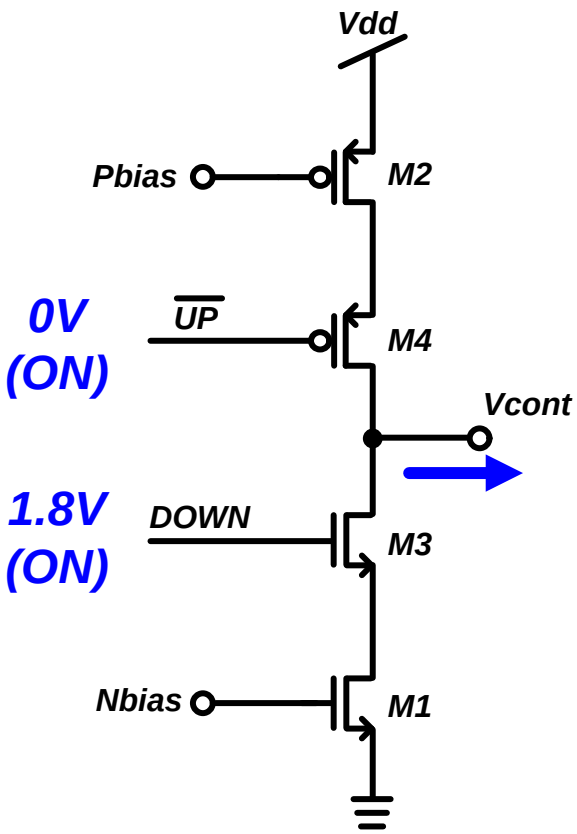


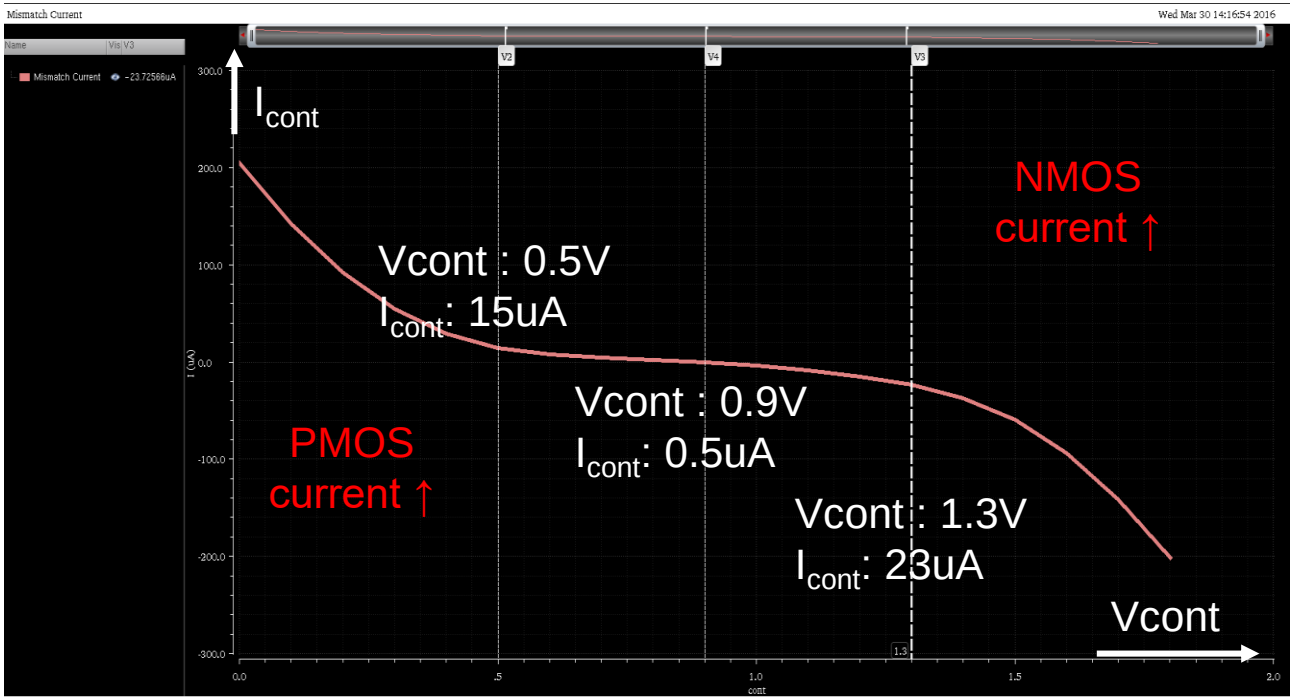
NMOS & PMOS Current



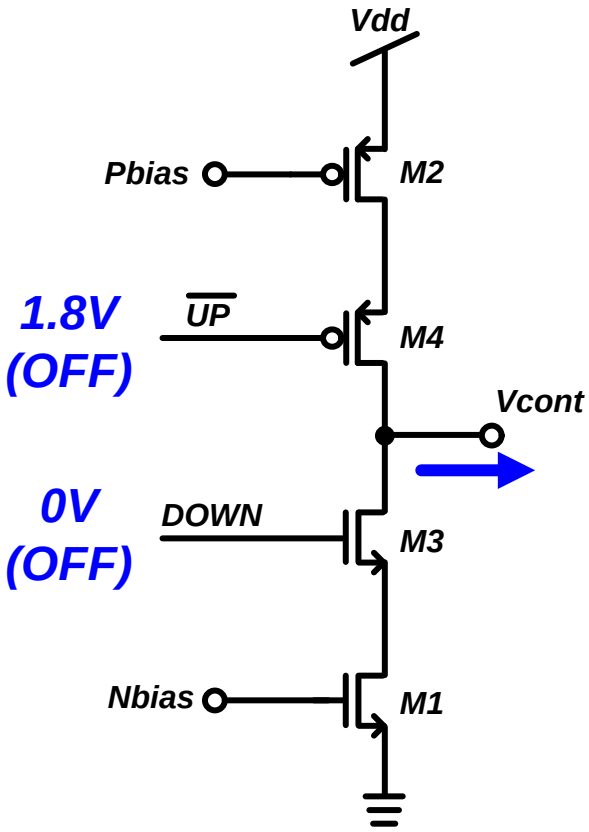


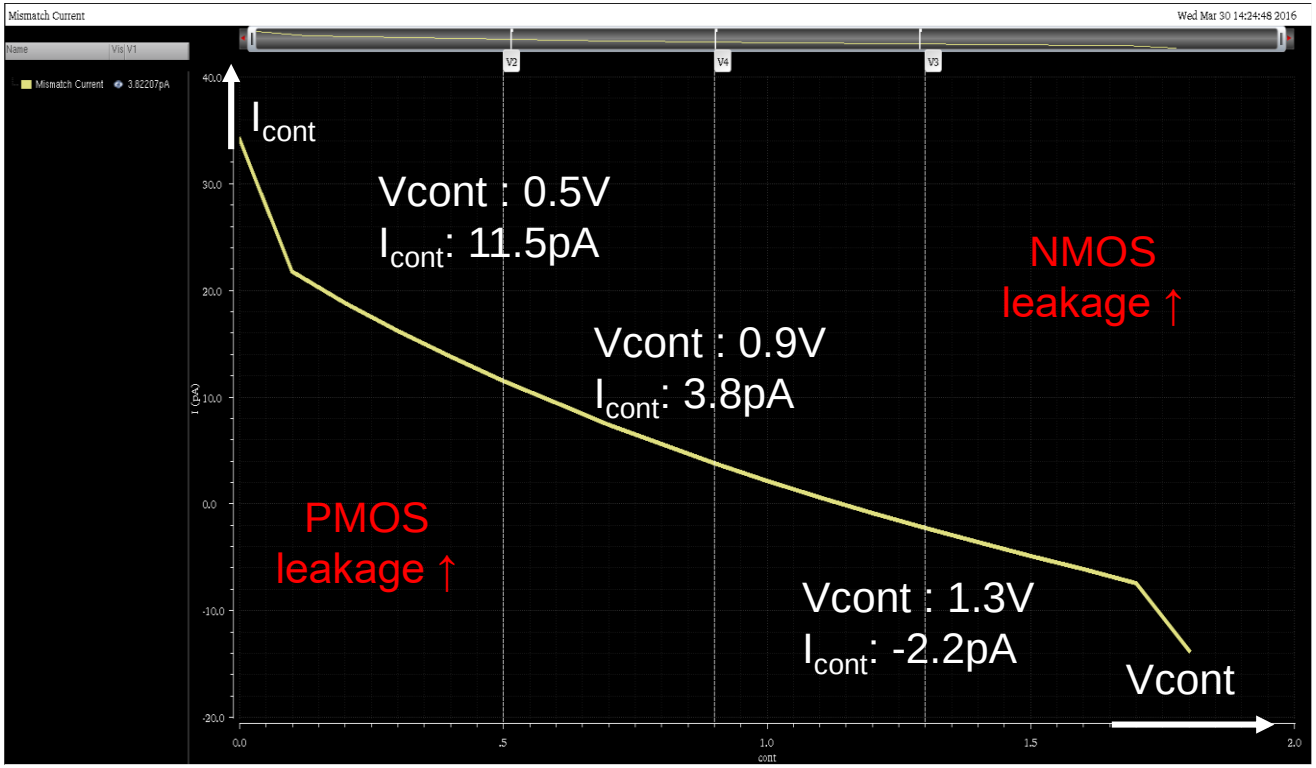
PMOS – NMOS Current



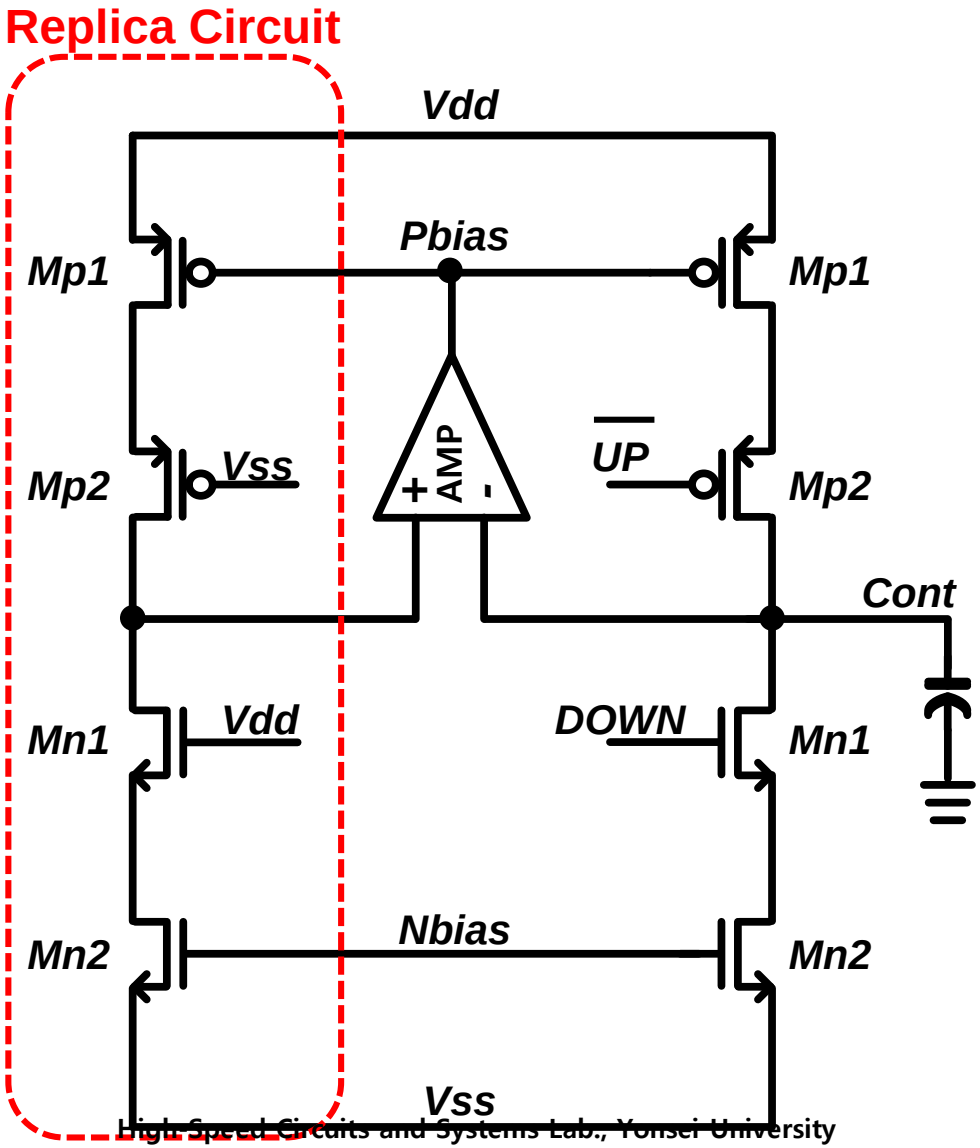


Leakage Current





Reducing Mismatch using Replica

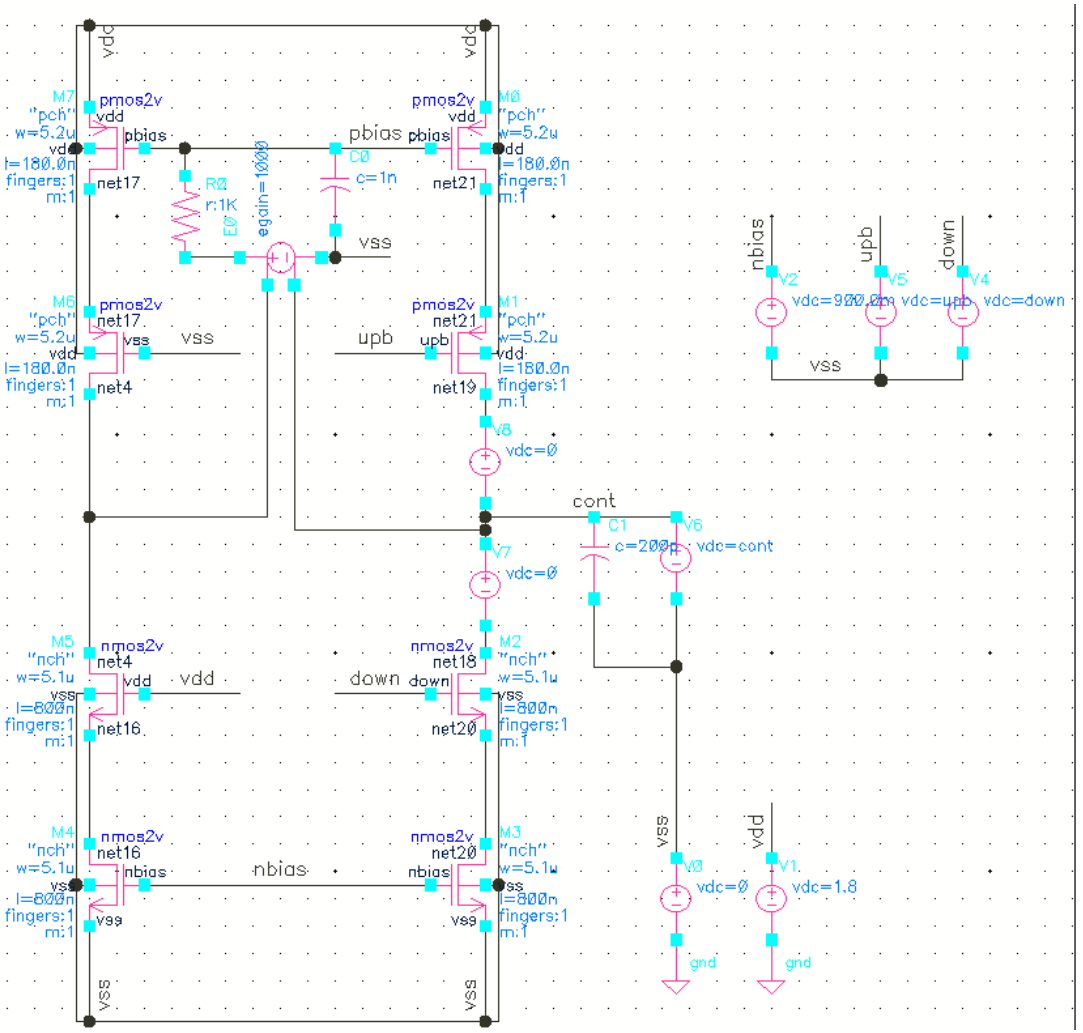


Design Example

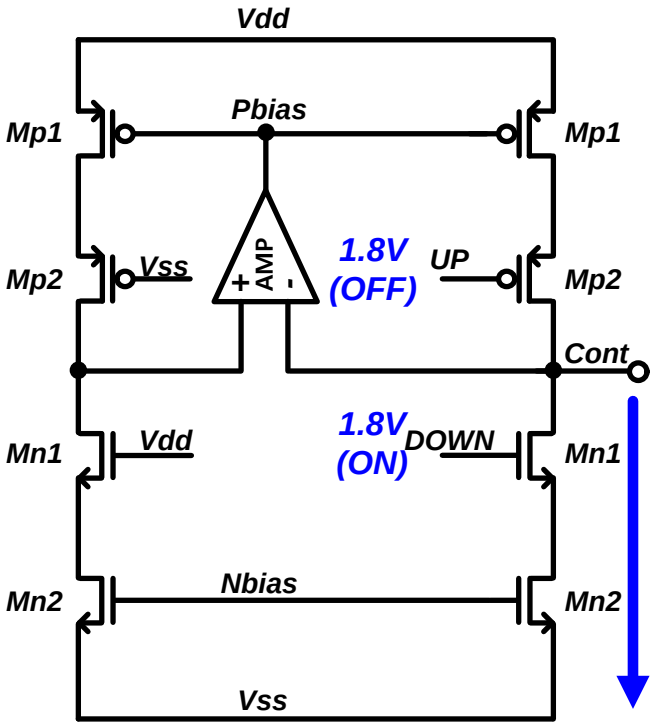
- ✓ Charge pump circuit
  - Supply voltage: 1.8V
  - Current of charge pump: 200uA ± 10uA
  - Current mismatch: <150nA with range of V_{cont} larger than 0.8V

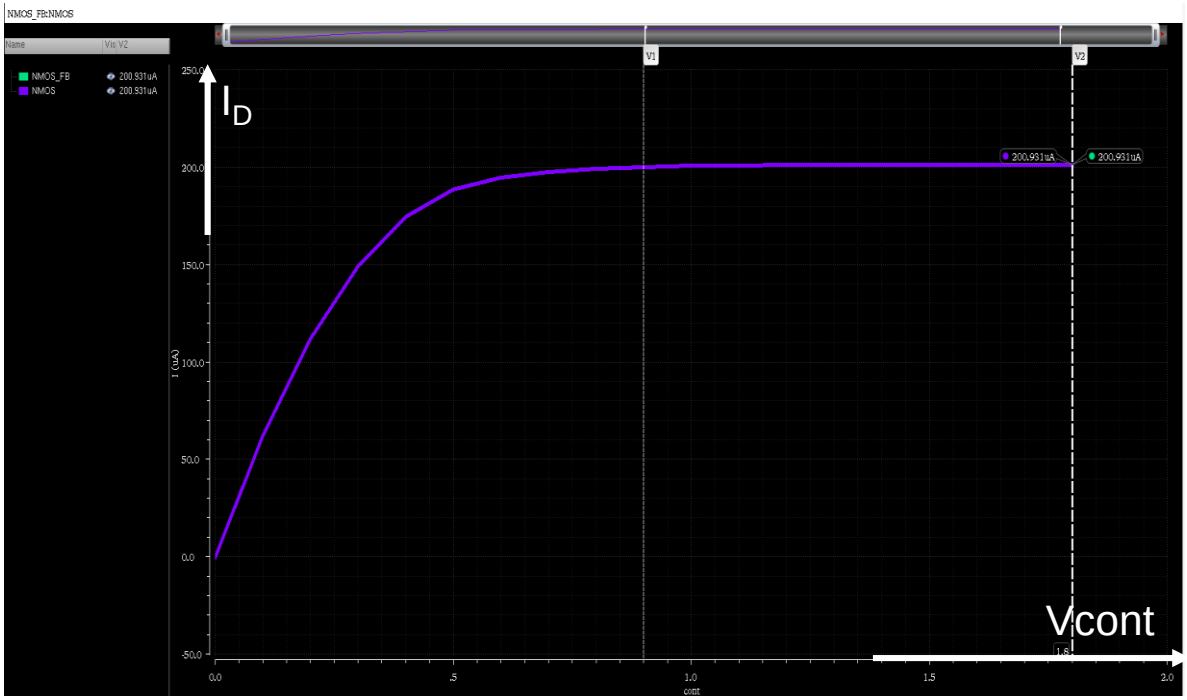
Simulation Schematic

- VCVS (OpAmp)
  - Voltage gain : 1000
  - Maximum output voltage :1.8V
  - Minimum output voltage : 0V
- RC Filter of OpAmp
  - Resistor : 1Kohm
  - Capacitance : 1nF
- Replica circuit
  - Charge pump size same
- Load
  - Capacitance : 200pF
- Nbias
  - Voltage : 0.9V

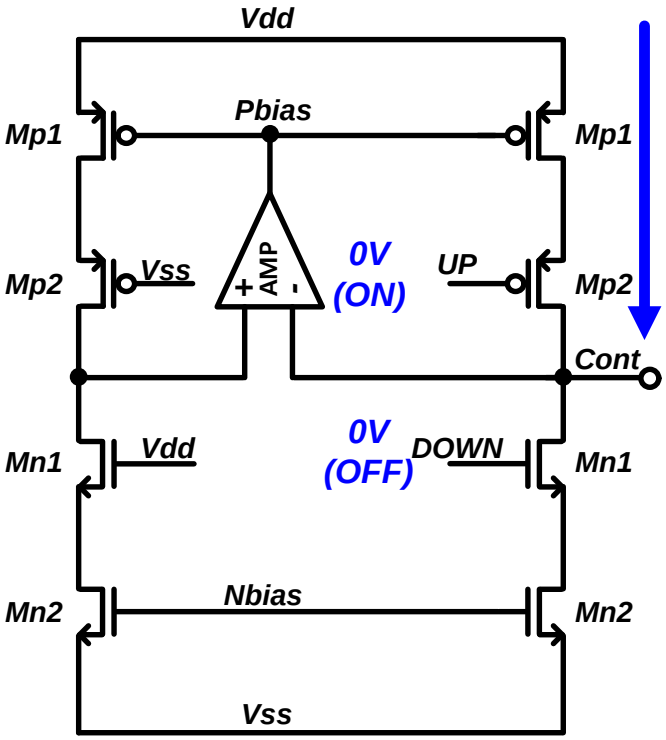


NMOS Current



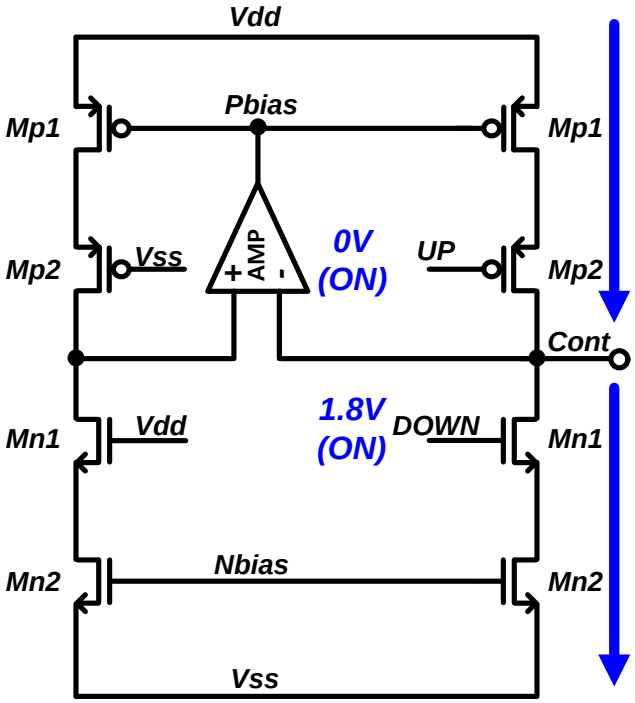


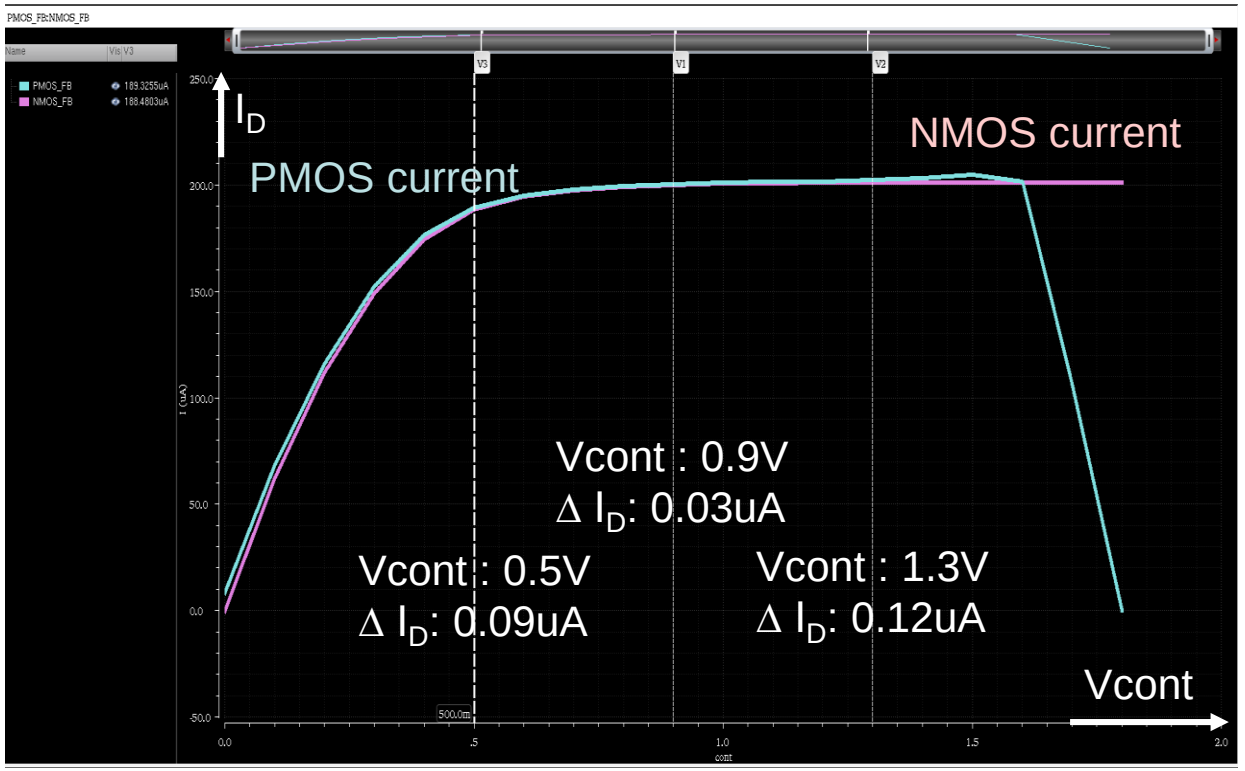
PMOS Current



– Change PMOS current though the feedback.

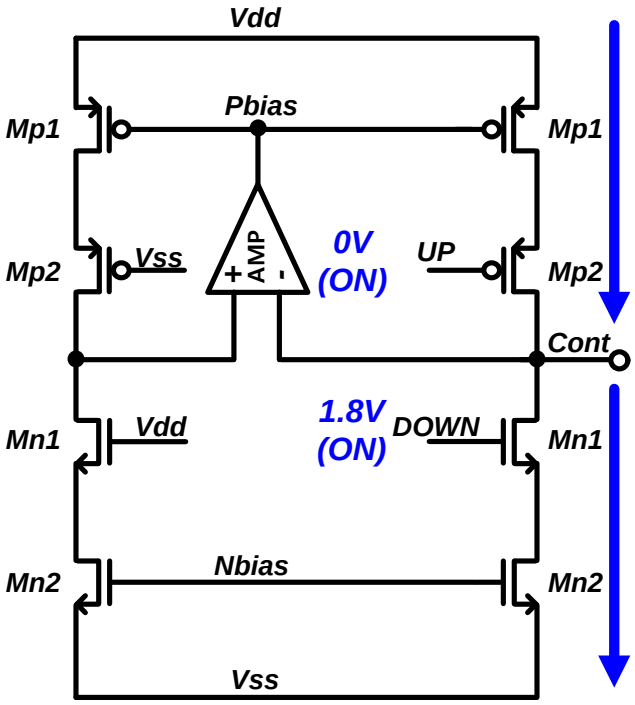
NMOS & PMOS Current

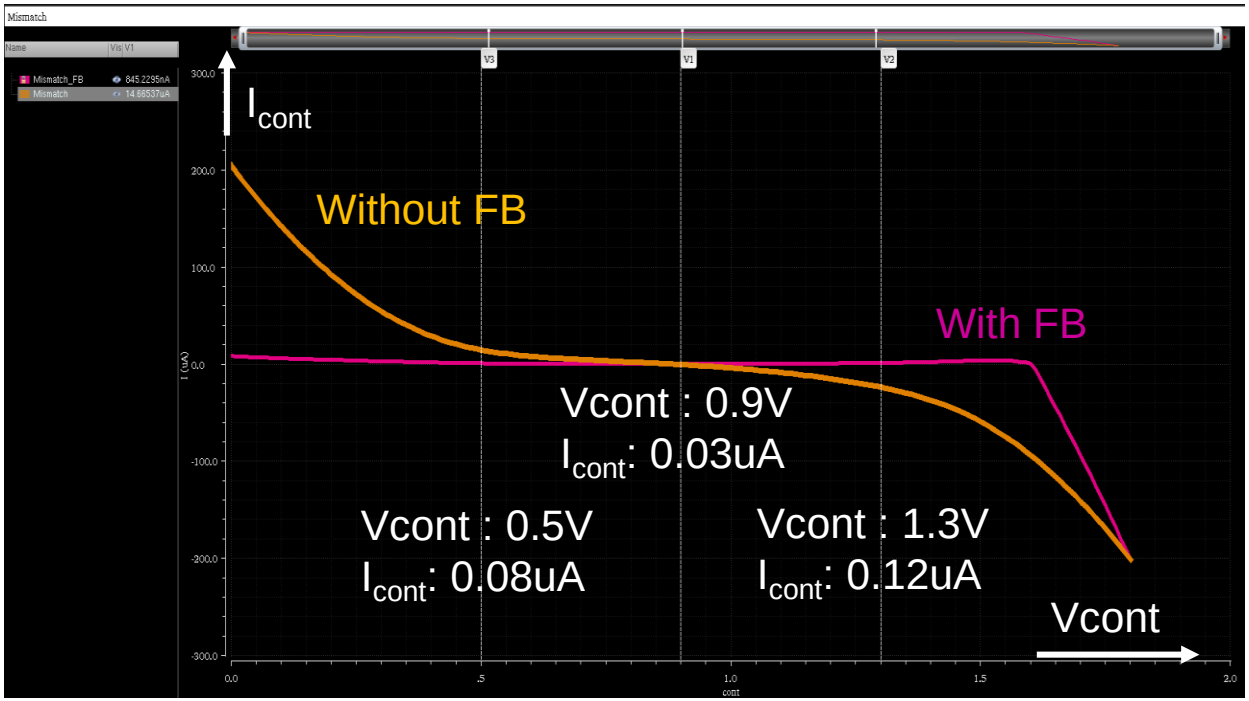




– NMOS and PMOS currents are equalized through the feedback system.

NMOS – PMOS Current





– NMOS and PMOS currents are equalized through the feedback system.

Homework

- ✓ Design 500uA (±20uA) charge pump with replica circuit.
- ✓ Without replica circuit, verify and plot pmos and nmos current waveforms with respect to cont voltage.
  - Current mismatch : less than 60uA (cont voltage range : 0.5V ~ 1.3V)
- ✓ With replica circuit, verify and plot pmos and nmos current waveforms with respect to cont voltage.
  - Current mismatch : less than 400nA (cont voltage range : 0.5V ~ 1.3V)
- ✓ Charge pump specification
  - VDD supply voltage : 1.8V
  - Nbias voltage : 0.9V
  - Charge pump current : 500uA (±20uA) at nbias voltage 0.9V
- ✓ Due: Next design class (Hardcopy)