High-Speed Serial Interface Circuits and Systems

Design Exercise 7 –

Continuous-Time Linear Equalizer (CTLE)

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Continuous-Time Linear Equalizer(CTLE)



<Frequency response flattening>



<Integrated power spectrum of NRZ data>

- Until what frequency..??
 - Nyquist frequency:
 In order to recover data,
 it is necessary to have bandwidth <u>at least half of data rate</u>
 ex) 2Gbps → 1GHz bandwidth required

Channel Characteristic

mtline (microstrip)

- -Dielectric const.: 4.8
- -Dielectric layer thickness: 360u (m)
- -Signal line width: 625u (m)
- -Signal line thickness: 17.78u (m)
- -Physical length: 8 (m)





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Source-Degenerated CTLE



- Goal: Boost 9.5dB @ 1GHz
 Equalize 2Gbps data transmission
- 2 pole, 1 zero change with R,C tuning
- Find R,C where 1st pole has 1GHz and peaking has 9.5dB by hand calculation

CTLE AC Simulation



Input source

-vcvs gain: ±0.5 -V_{CM}: 1.55V -Input resistor: 50 Ohm -Vsin: 1V ac magnitude

CTLE

-Input MOSFETs: 30u/180n

- -Tail MOSFETs: 50u/800n
- -Load resistors: 1K Ohm
- -Load capacitor: 50f F

-R_{deg}: 1.3K Ohm -C_{deg}: 350f F -Tail MOSFET bias: 0.6 V

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Simulation Results



- 1M~10G, logarithmic, 101points
- DC attenuation: -0.45dB
- 7.3dB peaking @ Nyquist frequency
- Slight difference with calculation

Channel + CTLE AC Simulation



Channel(mtline)

-Differential termination(100 Ohm termination)

- -Dielectric const.: 4.8
- -Dielectric layer thickness: 360u (m)
- -Signal line width: 625u (m)
- -Signal line thickness: 17.78u (m)
- -Physical length: 8 (m)

Simulation Results(Channel)



- -6dB DC gain loss due to termination
- -9.5dB loss @ 1GHz due to channel loss

Simulation Results(Channel + CTLE)

- Gain equalization by CTLE

Channel + CTLE Transient Simulation

🔀 Choosing A	nalyses Vir	tuoso® A	nalog Design	Environment (14)	x
Analysis	🖲 tran	🔾 dc	🔾 ac	🔾 noise	
	⊖ ×f	🔾 sens	🔾 dcmatch	🔾 stb	
	🔾 pz	🔾 sp	🔾 envlp	🔾 pss	
	🔾 pac	🔾 pstb	🔾 pnoise	🔾 pxf	
	🔾 psp	🔾 qpss	🔾 qpac	🔾 qpnoise	
	🔾 qpxf	🔾 qpsp	🔾 hb	🔾 hbac	
	🔾 hbnoise	🔾 hbsp			
	Т	ransient A	Analysis		
Stop Time	1u				
Accuracy I	Defaults (errp	ireset)			
🗹 conser	rvative 📃 m	oderate (liberal		
Transien	t Noise				
Dynamic	: Parameter				
Enabled 🕑				Options	
		ок с	ancel Defi	aults Apply	Help

Random bit stream

```
-Period: 1/2Gbps = 500ps
-seed: 1
-vlogic_high, low = 1, -1 → 500mV swing to Rx
-trise, tfall = 20p
```

Simulation Results(Channel)

Sig	qnal/Expr Names	
outp		
Start/Stop 0.1u	1.000	Ju
Period 1n		
- 📃 Edge Triggered	l Eye Diagram —	
Signal		
Threshold 0	Offset 0	
CrossType rising		•
Plot Mode	New Windo	w 🔽
Latensity		* F**2
Advanced Optio	ns	
Select Eye eye_out	p	
Threshold 1.55		
Level 0		
x-range 30	50	%
y-range 0	50	%
Level 1		
	50	%
x-range 30		
x-range 30 y-range 50	100	%
x-range 30 y-range 50 Bins 10	100 Sampling Interval	× •

Closed eye due to channel lossSmall

.5 time (ns

.25

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1.0

Simulation Results(Channel + CTLE)

Loss compensation by CTLEHigher SNR(15.8)

Homework

Rx CTLE

Design source-degenerate CTLE which provides larger SNR than 17 for the same channel using the same random bit stream shown in the class. For the SNR determination, simulate the eye for 1us.