High-Speed Serial Interface Circuits and Systems

Design Exercise 7 –

Continuous-Time Linear Equalizer (CTLE)

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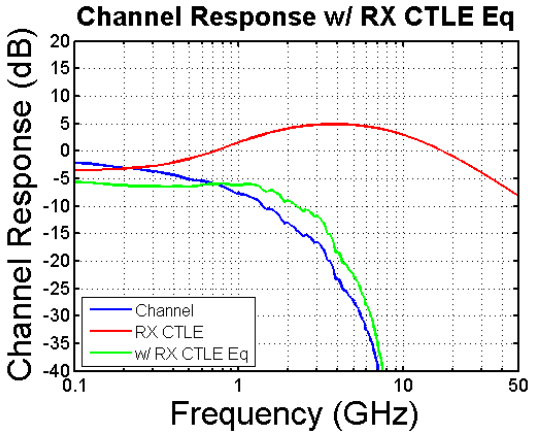
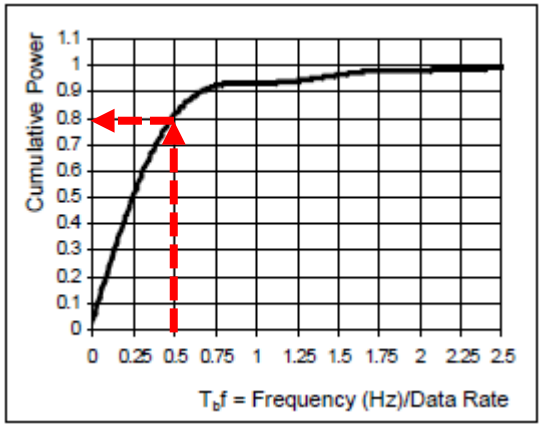


<Frequency response flattening>

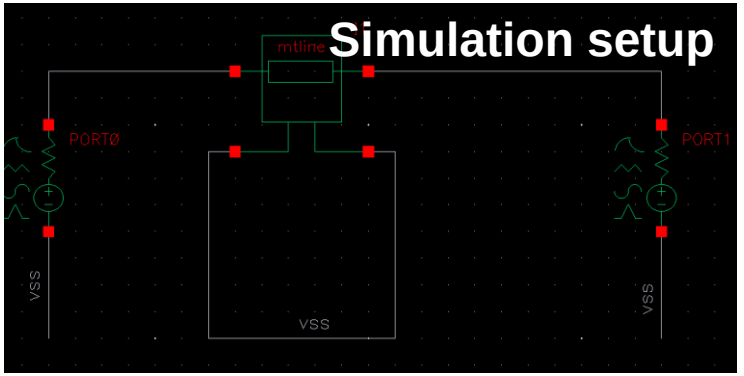


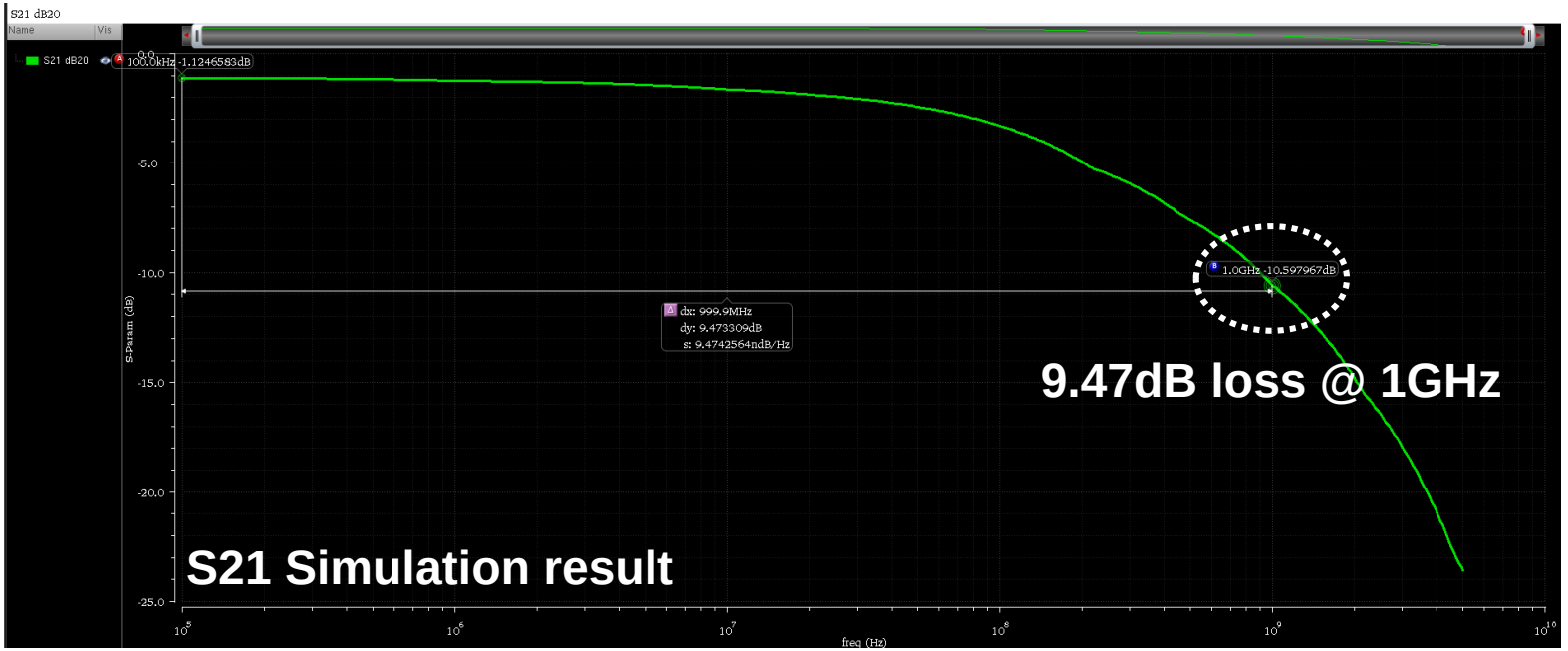
<Integrated power spectrum of NRZ data>

- Until what frequency..??
  - Nyquist frequency:
    In order to recover data,
    it is necessary to have bandwidth *at least half of data rate*
    ex) 2Gbps ➔ 1GHz bandwidth required

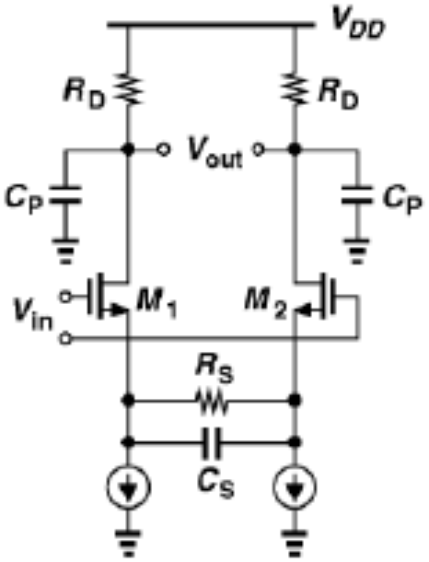
Channel Characteristic

- mtline (microstrip)
  -Dielectric const.: 4.8
  -Dielectric layer thickness: 360u (m)
  -Signal line width: 625u (m)
  -Signal line thickness: 17.78u (m)
  -Physical length: 8 (m)





Source-Degenerated CTLE

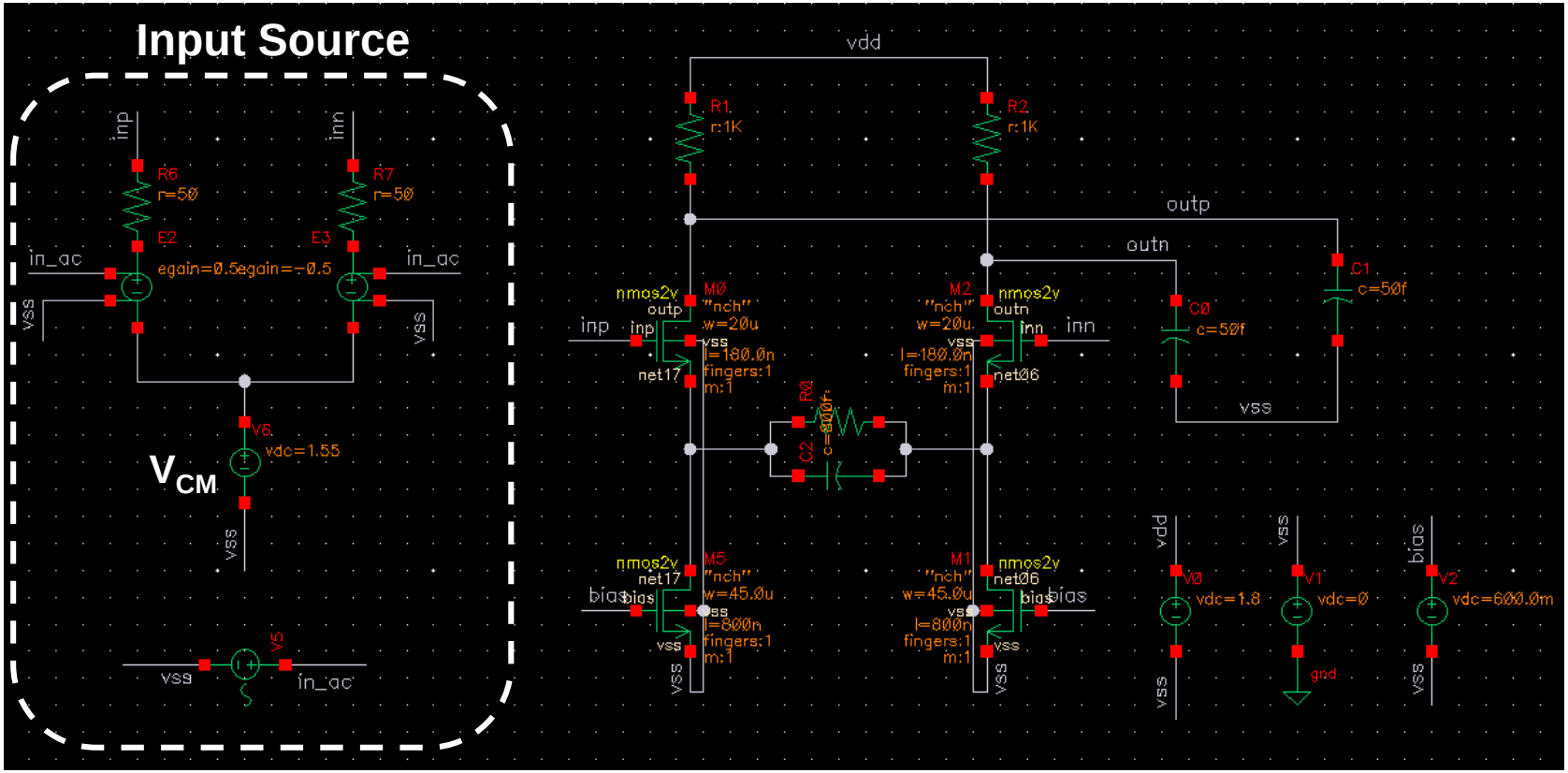


$$H(s) = \frac{g_m}{C_p} \frac{s + \frac{1}{R_S C_s}}{(s + \frac{1 + \frac{g_m R_S}{2}}{R_S C_s})(s + \frac{1}{R_D C_p})}$$

$$\text{Peaking} = 1 + \frac{g_m R_S}{2}$$

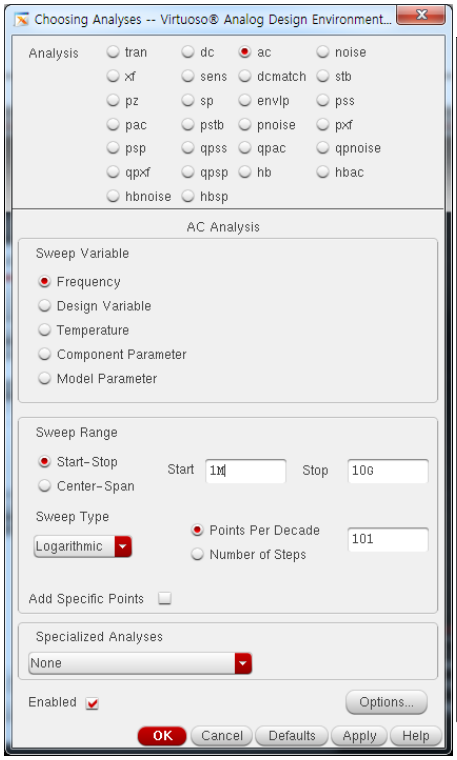
- Goal: Boost 9.5dB @ 1GHz
  ➔Equalize 2Gbps data transmission
- 2 pole, 1 zero change with R,C tuning
- Find R,C where 1st pole has 1GHz and peaking has 9.5dB by hand calculation

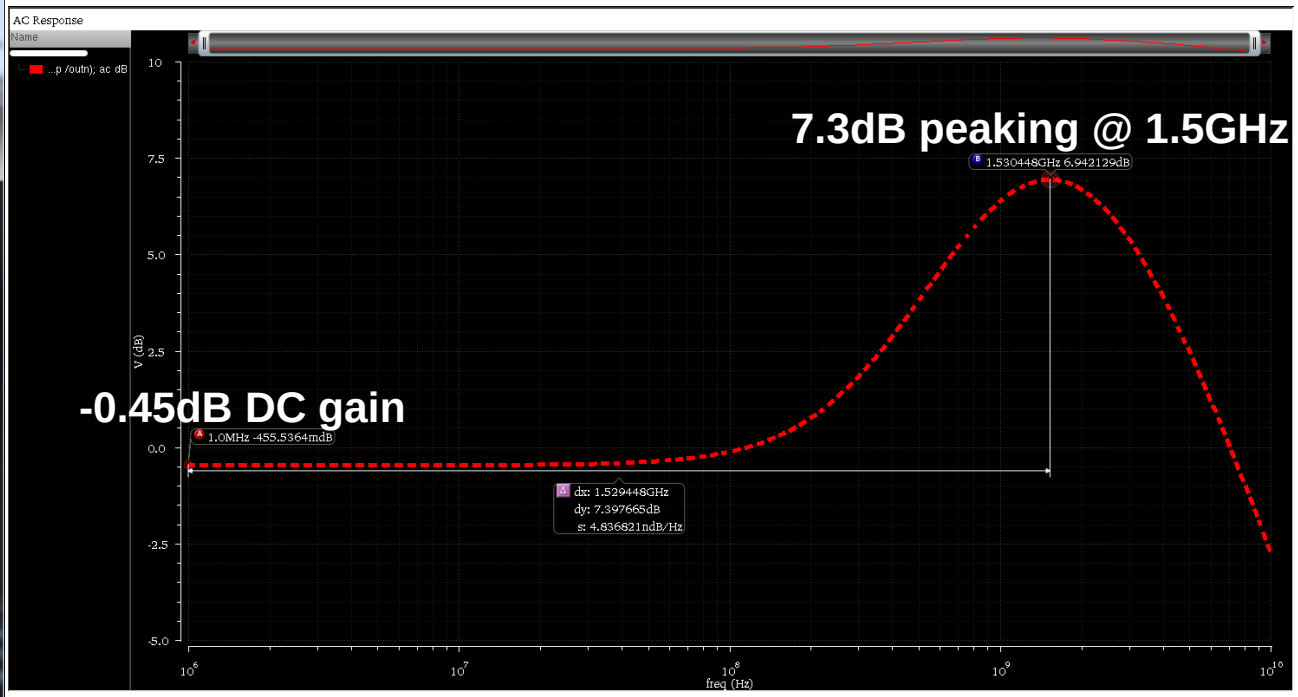
CTLE AC Simulation



- Input source
  - -vcvs gain: ±0.5
  - -V_{CM} : 1.55V
  - -Input resistor: 50 Ohm
  - -Vsin: 1V ac magnitude
- CTLE
  - -Input MOSFETs: 30u/180n
  - -Tail MOSFETs: 50u/800n
  - -Load resistors: 1K Ohm
  - -Load capacitor: 50f F
  - -R_{deg}: 1.3K Ohm
  - -C_{deg}: 350f F
  - -Tail MOSFET bias: 0.6 V

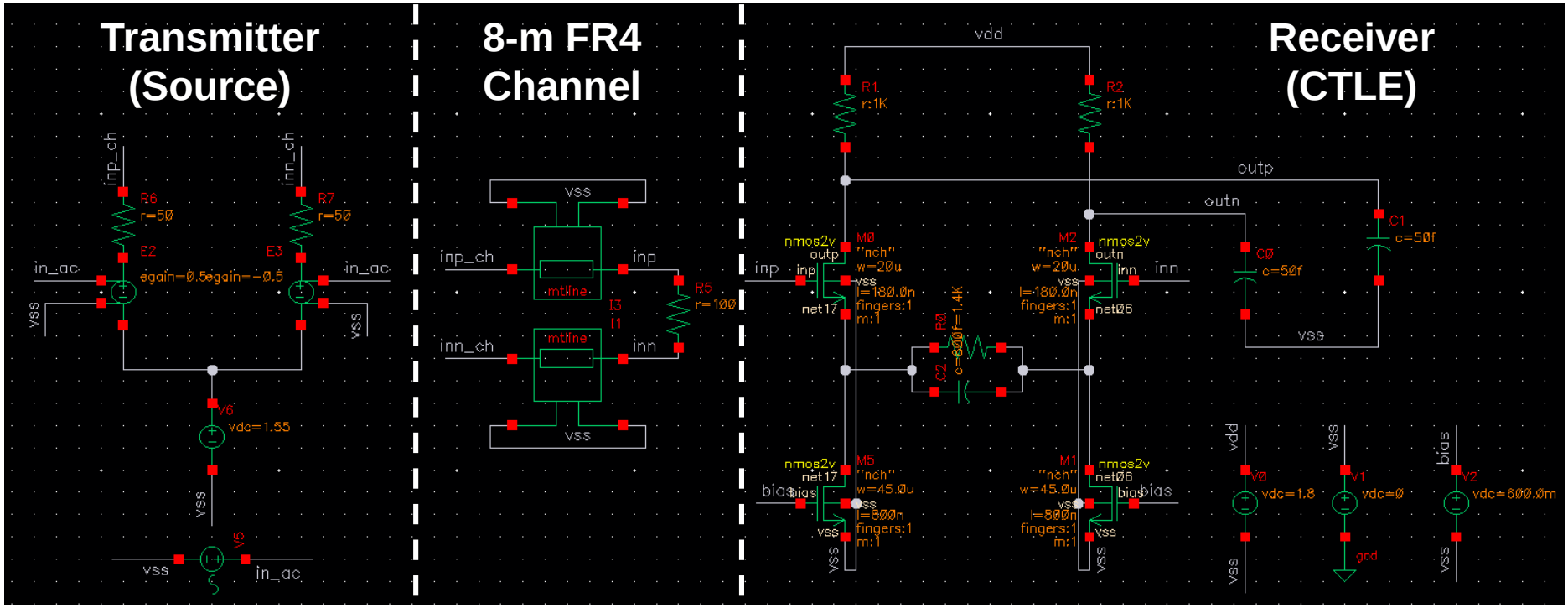
Simulation Results





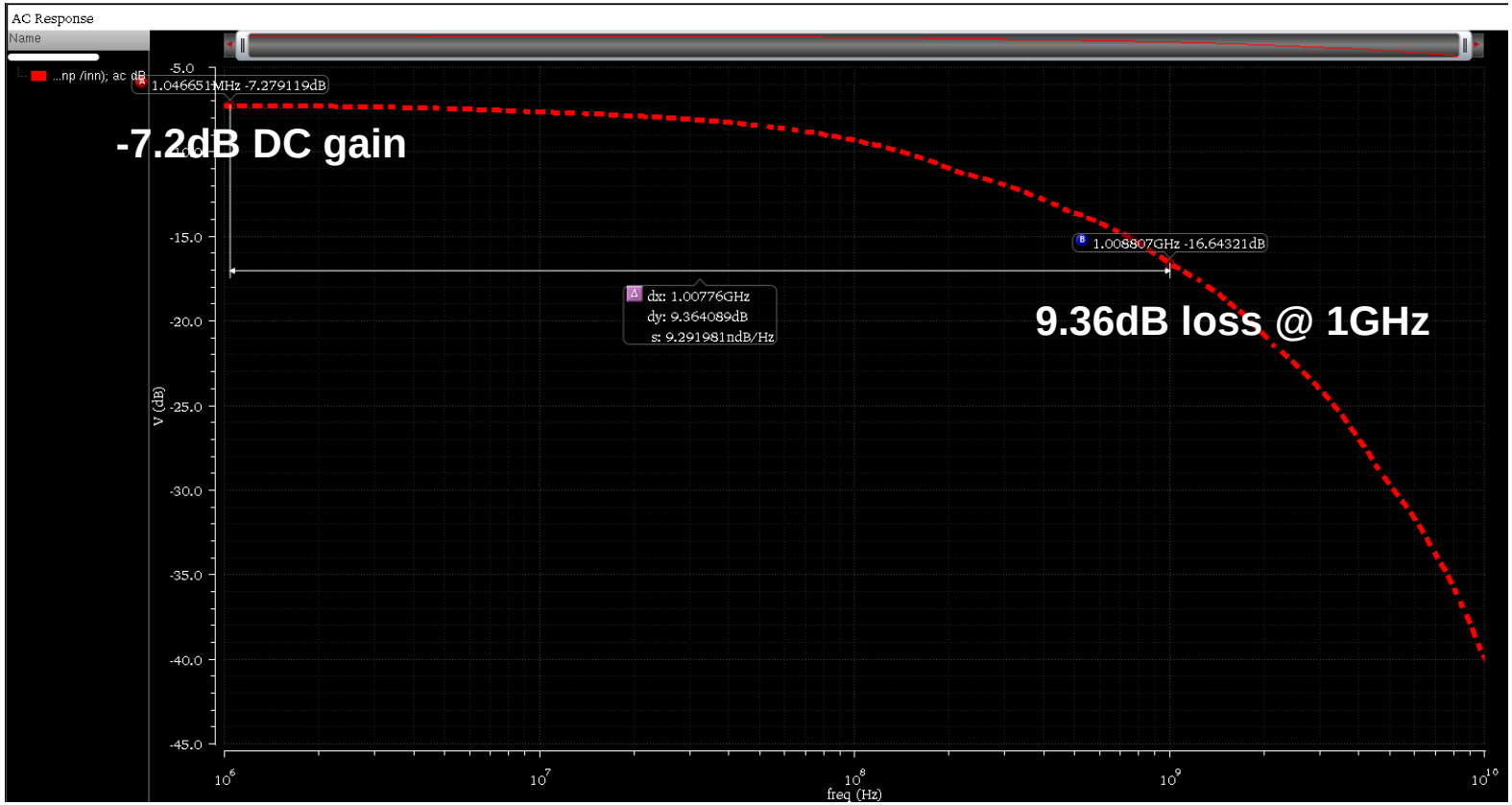
- 1M~10G, logarithmic, 101points
- DC attenuation: -0.45dB
- 7.3dB peaking @ Nyquist frequency
- Slight difference with calculation

Channel + CTLE AC Simulation



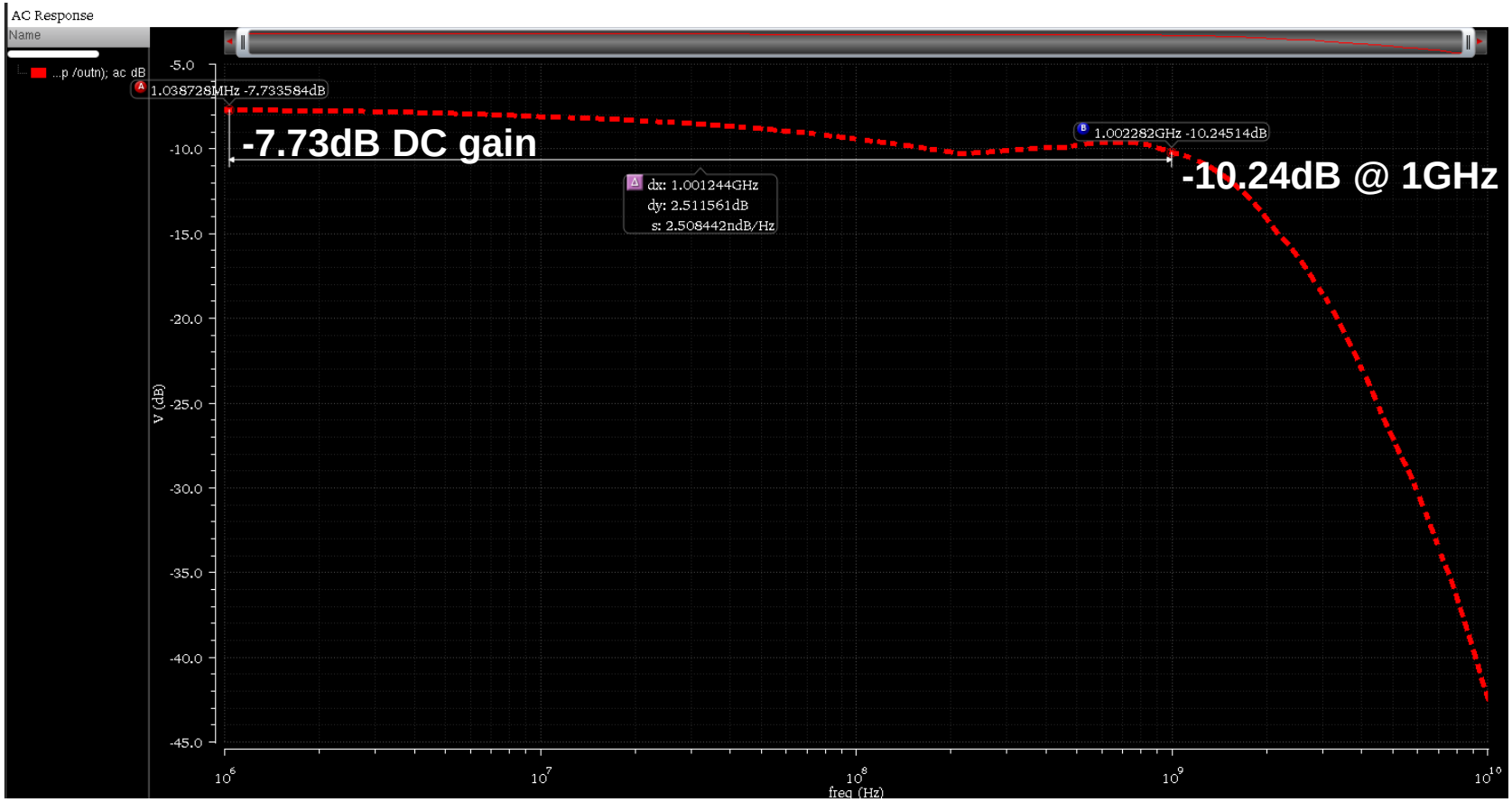
- Channel(mtline)
  - -Differential termination(100 Ohm termination)
  - -Dielectric const.: 4.8
  - -Dielectric layer thickness: 360u (m)
  - -Signal line width: 625u (m)
  - -Signal line thickness: 17.78u (m)
  - -Physical length: 8 (m)

Simulation Results(Channel)



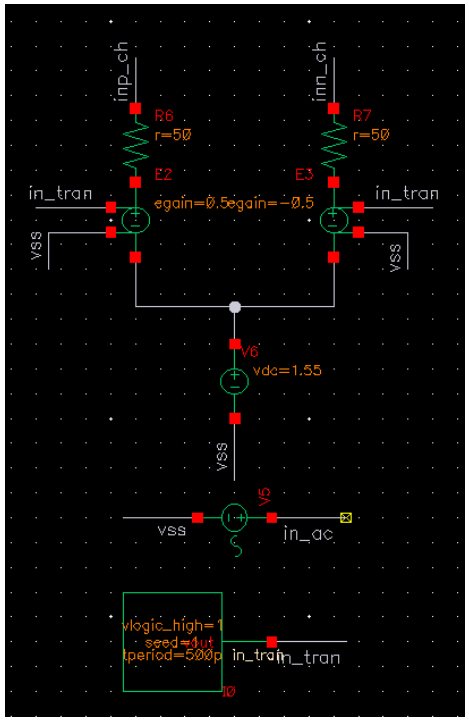
- -6dB DC gain loss due to termination
- -9.5dB loss @ 1GHz due to channel loss

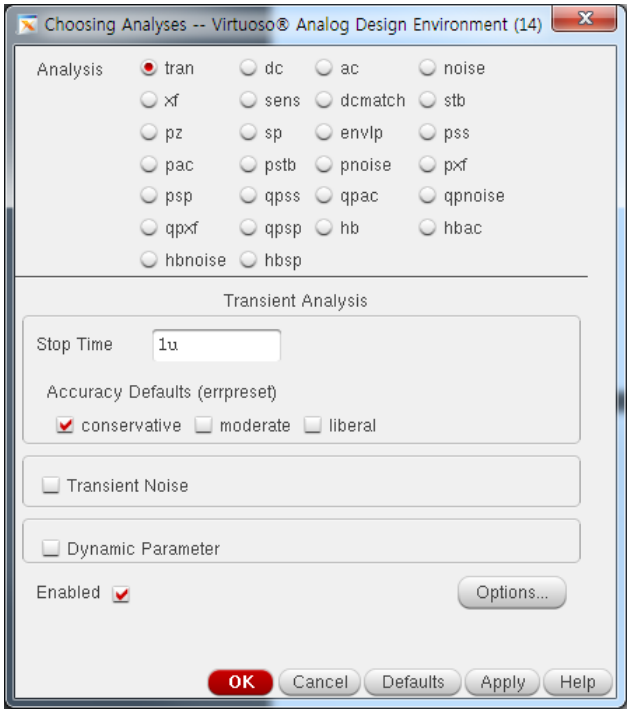
Simulation Results(Channel + CTLE)



- Gain equalization by CTLE
- Response fluctuation ➔ Channel non-ideality

Channel + CTLE Transient Simulation





- Random bit stream

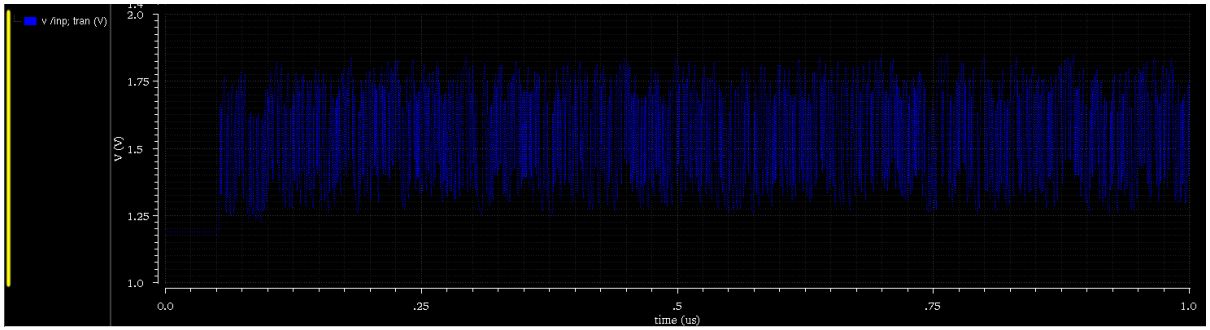
  -Period: 1/2Gbps = 500ps

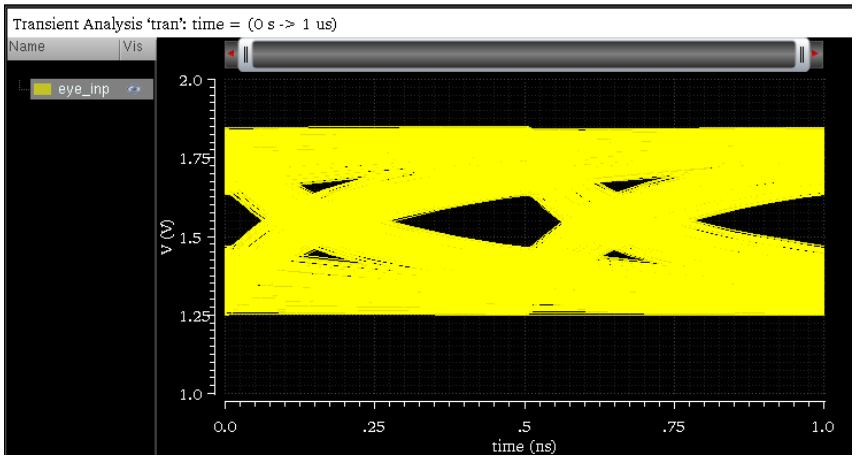
  -seed: 1

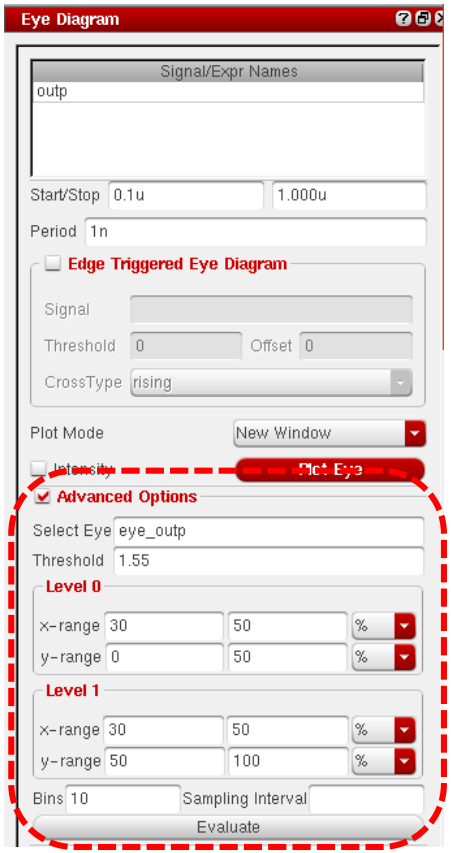
  -vlogic_high, low = 1, -1 ➔ 500mV swing to Rx

  -trise, tfall = 20p

Simulation Results(Channel)



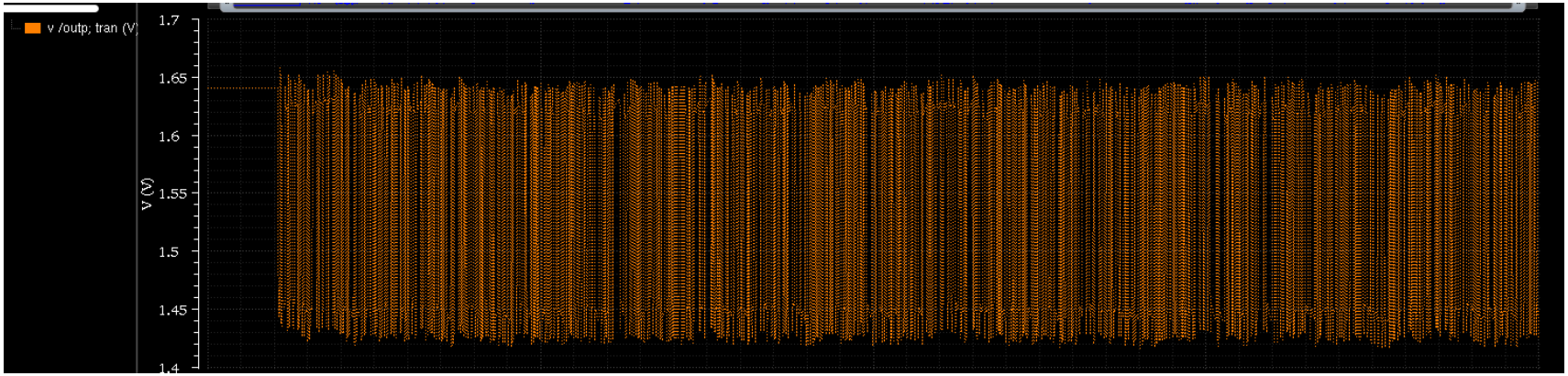


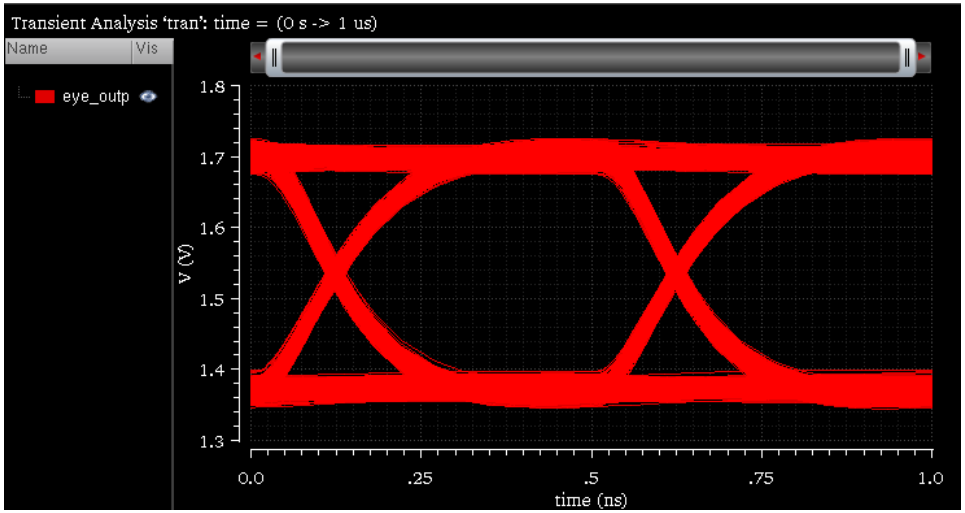


SNR Calculation

- Closed eye due to channel loss
- Small

Simulation Results(Channel + CTLE)





- Loss compensation by CTLE
- Higher SNR(15.8)

Homework

- Rx CTLE

Design source-degenerate CTLE which provides larger SNR than 17 for the same channel using the same random bit stream shown in the class. For the SNR determination, simulate the eye for 1us.