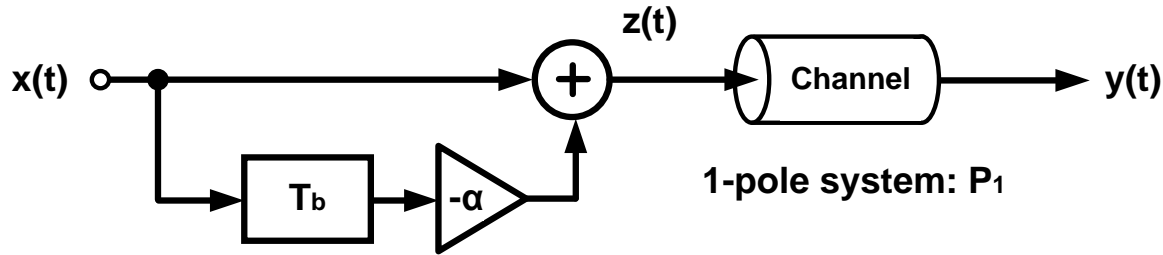


# **High-Speed Serial Interface Circuits and Systems**

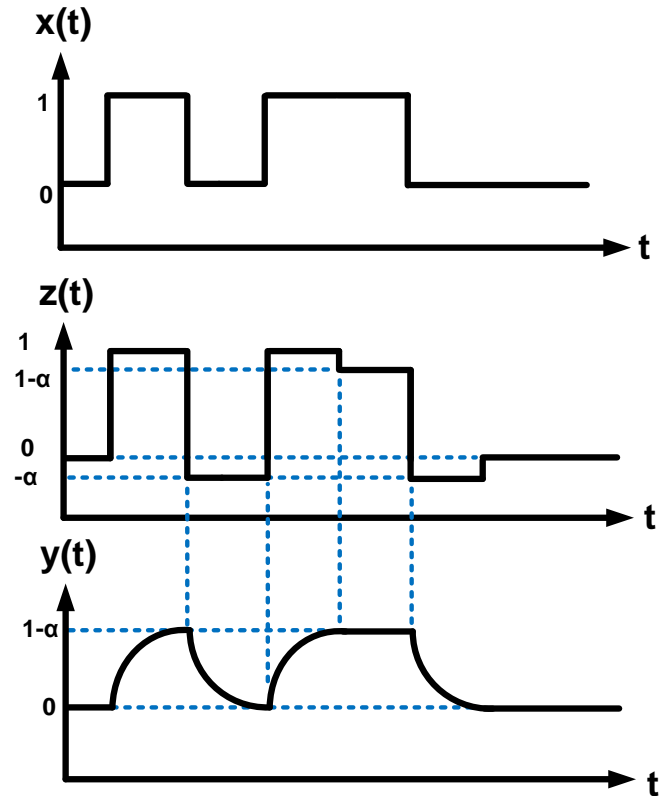
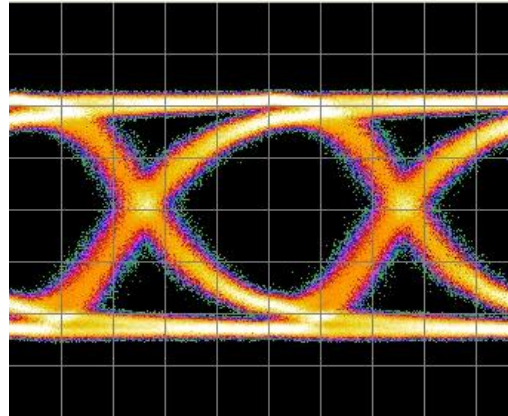
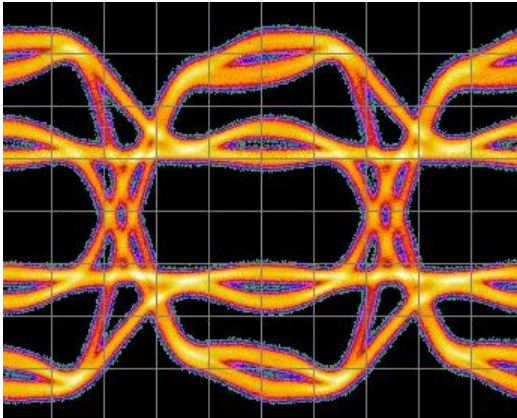
## **Design Exercise 8 – FIR(Finite-Impulse Response) Equalizer**

# FIR Equalization



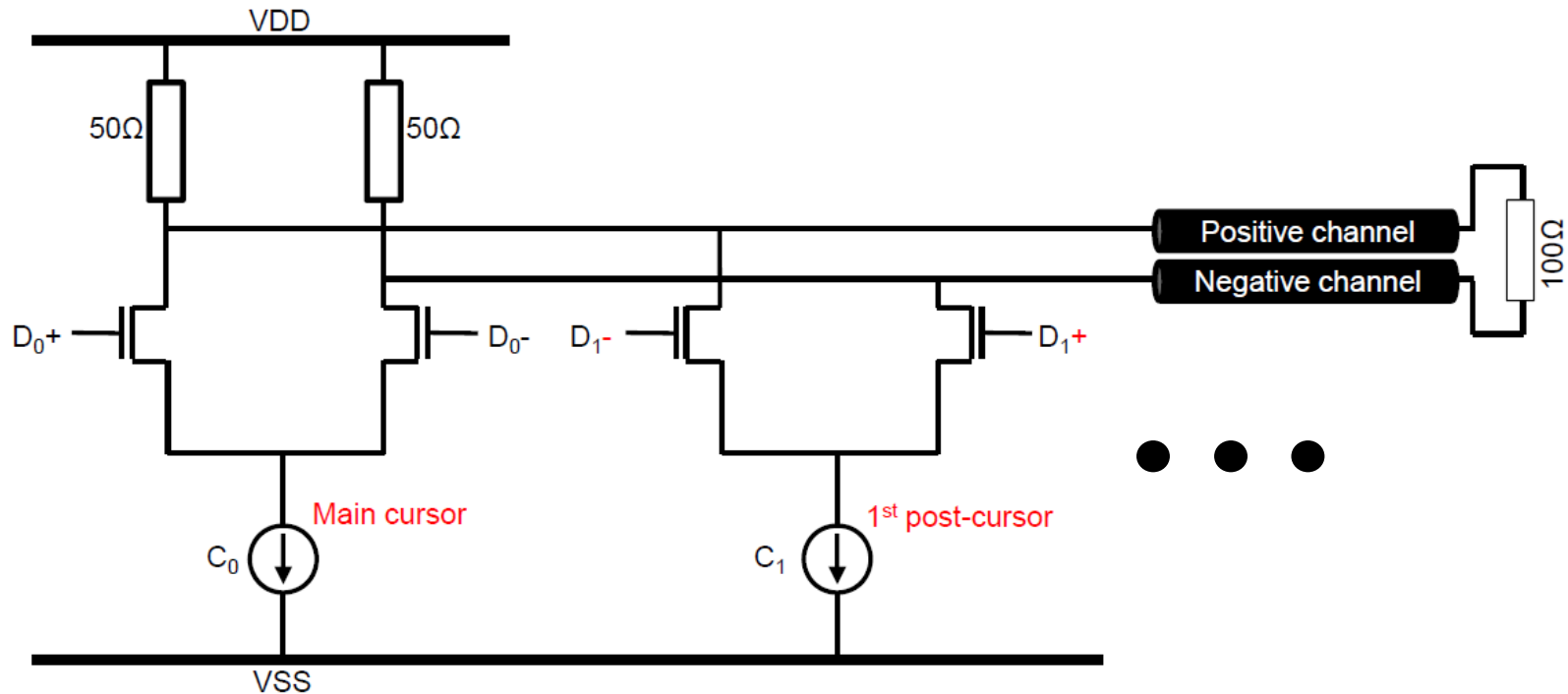
1-pole system:  $P_1$

$$bg_P = \frac{1 + \alpha}{1 - \alpha}$$



- Equalization by boosting transition bits(Pre-emphasis)
- Equalization by reducing transition bits(De-emphasis)

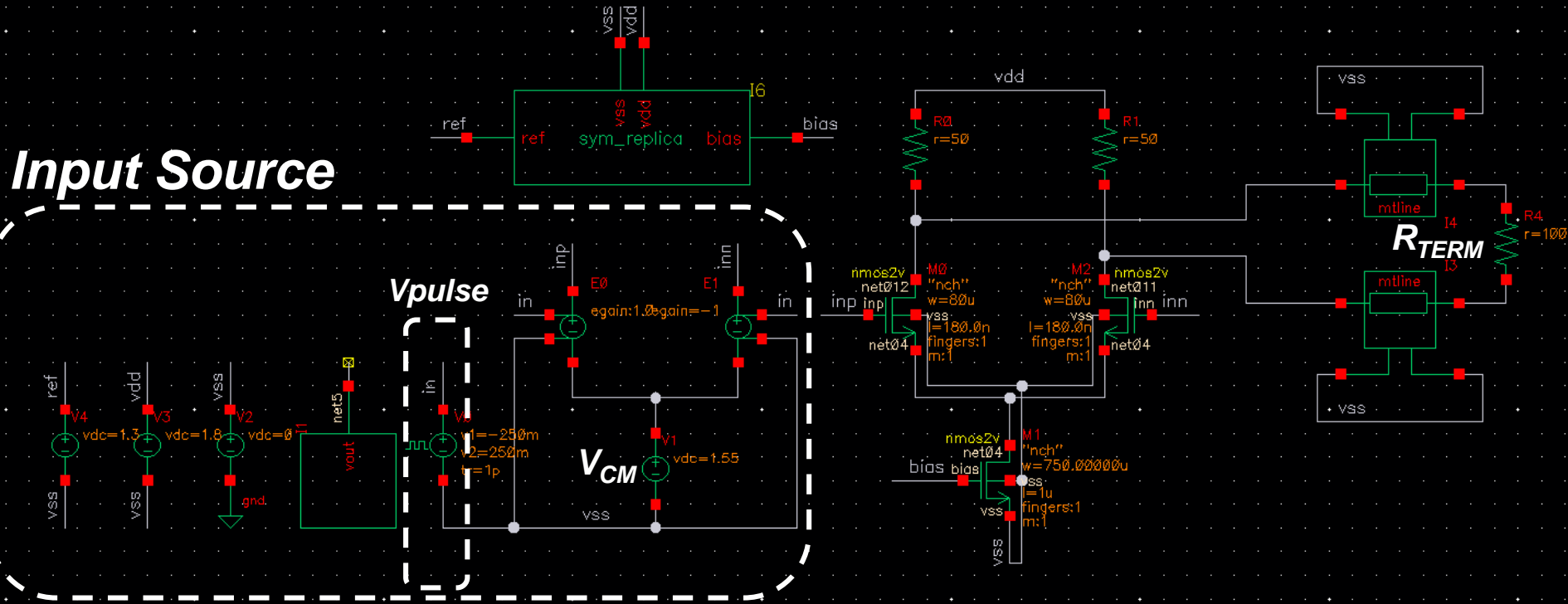
# FIR Equalizer Using CML Driver



- Goal: Equalize 2Gbps data transmission  
➔ By time-domain analysis(pulse response)
- 2-tap (one post-cursor) FIR equalizer

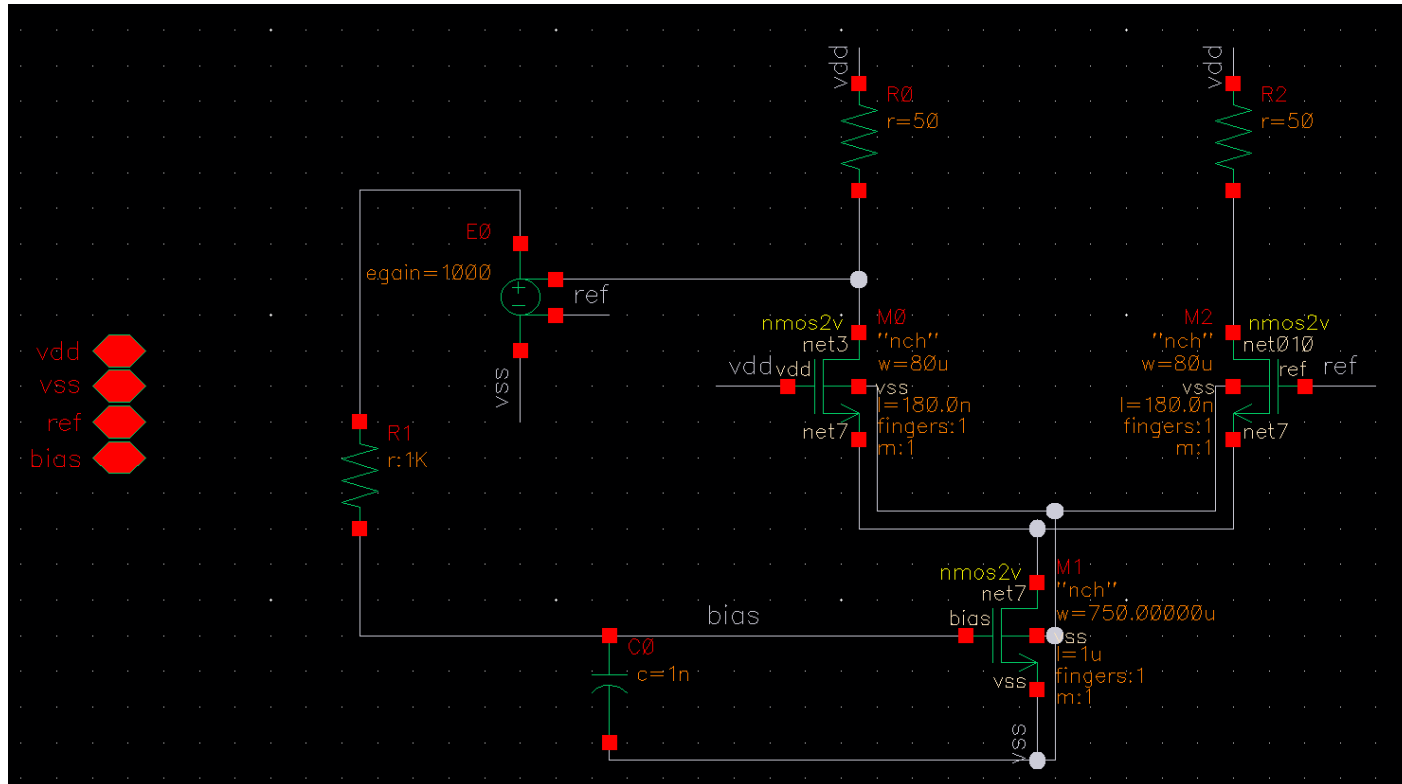
# Time-Domain Channel Characteristic

## Input Source



- Input source (Impulse)
  - Vpulse
  - 250mV ~ 250mV
  - Period : 1s
  - Delay time : 1ns
  - Rise & fall time : 1ps
  - Pulse width : 499ps
- CML Output Driver
  - Input MOSFETs: 80u/180n
  - Tail MOSFETs: 750u/1u
  - Load resistors: 50 Ohm
  - Reference voltage : 1.3 V (500mV swing)
  - RTERM : 100 Ohm

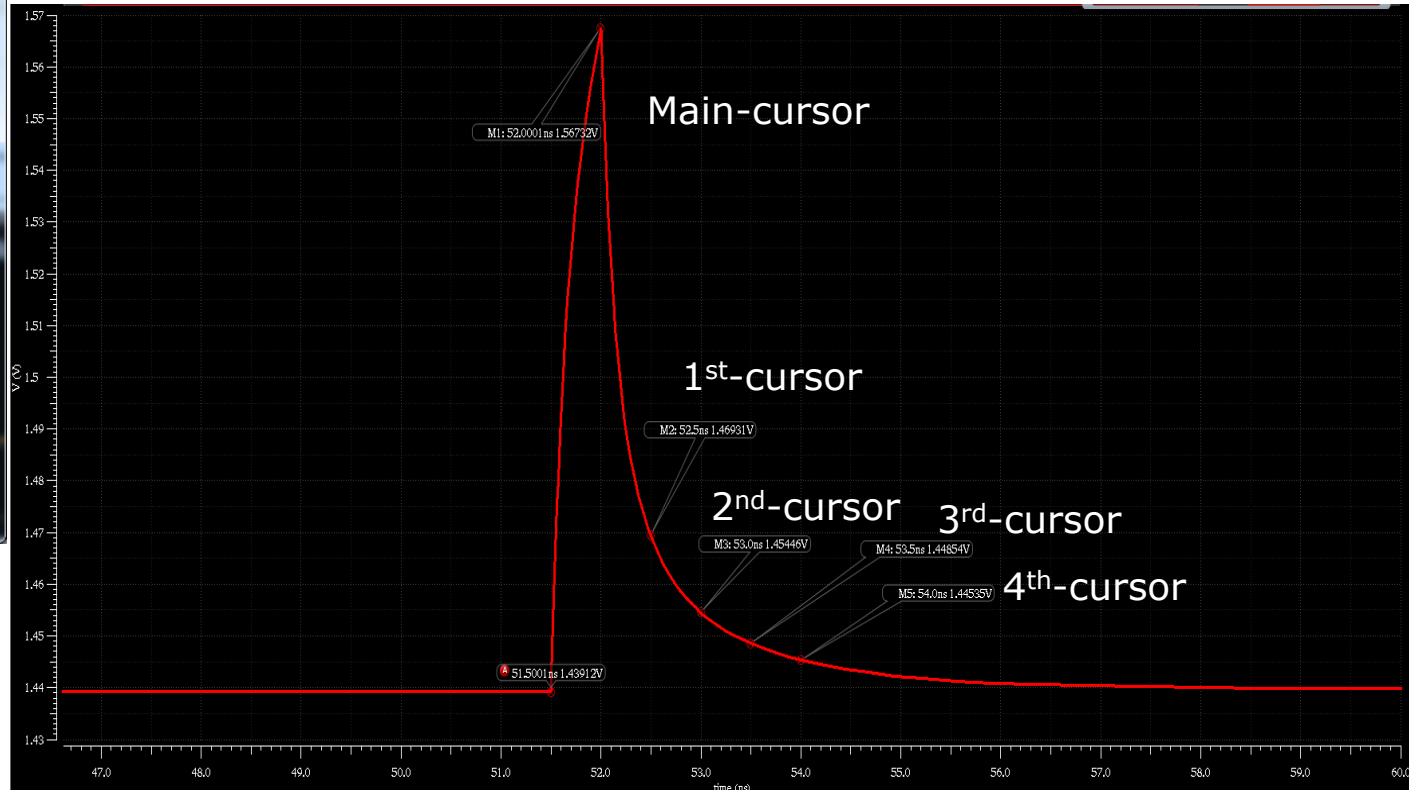
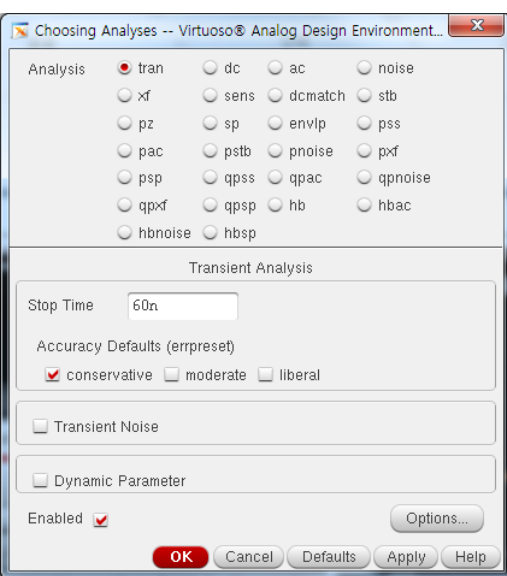
# Replica Circuit



Resistor: 1K Ohm  
Capacitor: 1n F

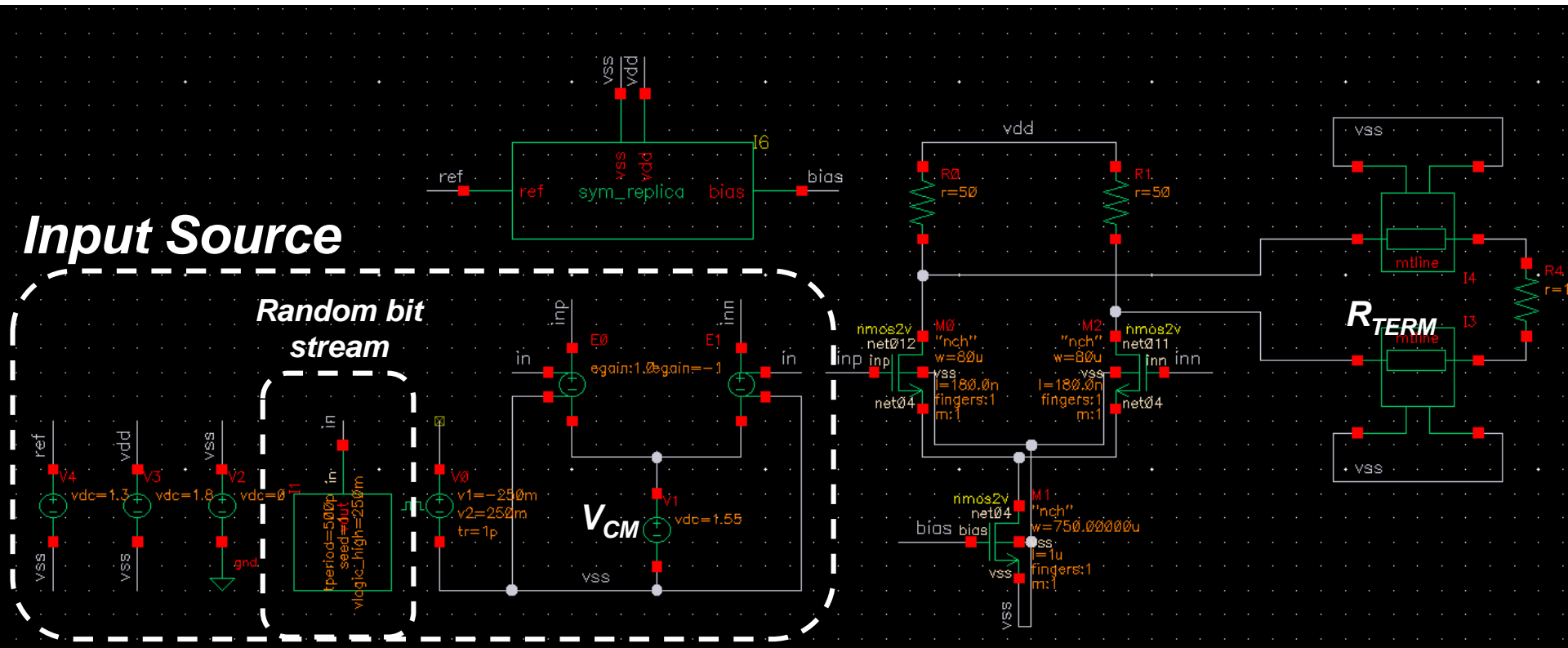
VCVS  
gain: 1000  
Max, Min output voltage: 1.8, 0 V

# Simulation Results (Pulse Response)



- Impulse Response
  - 0.5ns spacing each cursor
  - Main-cursor, 1<sup>st</sup> post-cursor, 2<sup>nd</sup> post-cursor, 3<sup>rd</sup> post-cursor, 4<sup>th</sup> post-cursor

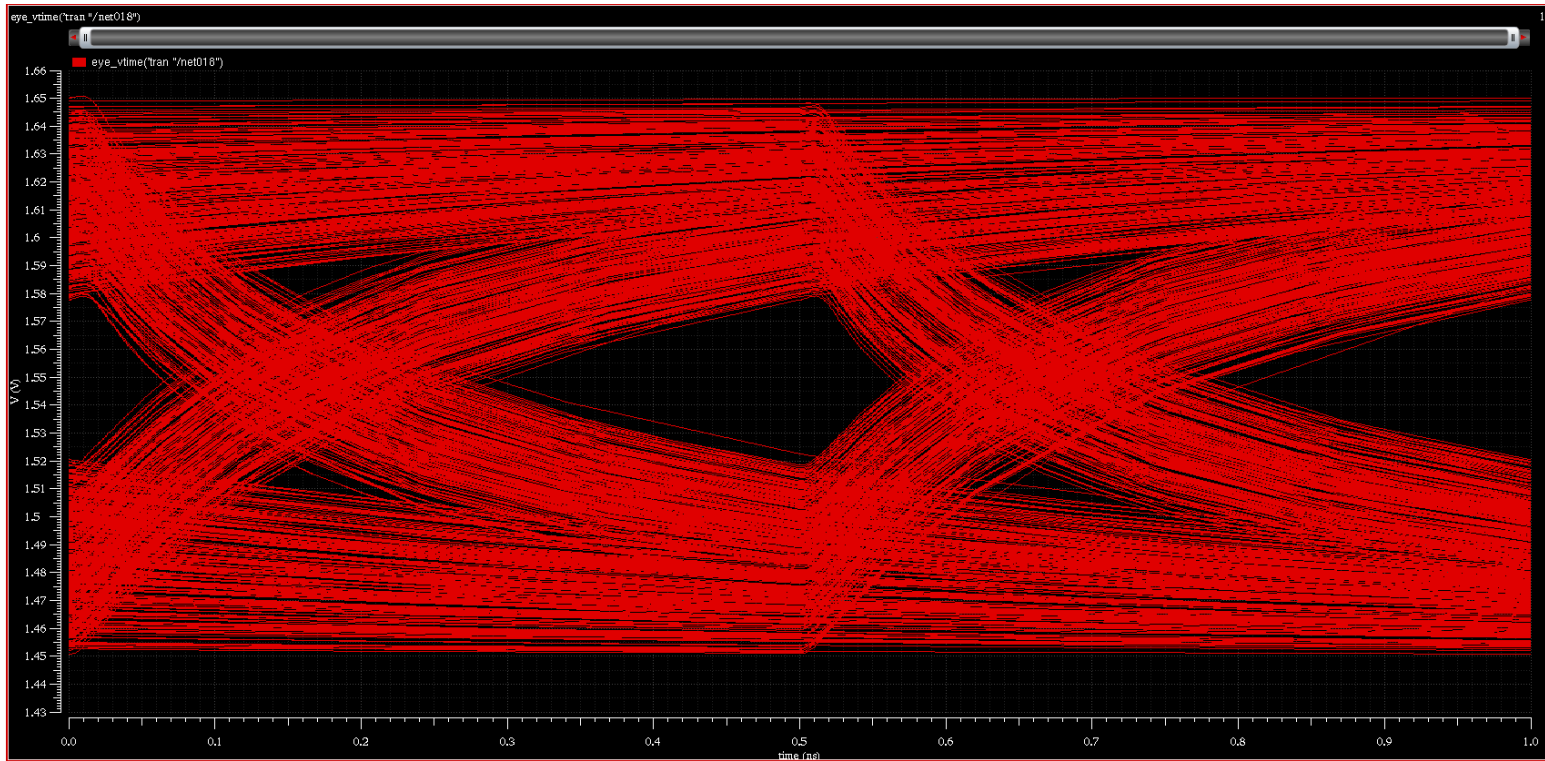
# Data Transmission with Channel



## Random bit stream

- Period:  $1/2\text{Gbps} = 500\text{ps}$
- seed: 1
- vlogic\_high, low = 250mV, -250mV  $\rightarrow$  500mV swing to Rx
- trise, tfall = 20p

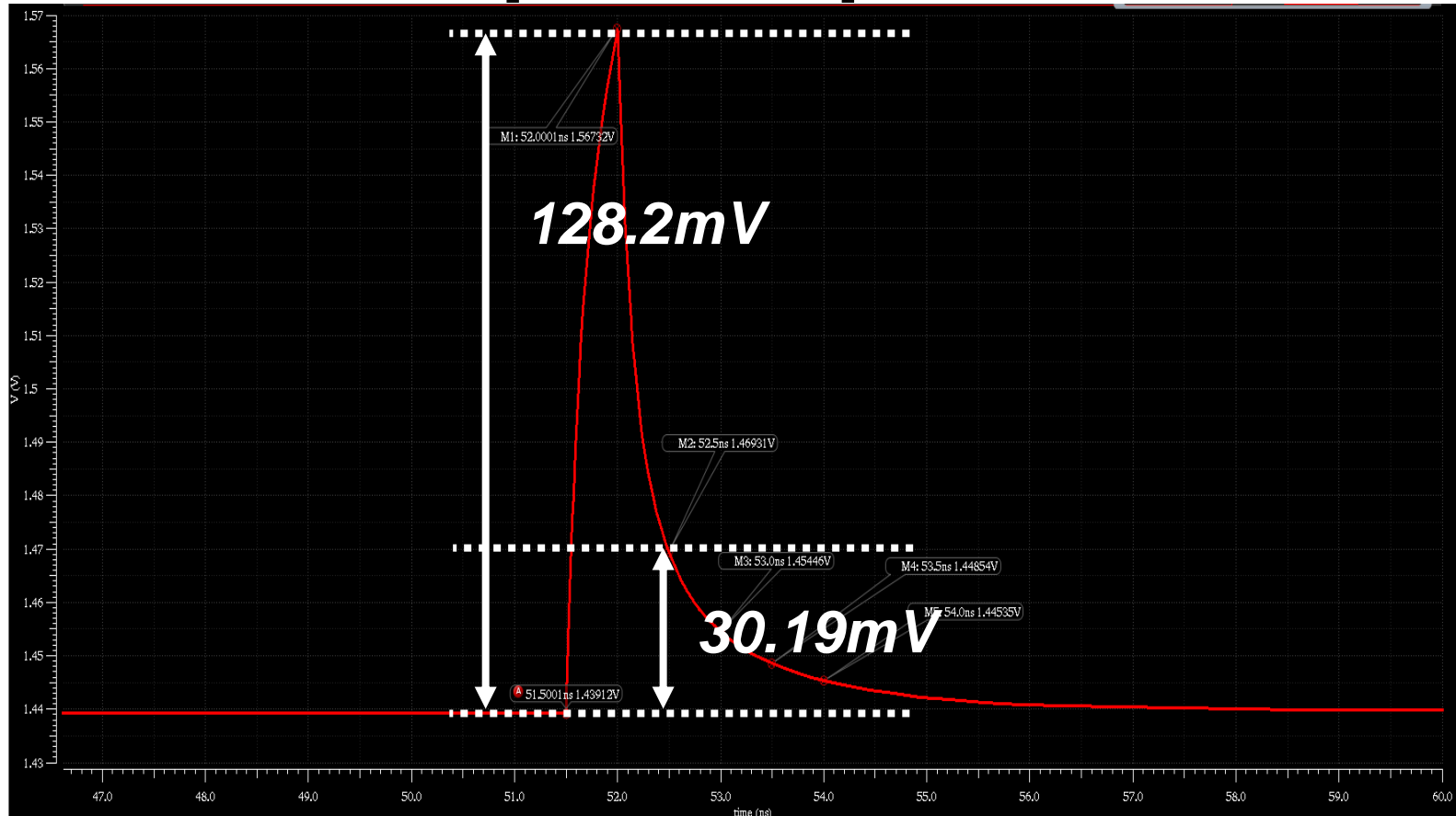
# Simulation Results (Channel Output)



Closed eye due to channel loss(1u simulation, 0.1u~1u eye diagram)



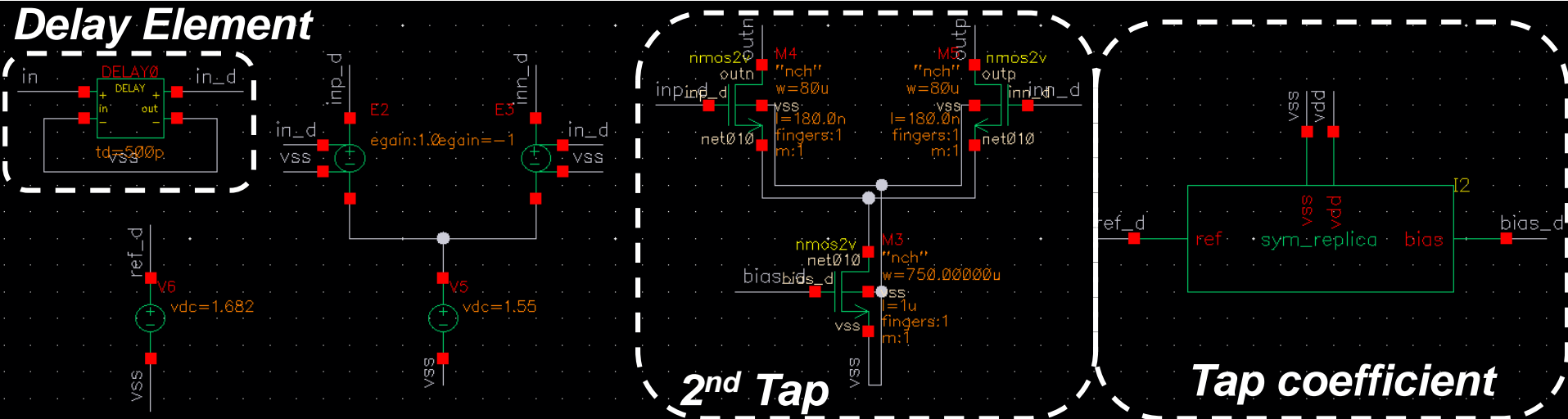
# 2-Tap FIR Equalizer



- Remove 1<sup>st</sup> post-cursor with 2-tap FIR equalizer
- FIR coefficient calculation
  - Main tap : 500mV (signal swing)
  - Second tap : 117.74mV (= 500mV x (30.19 / 128.2) )

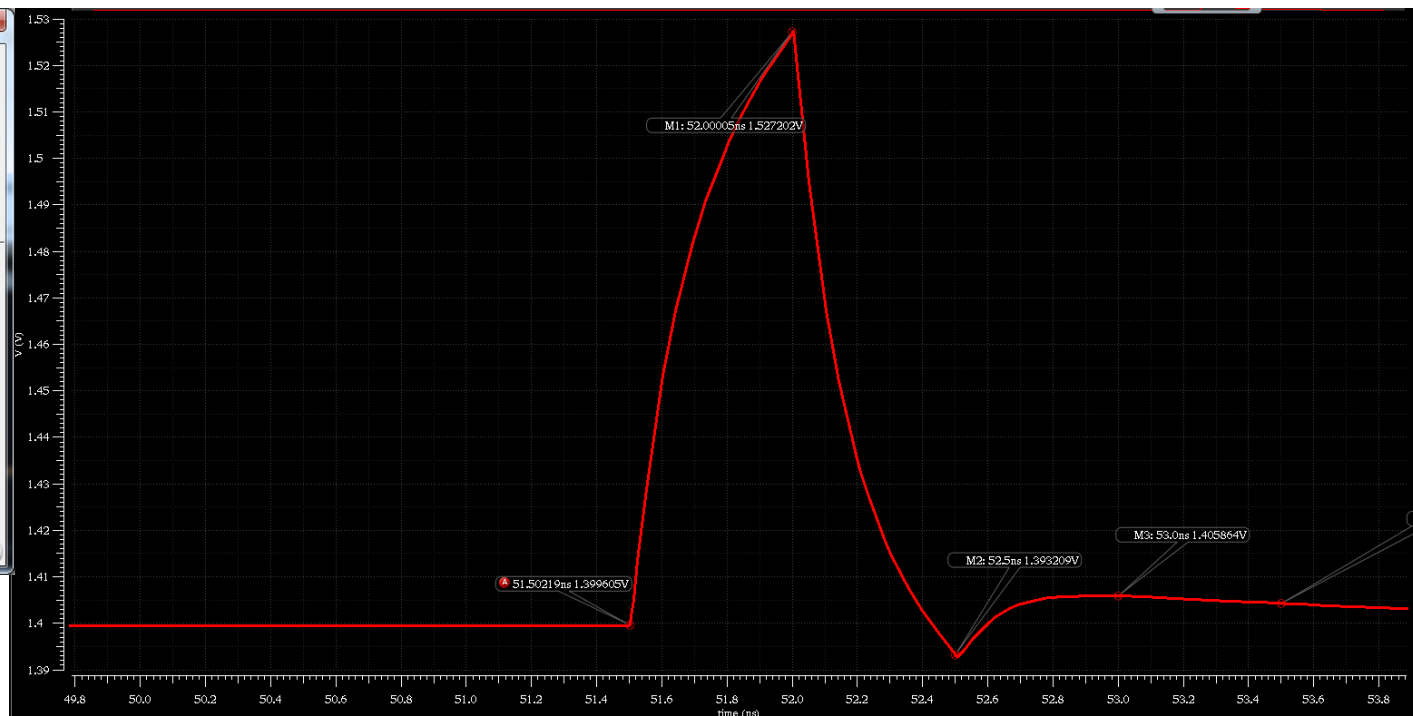
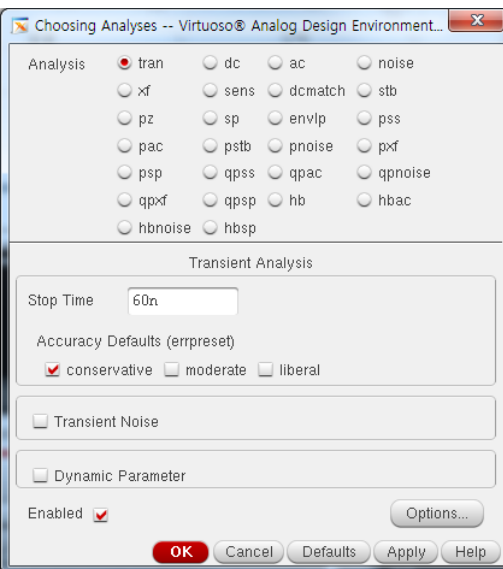
# 2-Tap FIR Equalizer

- Additional schematic for 2-tap FIR Equalizer



- 2<sup>nd</sup> tap FIR filter
  - Same sizing as CML output driver
  - Carefully connect output (outp, outn)
- Delay element(analogLib→delay)
  - 1-period (500ps) delay
  - Make sure ground tied at both input & output
- 2<sup>nd</sup> tap coefficient (117.74mV)
  - Reference voltage : 1.682V (1.8V – 117.74mV)

# Simulation Results (Pulse Response)



# Simulation Results (Channel Output)

