High-Speed Serial Interface Circuits and Systems

Design Exercise3 –

LC VCO

LC VCO Structure

✓LC Tank
- Spiral inductor (symmetric type)
- Ideal capacitor

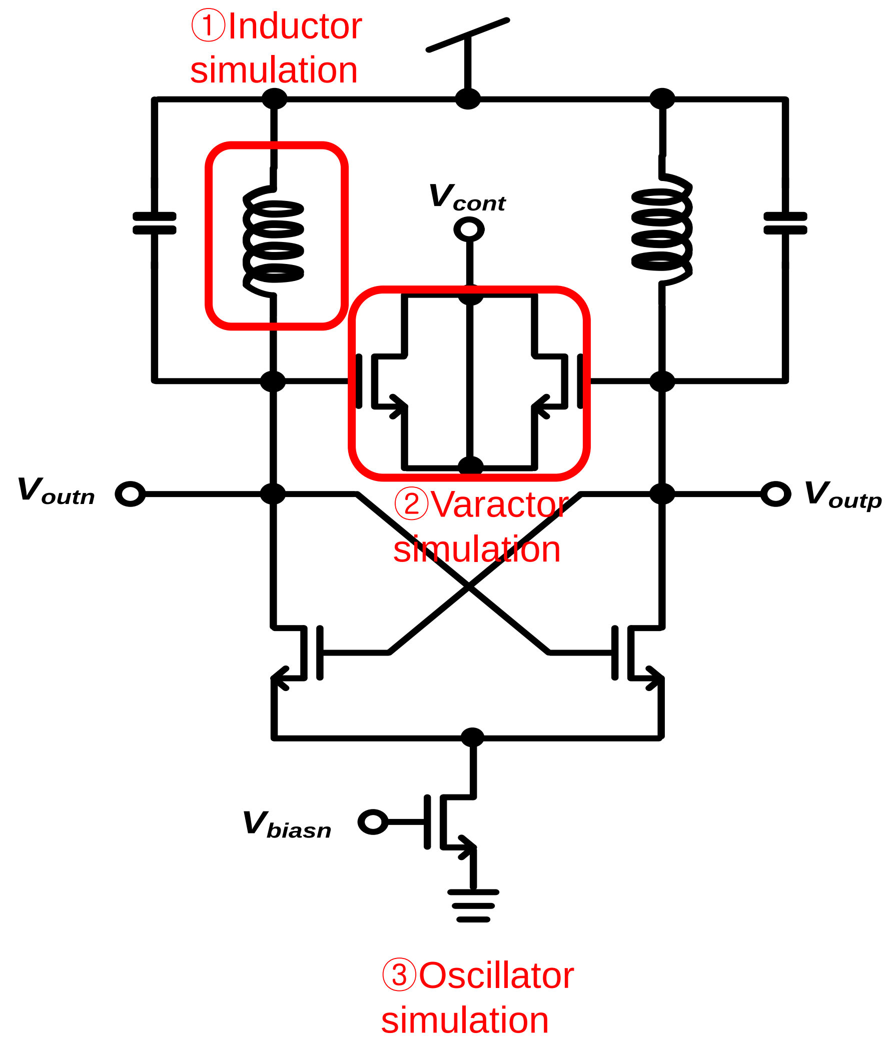
✓Varactor
- Accumulation varactor

✓Cross coupled circuit
- Negative resistance
- To compensate for the loss of the tank

✓Source MOSFET

✓OSC frequency

$$f_o = \frac{1}{2\pi\sqrt{LC}}$$



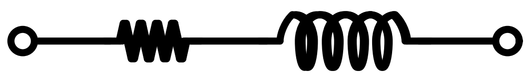
Design Example

✓ LC voltage controlled oscillator (VCO)

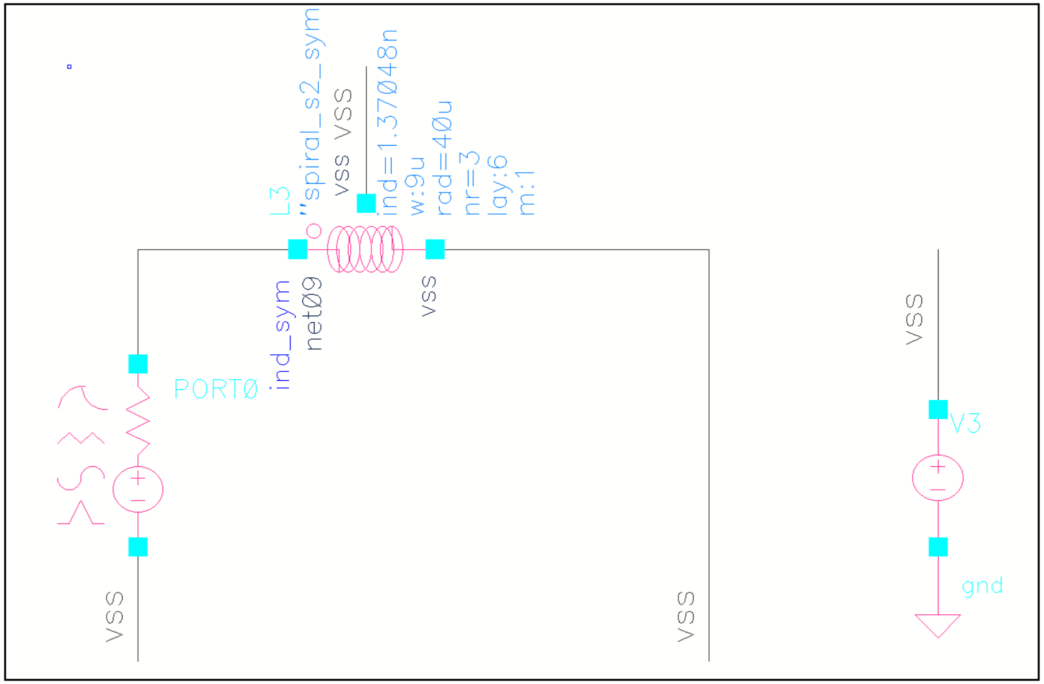
- Supply voltage: 1.8V
- Frequency tuning range: > 30-MHz
- Oscillation frequency : 1.5-GHz
- Phase noise @ 1-MHz offset with 1.5-GHz: < -125dBc

Inductor Model

- An equivalent circuit model of inductor
  - Series connection of resistance and inductance
  - Analyze inductance into using Z-parameter



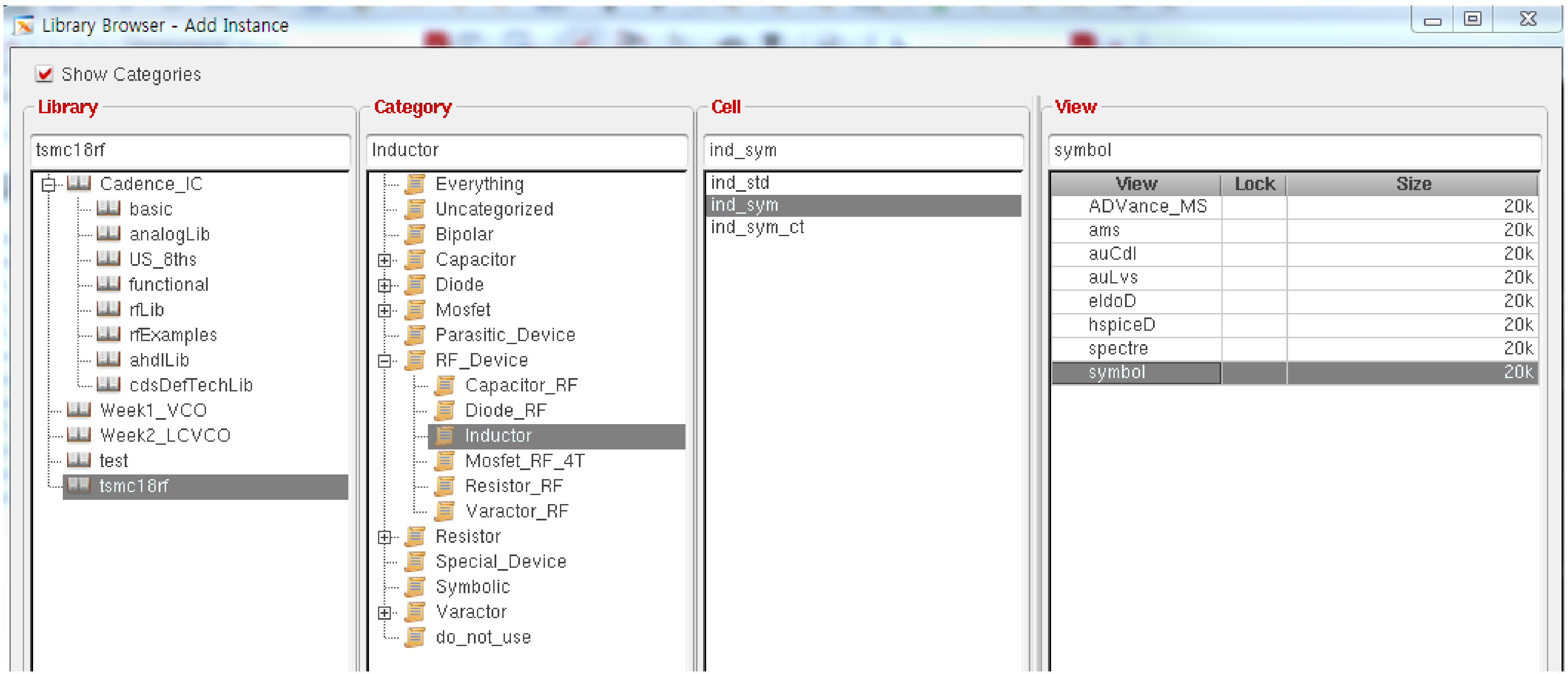
< Equivalent circuit of inductor >



< Simulation schematic >

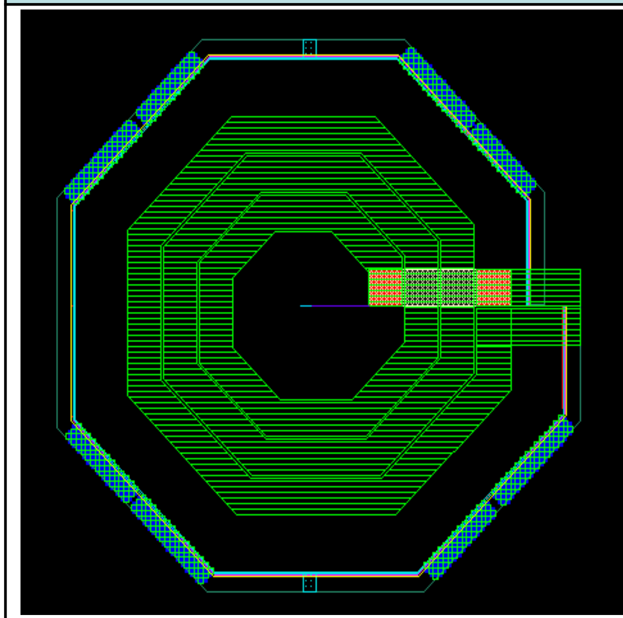
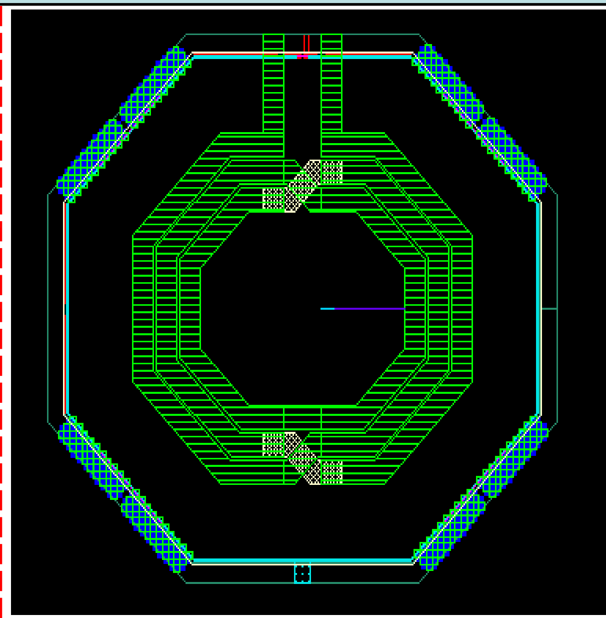
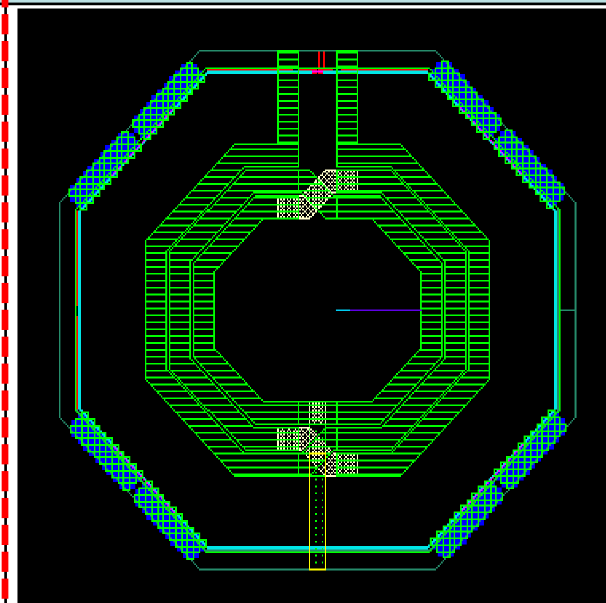
Inductor

- Inductor selection
  - Tsmc18rf → RF_Device → Inductor → ind_sym → symbol
  - Symmetric inductor selection



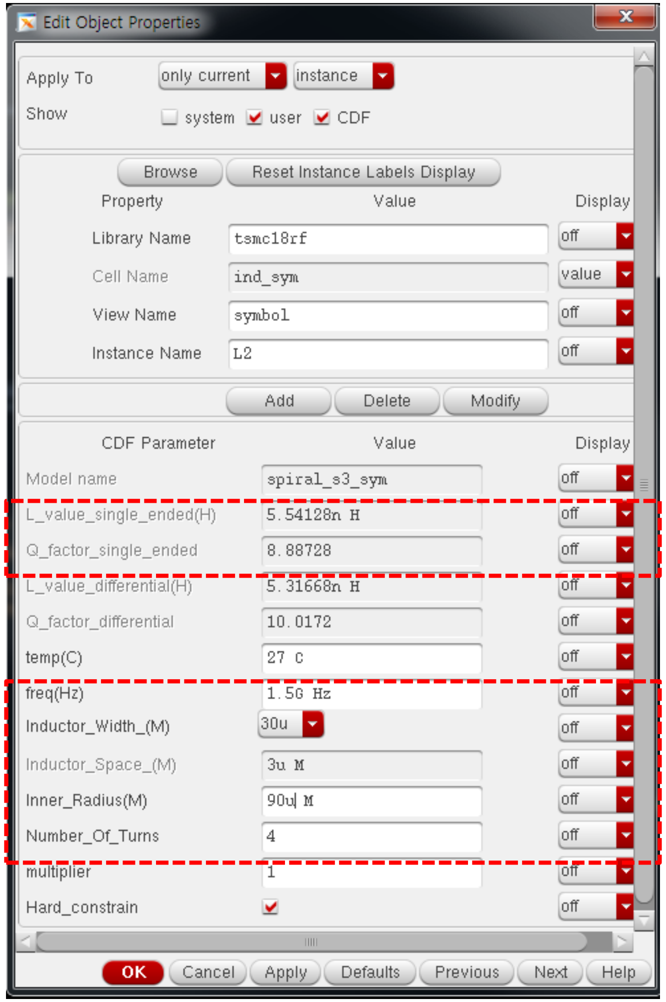
Inductor PDK

- TSMC 180nm spiral inductor PDK
  - Single-ended
  - Symmetric
  - Symmetric with a center tap

ind-_std	ind_sym	ind_sym_ct
		

Inductor Parameters

- Setting of frequency, inductor width, inner radius and number of turns.

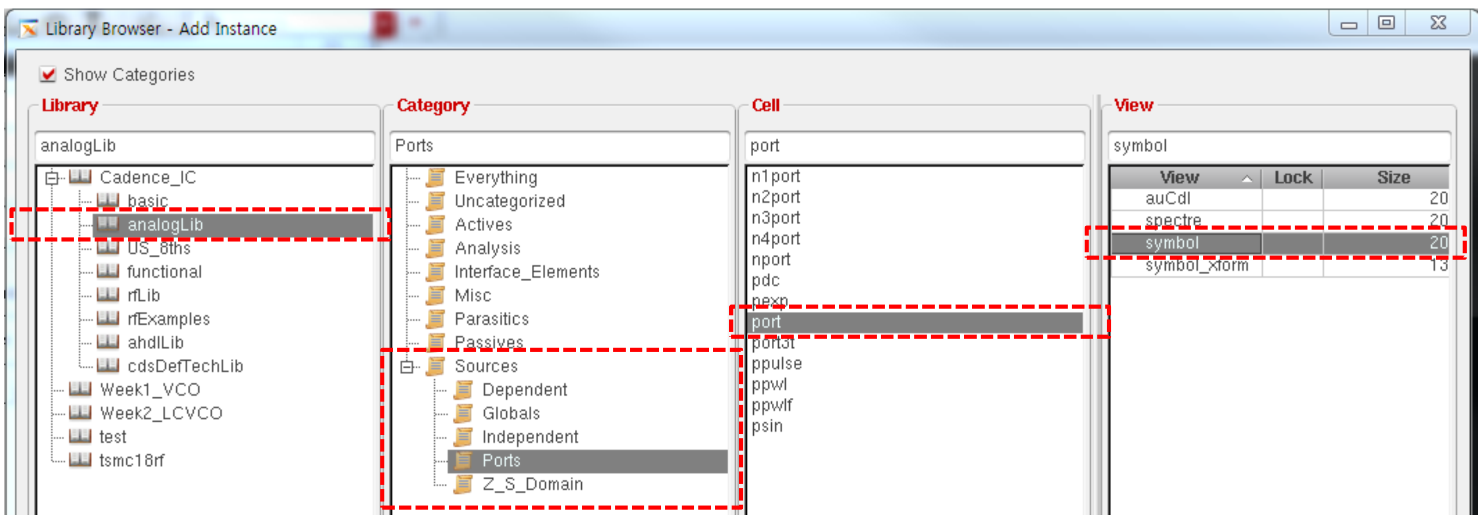


- Freq(Hz) : 1.5G
- Inductor_Width (M) : 30u
- Inner_Radius (M) : 90u
- Number_Of_Turns : 4

→ Inductance : 5.54nH
→ Q_factor : 8.88

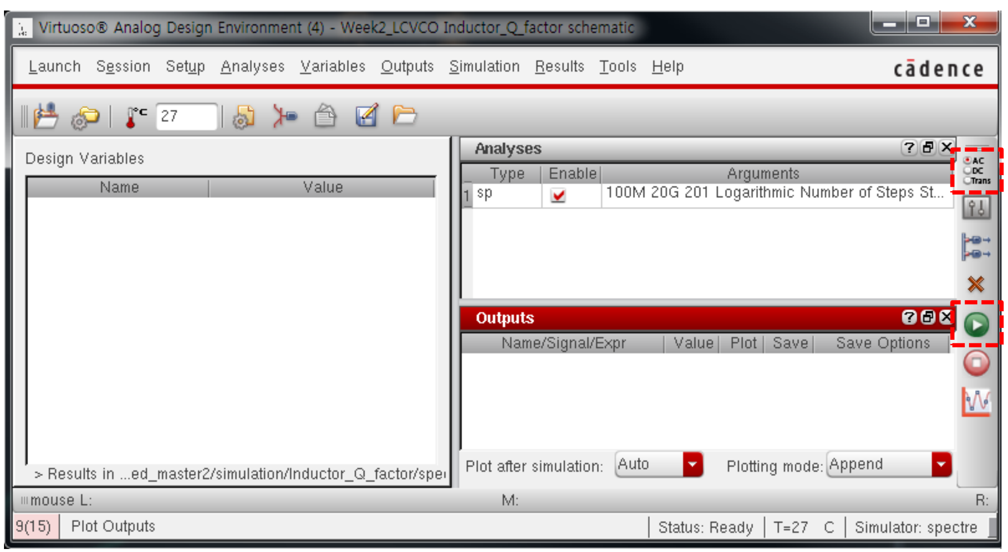
Port for S-parameter Simulation

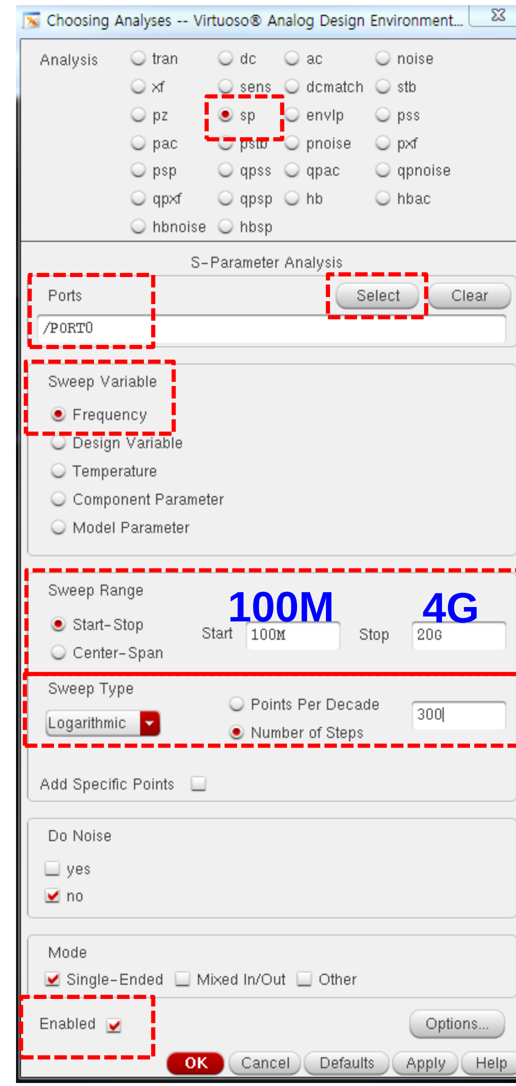
- Port
  - Show Categories check
  - analogLib → Sources → Ports → port → symbol



S-parameter Simulation Setup

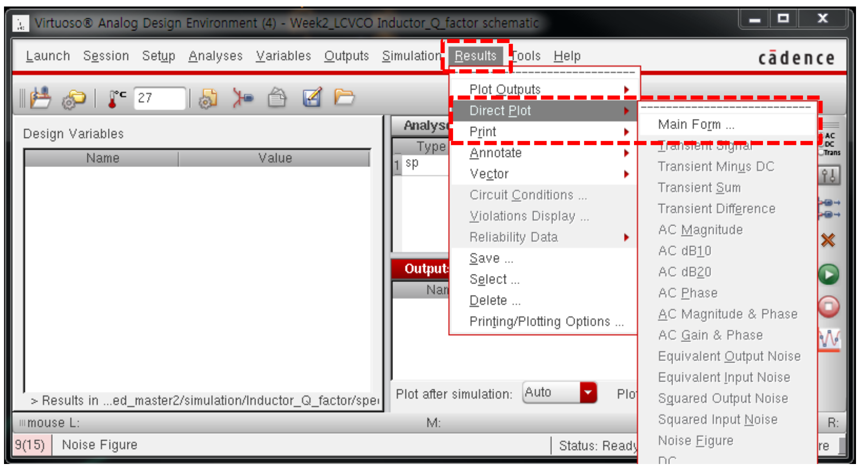
- Simulation condition setting
  - Analysis : sp (S-Parameter Analysis)
  - Ports : Port0 (schematic node choice)
  - Sweep Variable : Frequency
  - Sweep Range : 100M ~ 4G
  - Sweep Type : Logarithmic
  - Number of Steps : 300
  - Enabled check → OK → Netlist and Run

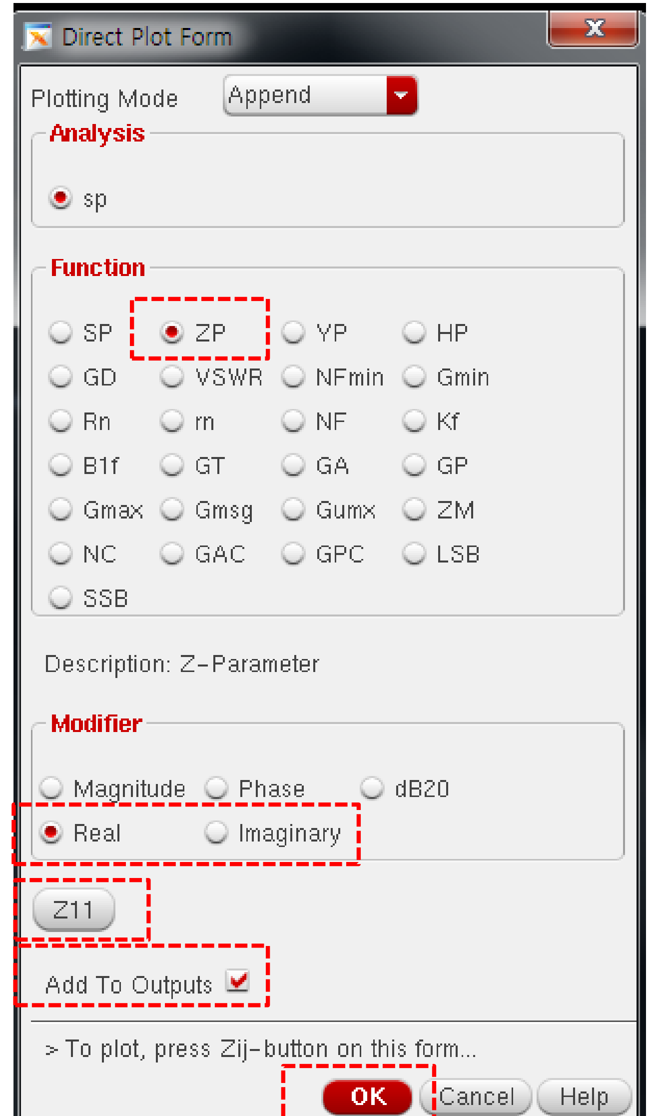




Plotting Z-parameter

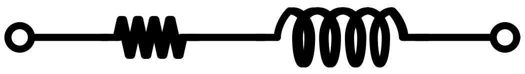
- Simulation condition setting
  - Results → Direct Plot → Main Form
  - Function : ZP
  - Add To Outputs choice
  - Modifier : Real → Z11 and Imaginary → Z11
  - OK





Z-parameter Results

- Z = R + jωL
  - Resistance = Real [Z11]
  - Inductance = Imaginary [Z11] / ω
  - Check the SRF(self resonance frequency)



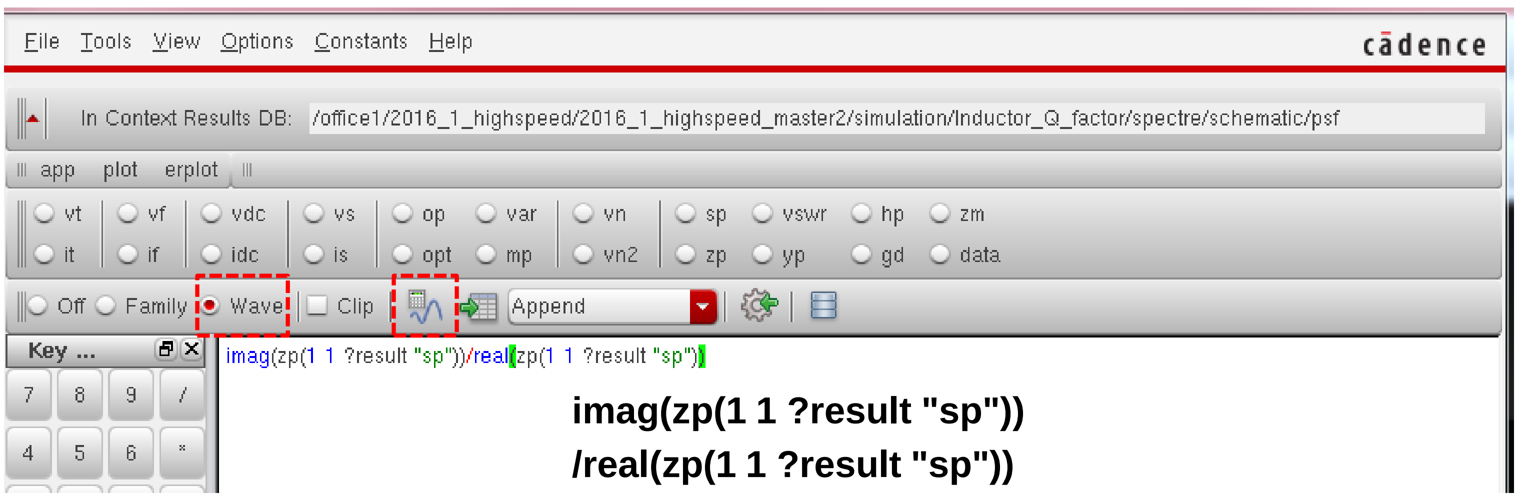
< Equivalent circuit of inductor >

Q-factor

- In an ideal series RL circuit

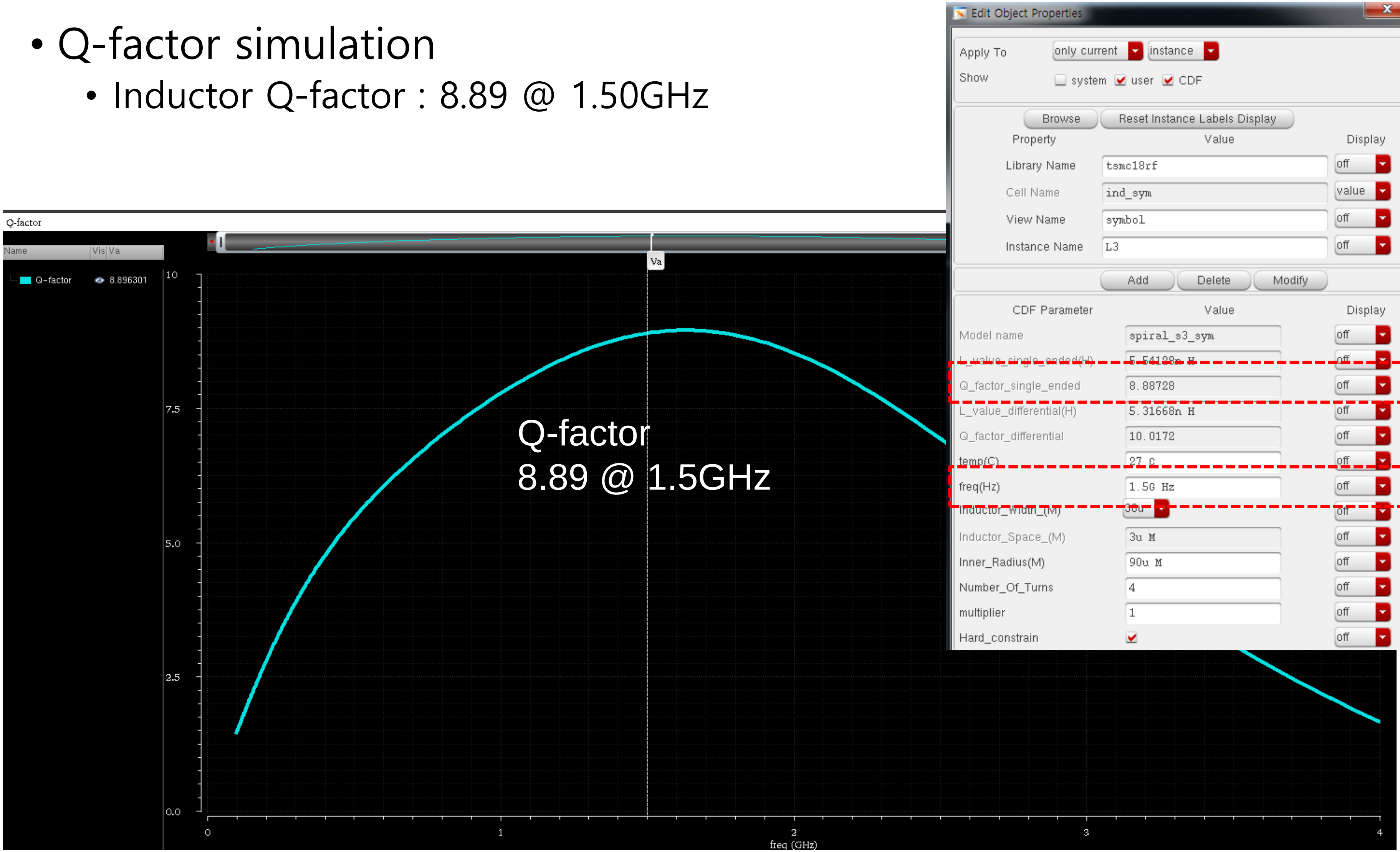
$$Q = \omega \frac{energy\,stroed}{energy\,loss} = \frac{\omega L}{R} = \frac{imag(\mathrm{Z11})}{rea(\mathrm{Z11})}$$

  - Calculator (Visualization & Analysis XL)
  - Wave choice → imag(zp(1 1 ?result "sp")) /real(zp(1 1 ?result "sp"))



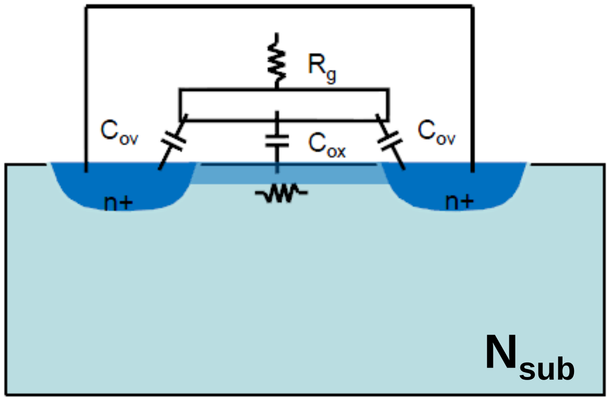
Q-factor Results

- Q-factor simulation
  - Inductor Q-factor : 8.89 @ 1.50GHz

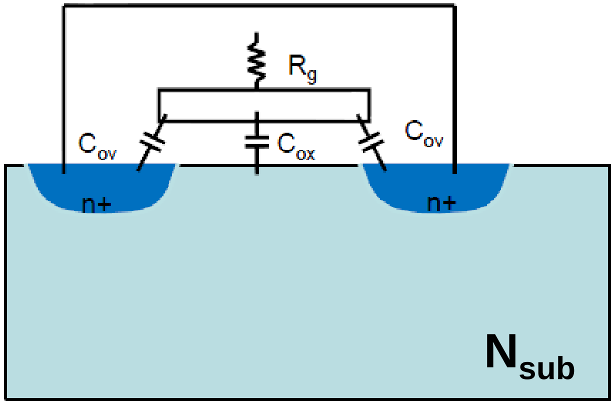


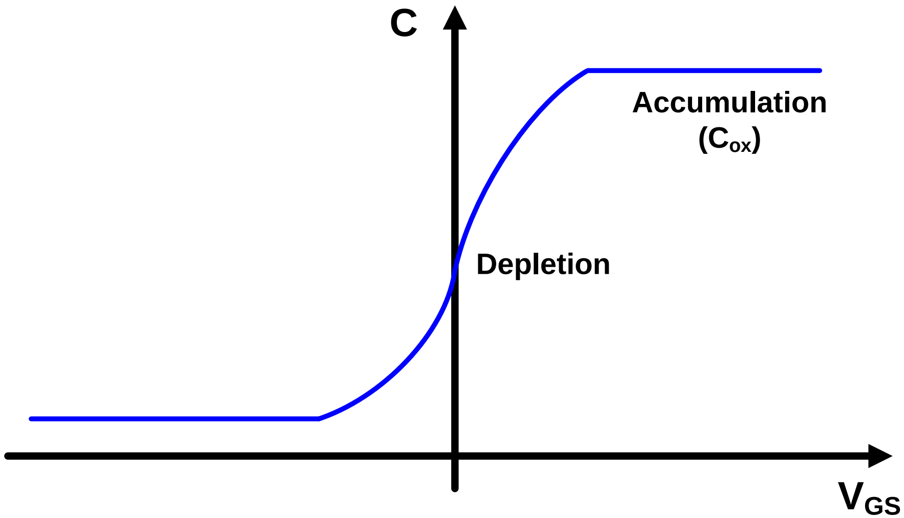
Accumulation Mode Varactor

- On (Accumulation)

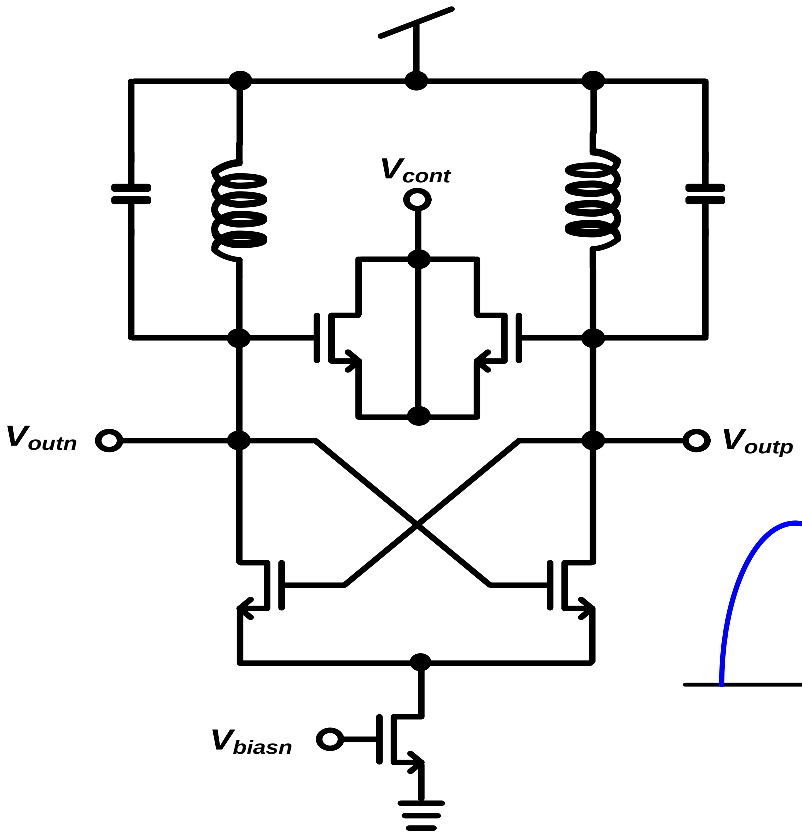


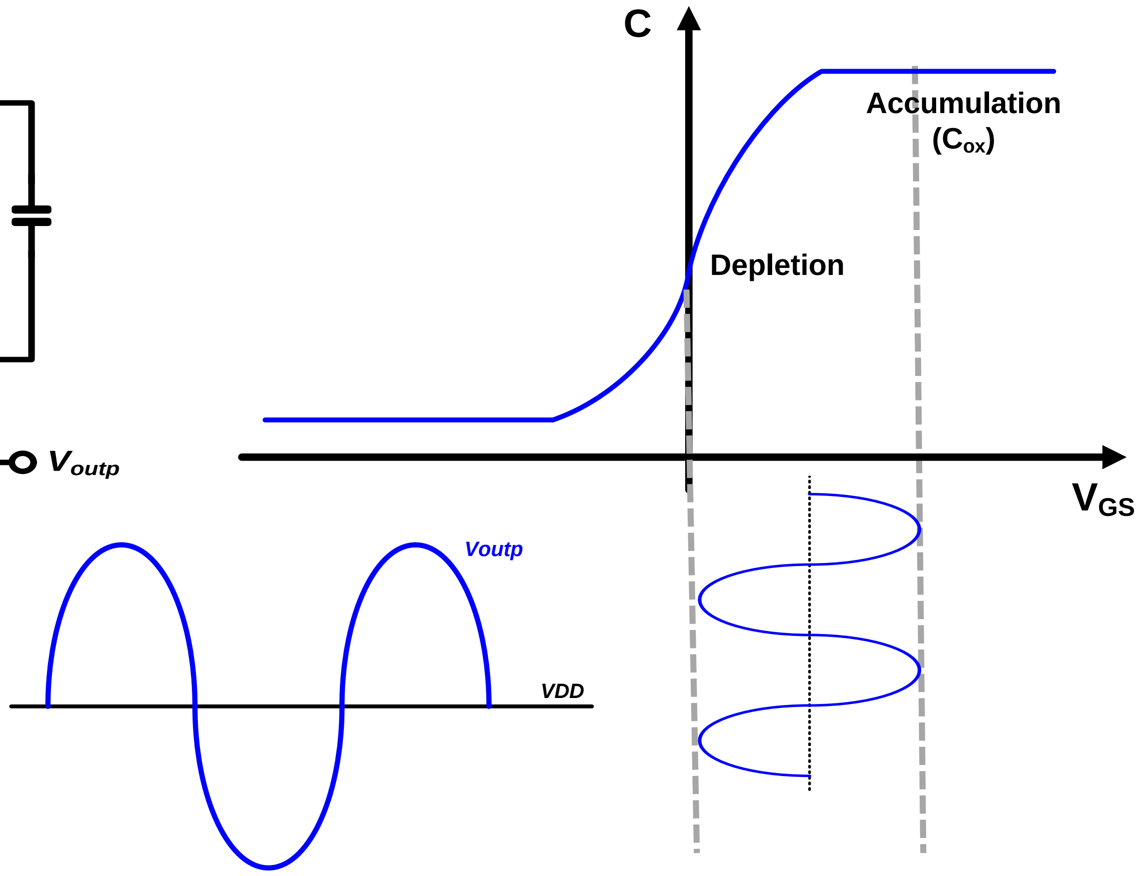
- OFF (Depleted)





Oscillator with Varactor

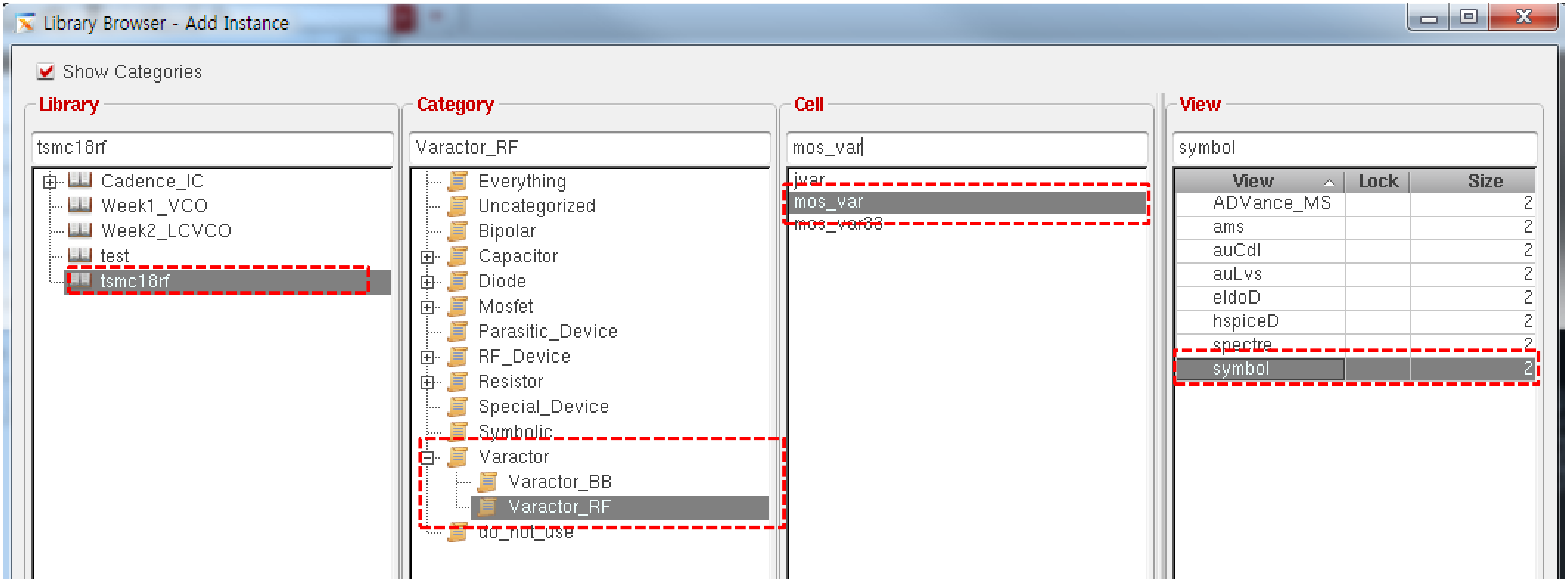




- Change average capacitance from control voltage.

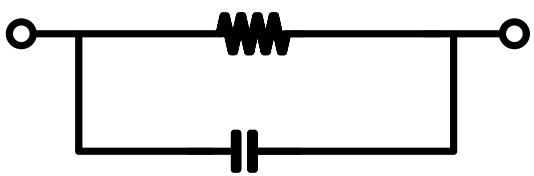
Varactor

- Varactor selection
  - Tsmc18rf → Varactor → Varactor_RF → mos_var → symbol

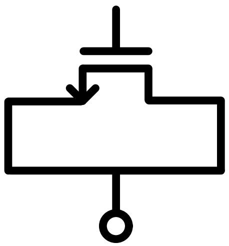


Varactor Modeling

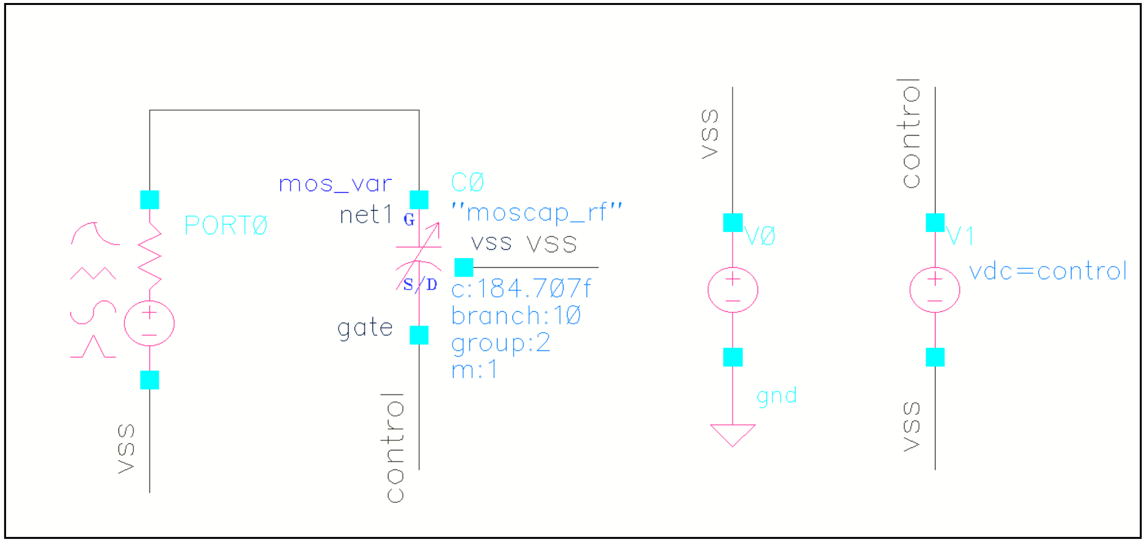
- An equivalent circuit model of varactor
  - Parallel connection of resistance and capacitance
  - Analyze capacitance into using Y-parameter



< Equivalent circuit of varactor >



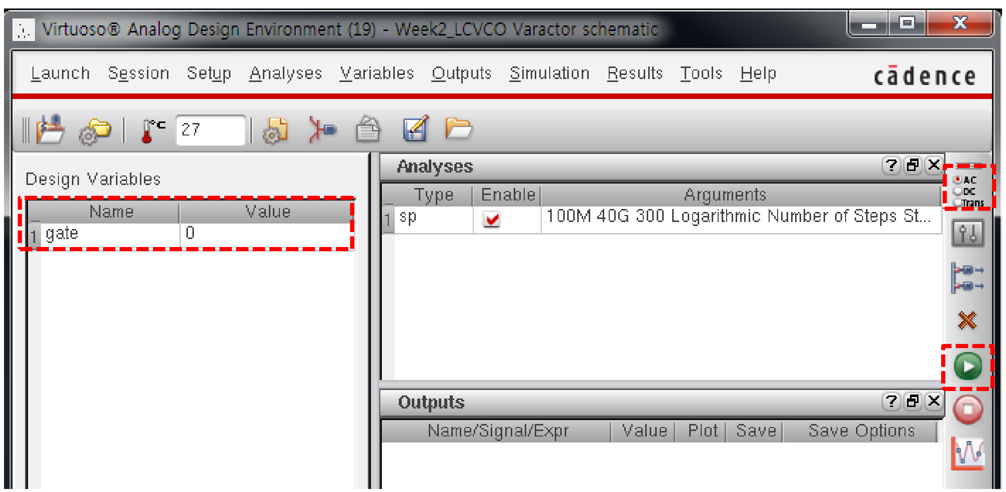
< Varactor structure >

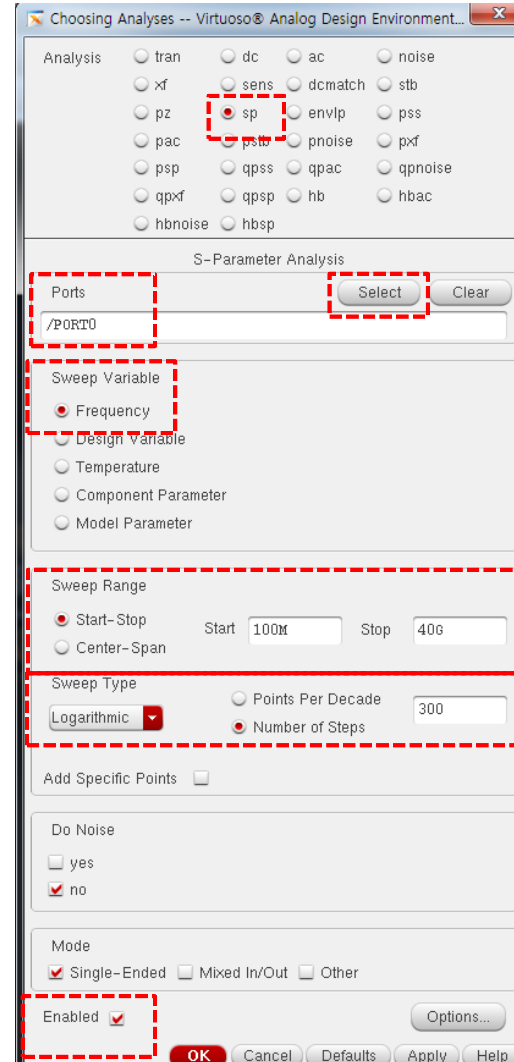


< Test schematic >

S - Parameter

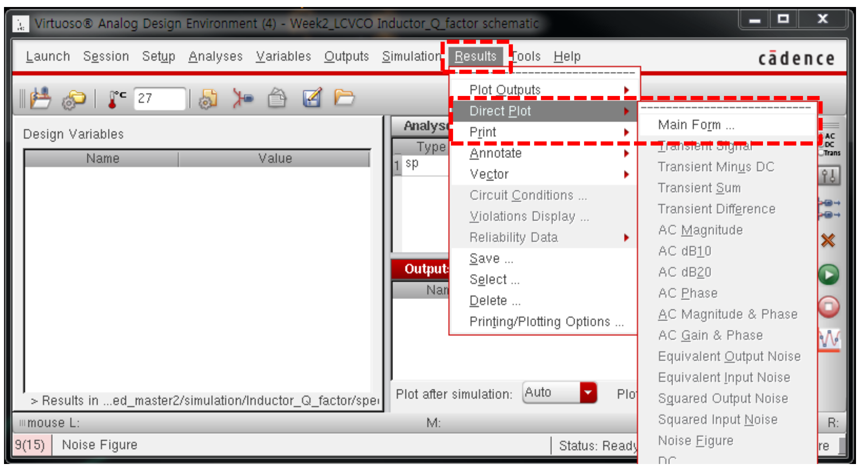
- Simulation condition setting
  - Analysis : sp (S-Parameter Analysis)
  - Ports : Port0 (schematic node choice)
  - Sweep Variable : Frequency
  - Sweep Range : 100M ~ 40G
  - Sweep Type : Logarithmic
  - Number of Steps : 300
  - Enabled check → OK → Netlist and Run

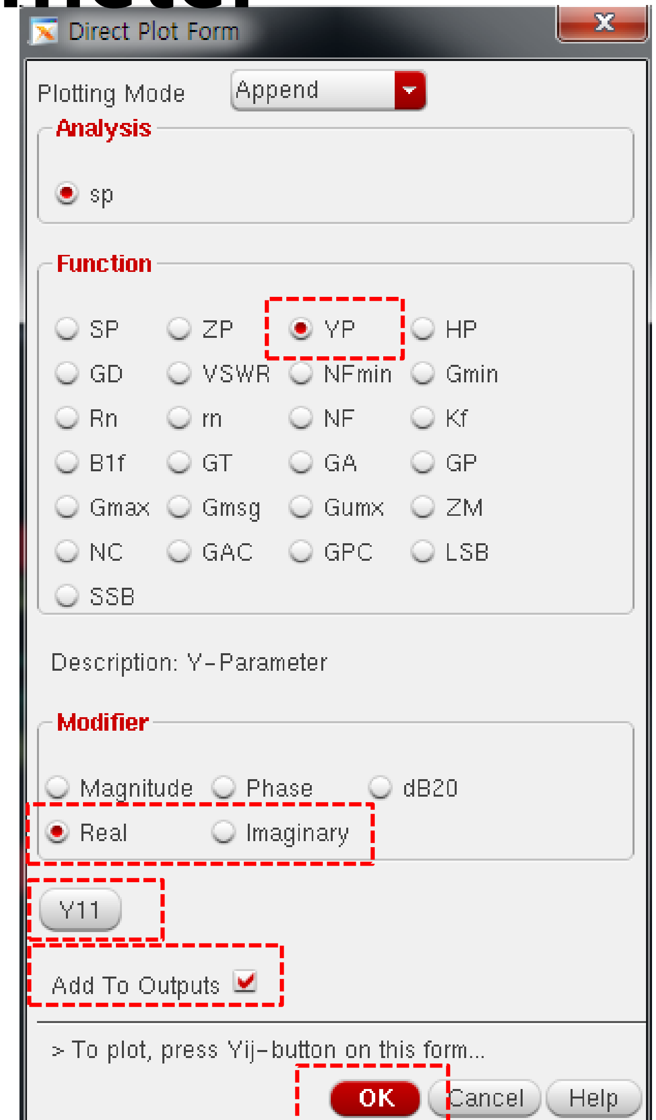




Plotting Y- Parameter

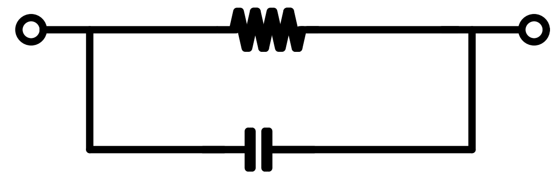
- Simulation condition setting
  - Results → Direct Plot → Main Form
  - Function : YP
  - Add To Outputs choice
  - Modifier : Real → Y11 and Imaginary → Y11
  - OK



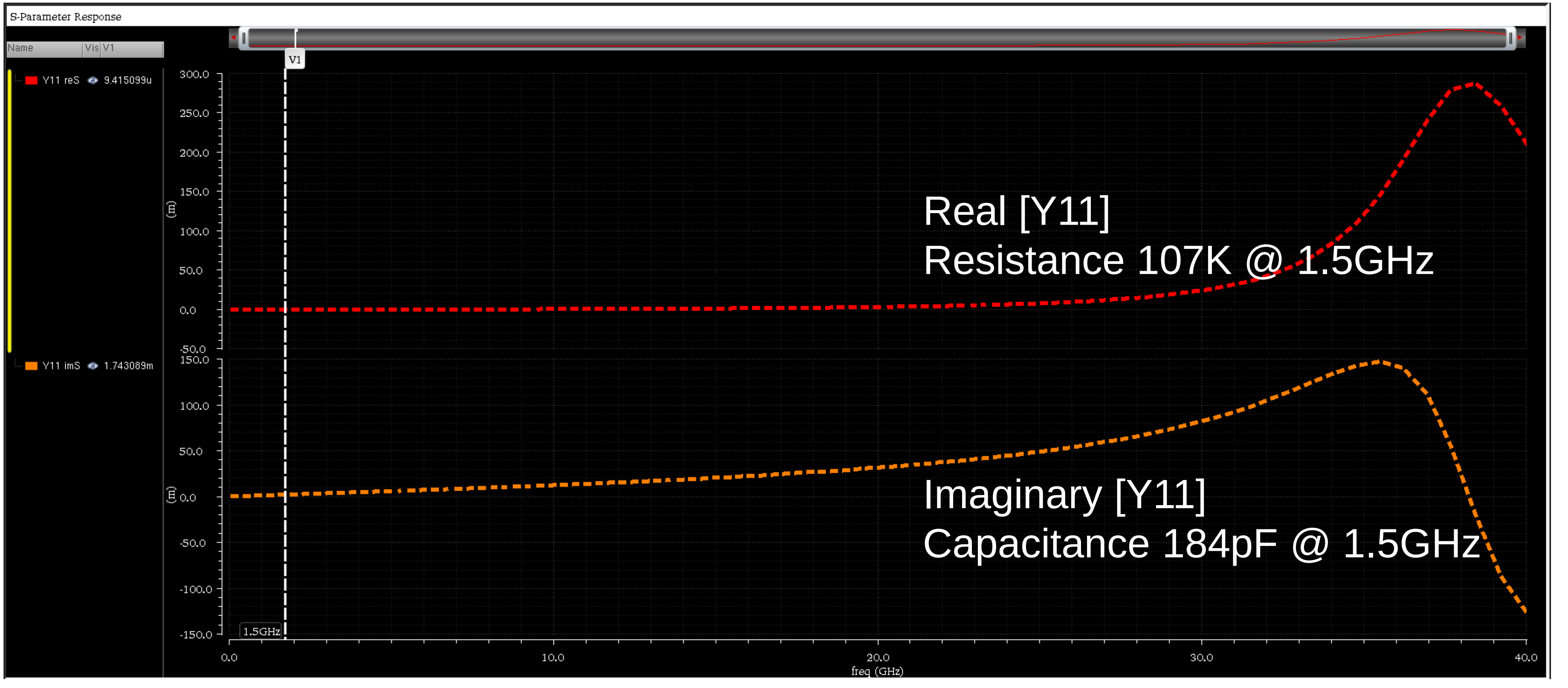


Y- Parameter

- Y = 1/R + jωC
  - Resistance = 1/ Real [Y11]
  - Capacitance = Imaginary [Y11] / ω

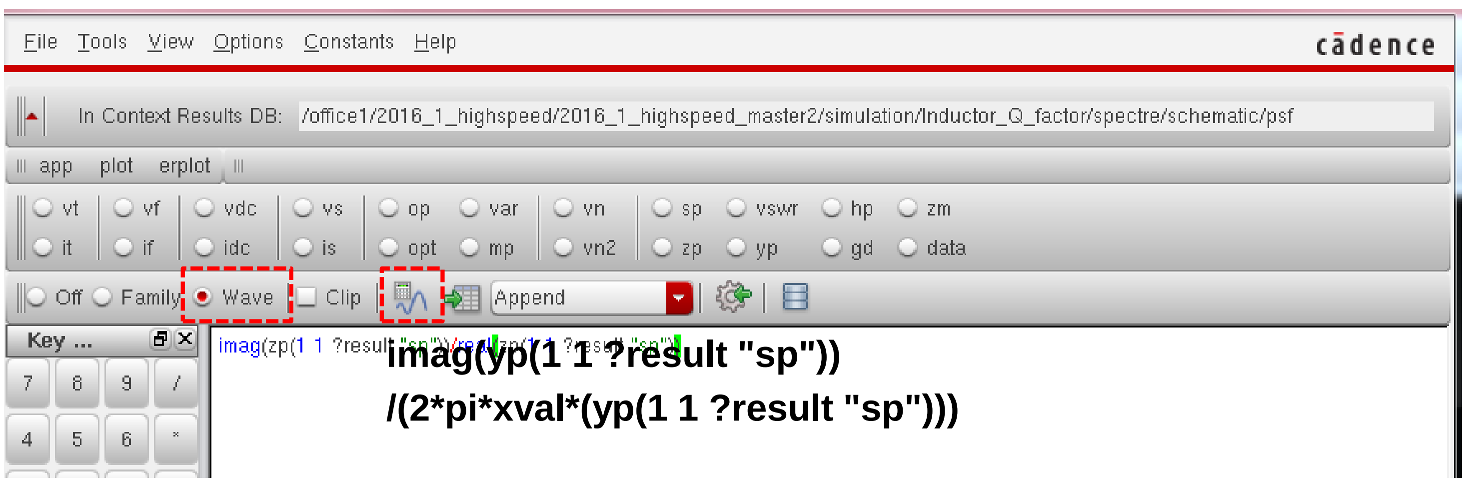


< Equivalent circuit of varactor >



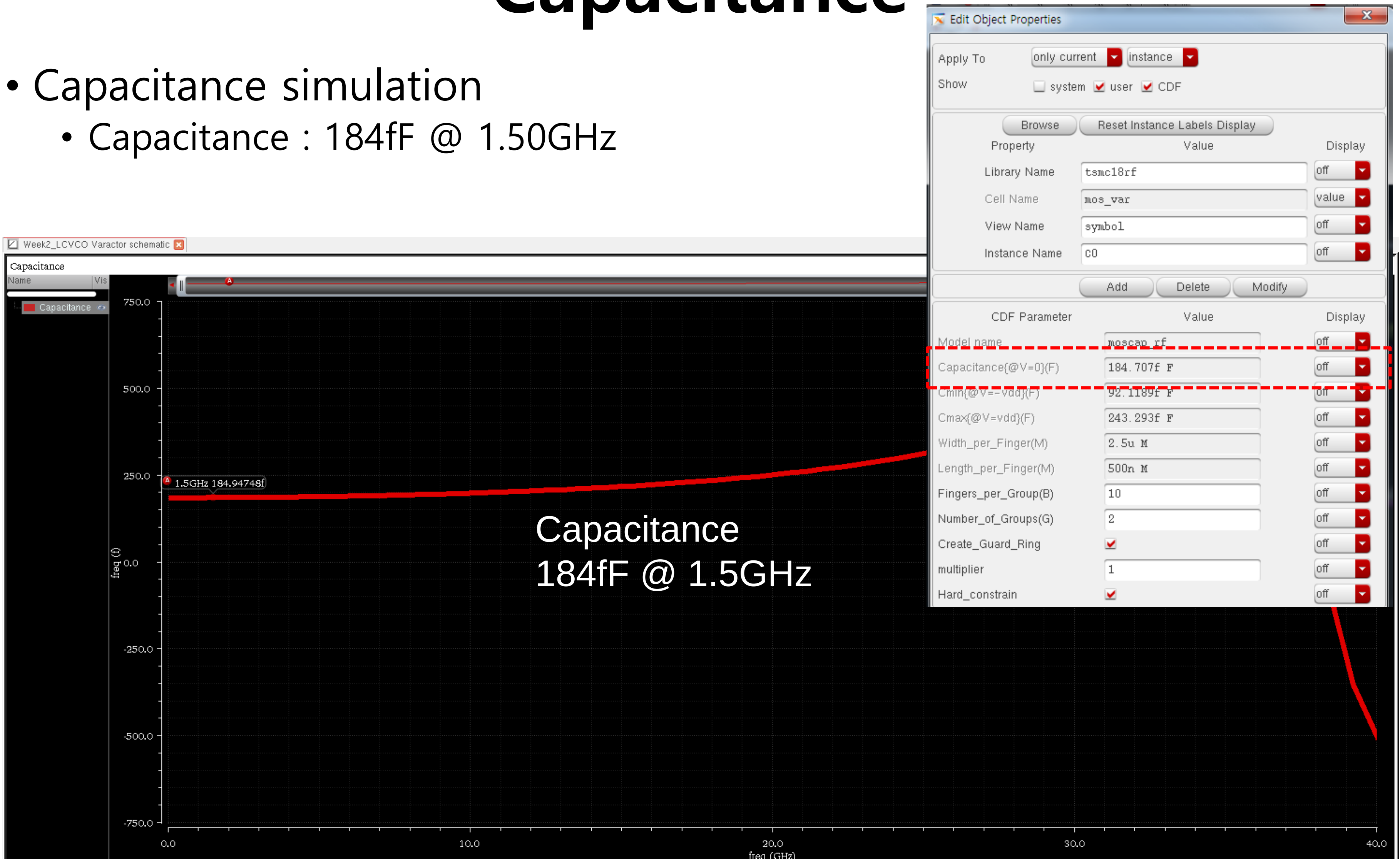
Capacitance

- Simulation condition setting
  - $C = \frac{\omega C}{\omega} = \frac{Imag[Y11]}{\omega}$
  - Calculator (Visualization & Analysis XL)
  - Wave choice → imag(yp(1 1 ?result "sp")) /(2*pi*xval(yp(1 1 ?result "sp")))



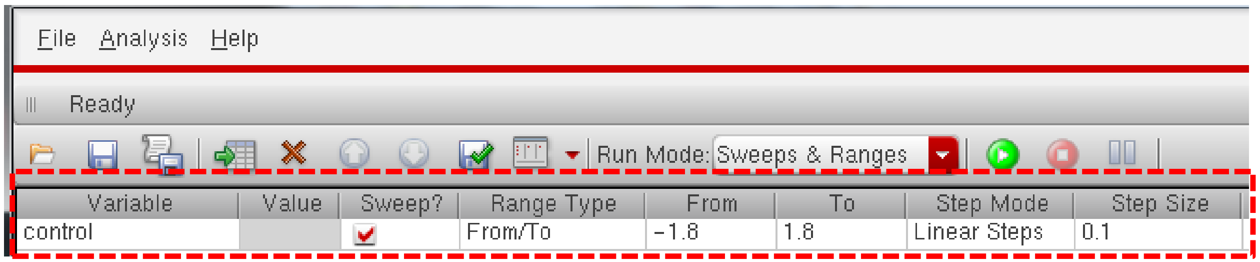
Capacitance

- Capacitance simulation
  - Capacitance : 184fF @ 1.50GHz

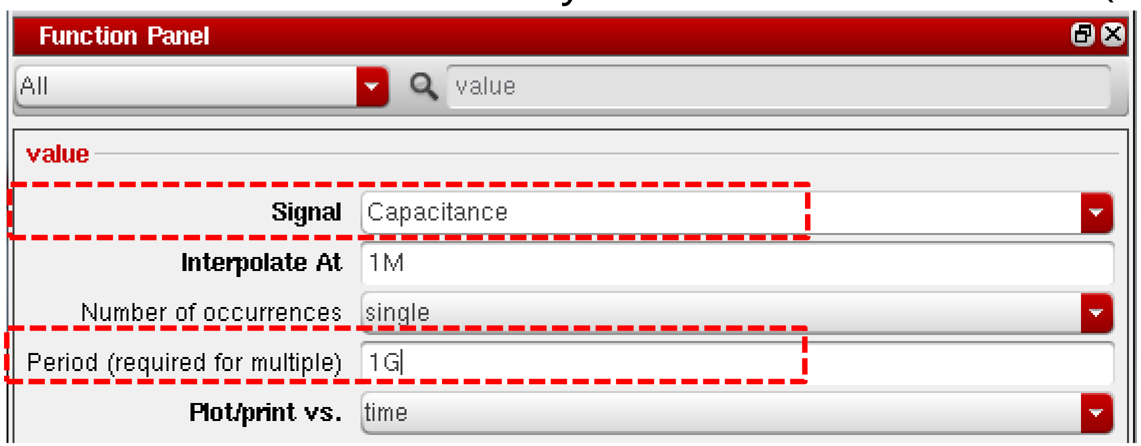


Capacitance

- Control voltage sweep
  - Tools → Parametric Analysis
    - Voltage : -1.8V ~ 1.8V

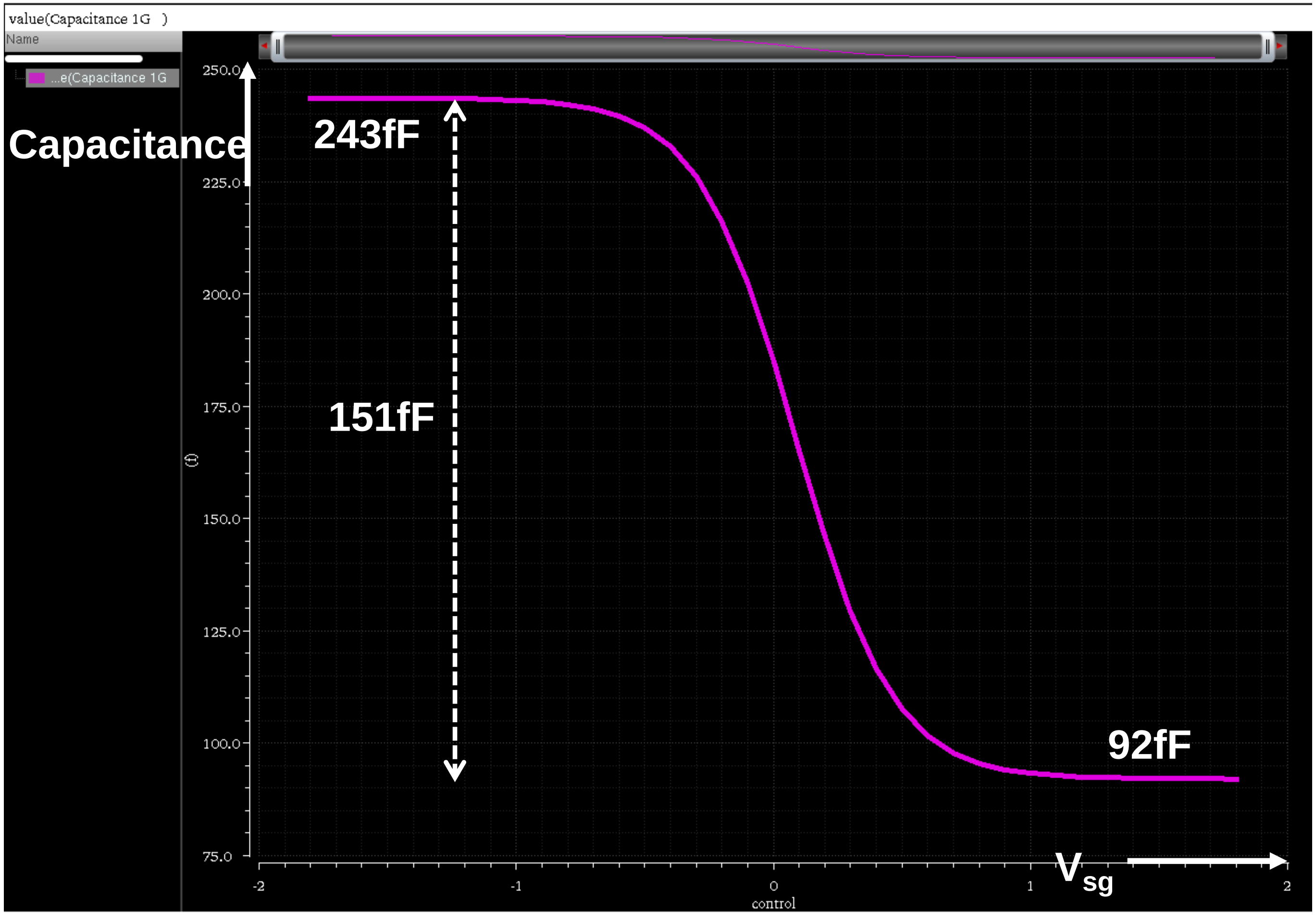


  - Calculator → Family → value → 파형 선택 (Capacitance) → Plot



Capacitance

- V_{SG} VS Capacitance

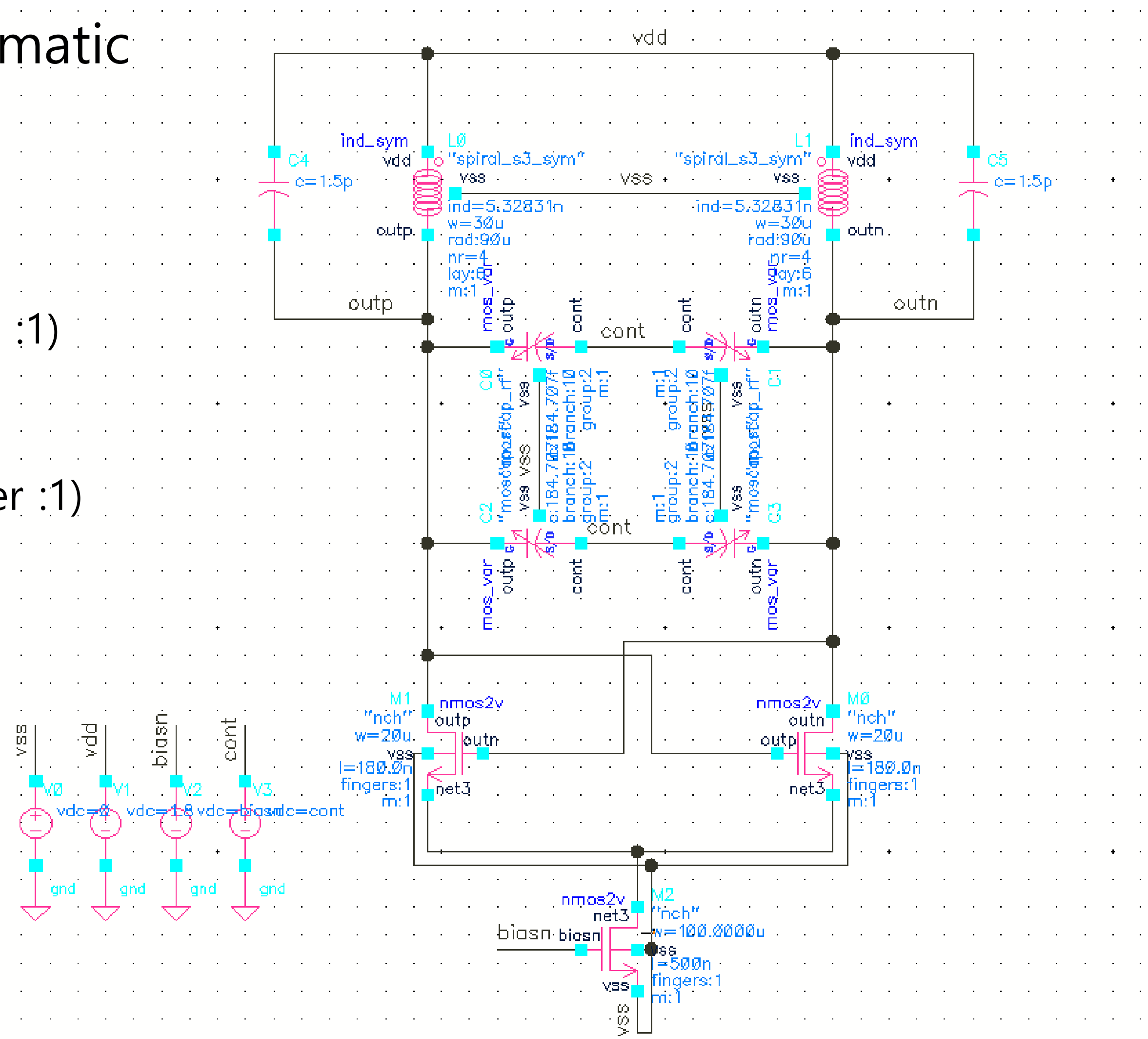


High-Speed Circuits and Systems Lab., Yonsei University

LC VCO Schematic

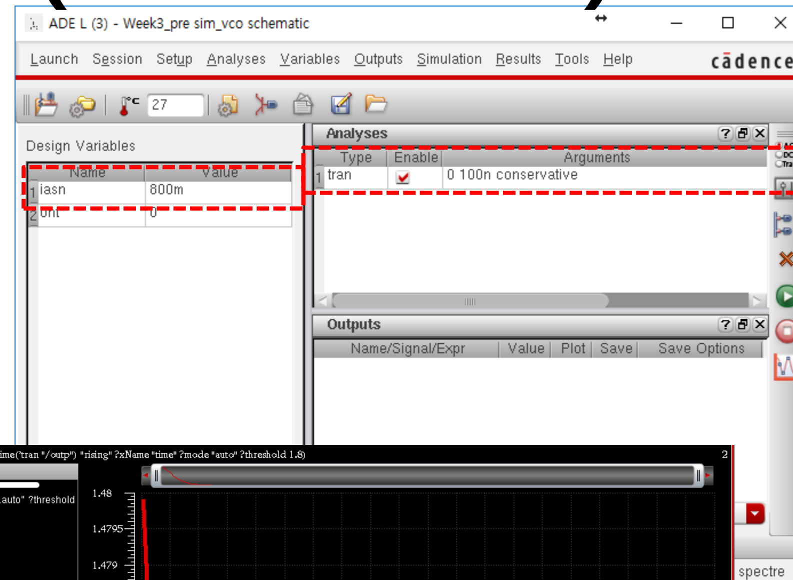
- Simulation LC VCO schematic
  - Inductor : 5.42nH
  - Capacitor : 1.5pF
  - Input NMOS
    - Length : 180n
    - Total Width : 20u (finger :1)
  - Source NMOS
    - Length : 500n
    - Total Width : 100u (finger :1)
  - Varactor
  - vdd : 1.8V
  - biasn : 0.8V
  - cont : 변수 지정 (cont)

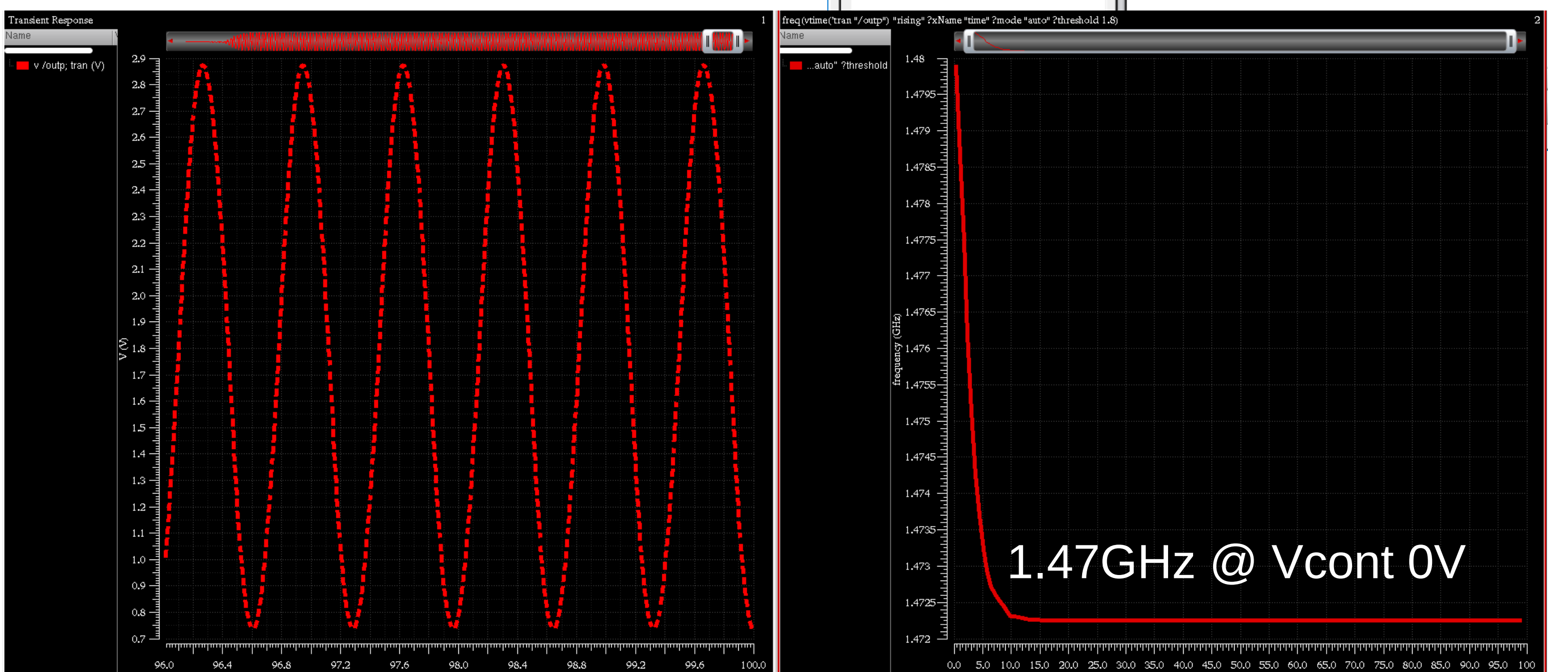
  - Initial condition
    outp & outn
    :1.8V, 1.85V



OSC Frequency (Vcont = 0V)

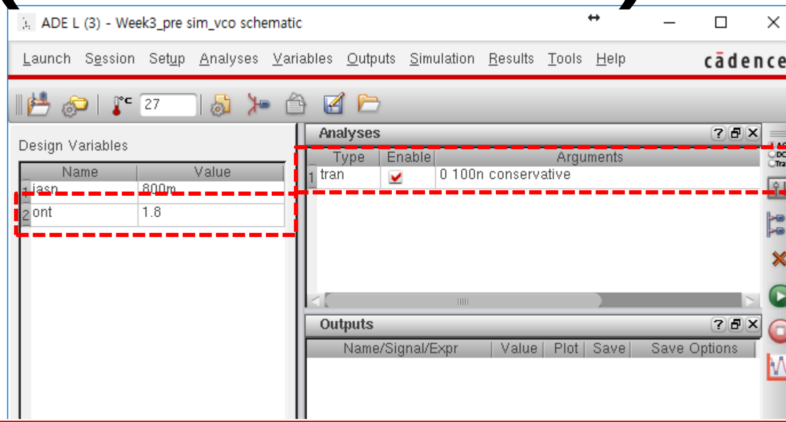
- Control Voltage 0V
  - OSC frequency : 1.36GHz
  - Transient simulation (100ns)
  - Output 파형 및 Frequency 측정

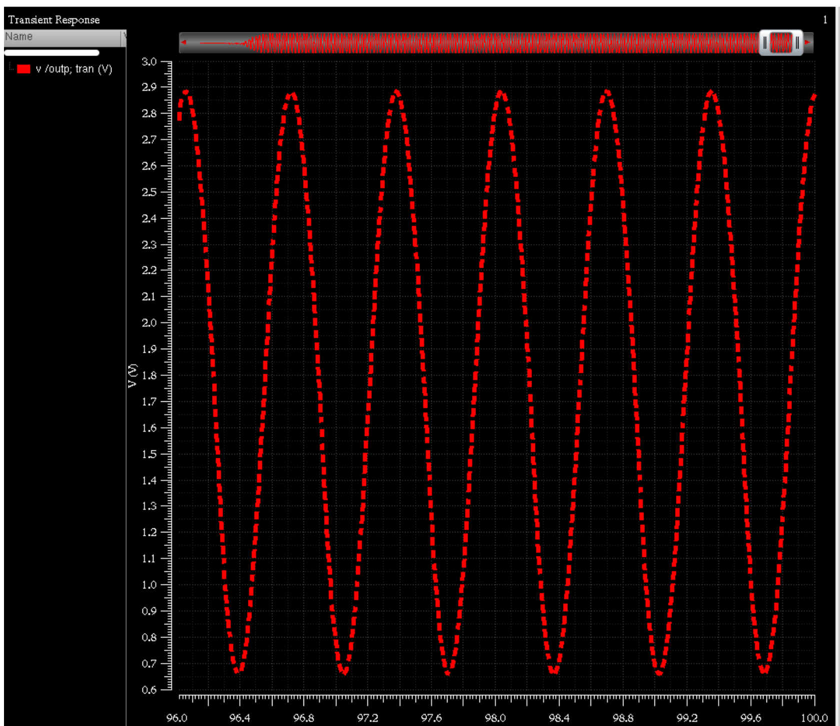


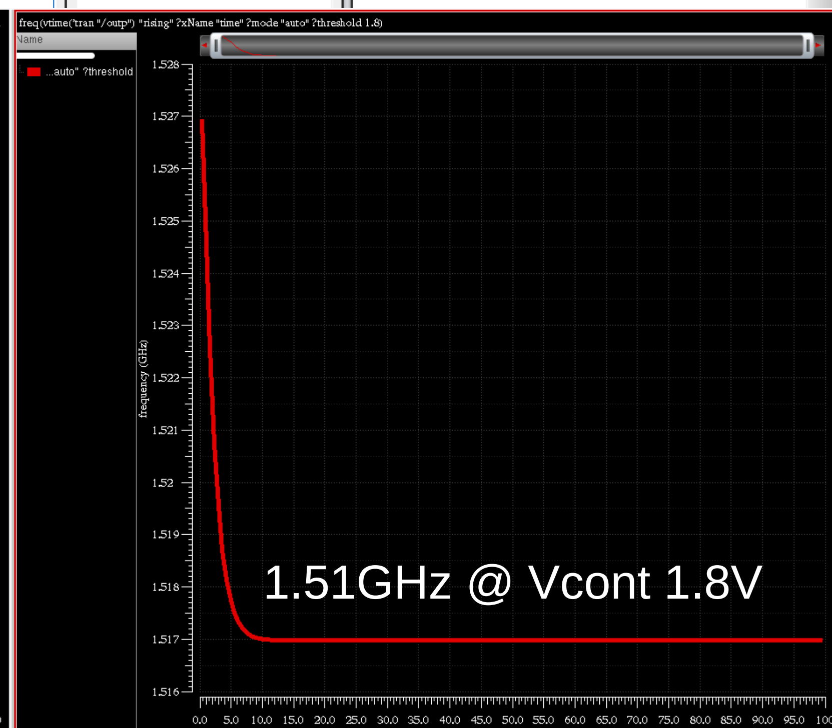


OSC Frequency (Vcont = 1.8V)

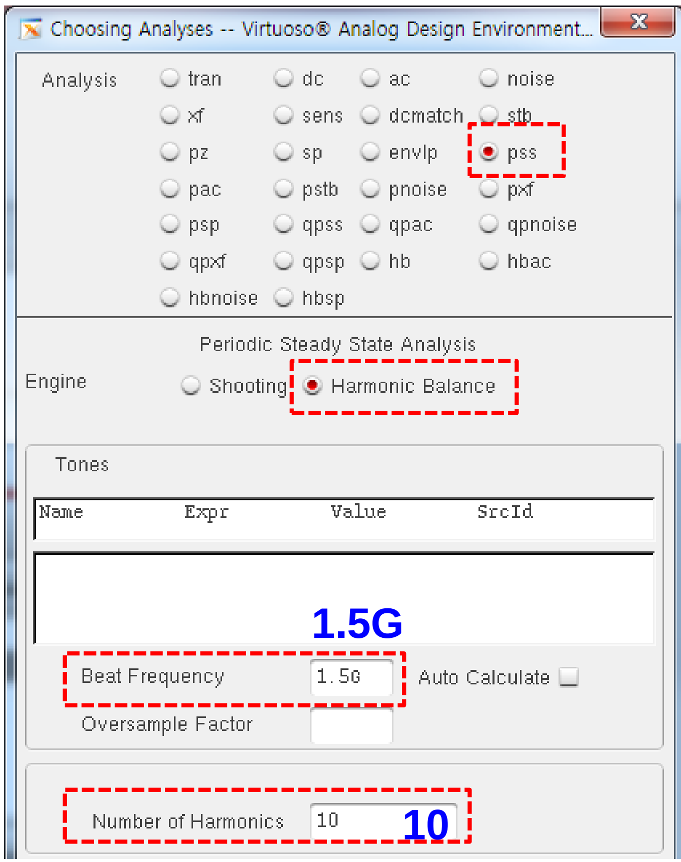
- Control Voltage 1.8V
  - OSC frequency : 1.36GHz
  - Transient simulation (100ns)
  - Output 파형 및 Frequency 측정

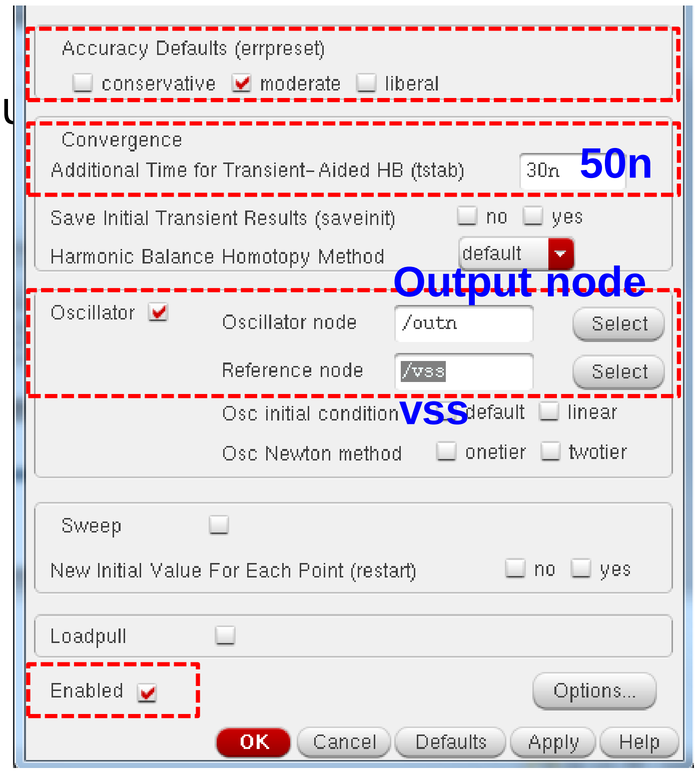






Phase Noise (PSS)

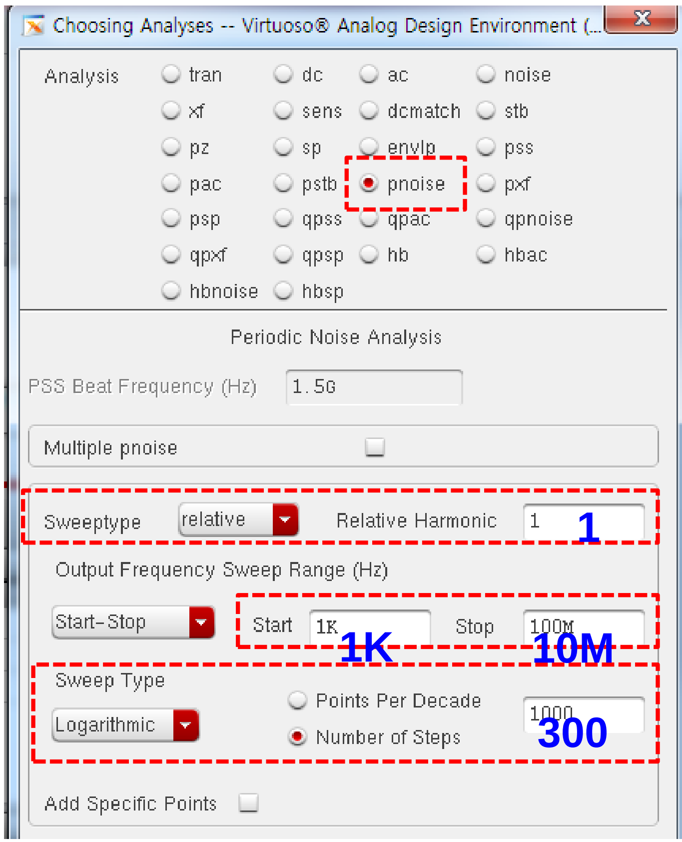


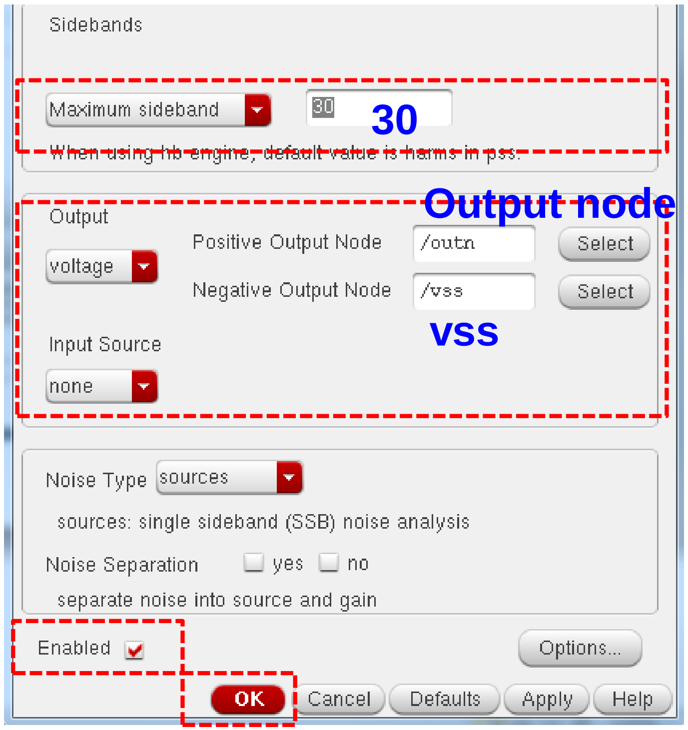


tstab : Oscillation
안정 구간 설정

Phase Noise (Pnoise)

- Pnoise
  - Setup PSS first, then Pnoise

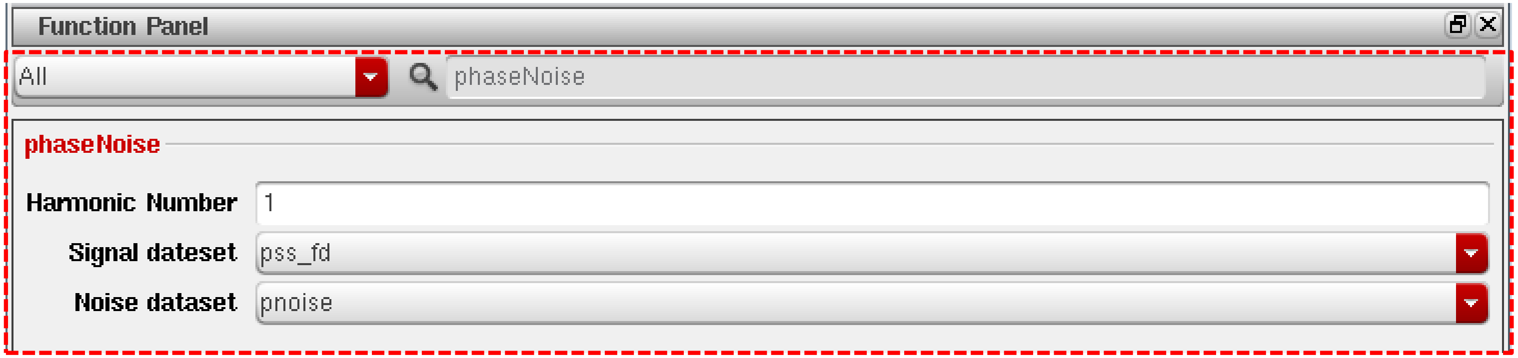




Output : Voltage 설정
Output Node 설정
Input : none

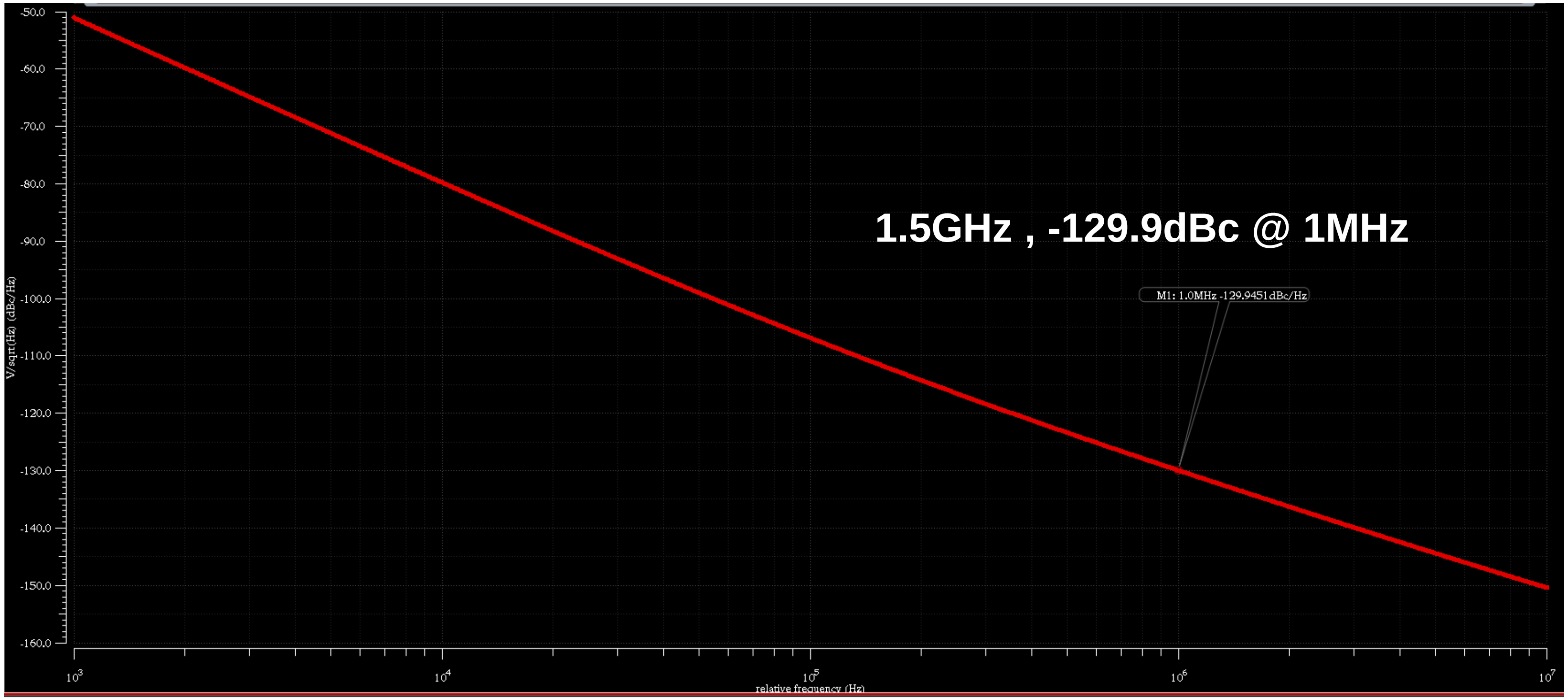
Phase Noise

- Phase noise
  - Calculator (Visualization & Analysis XL)
  - Function Panel (phaseNoise 입력)
    - Harmonic Number : 1
    - Signal dataset : pss_fd
    - Noise dataset : pnoise
  - Apply



Phase Noise

- Phase noise
  - V_{cont} = 1.48V
  - 1.5GHz, -129.9dBc @ 1MHz



Homework

- ✓ Design 2-GHz (±100MHz) LC VCO with tuning range larger than 100MHz

- ✓ Verify and plot output waveforms and K_{VCO}.
- ✓ Verify and plot phase noise with control voltage generating 2-GHz clock.
- ✓ Indicate LC VCO schematic, inductor and capacitor value, and using varactor count in the report.

- ✓ LC VCO specification
  - -Supply voltage : 1.8V
  - -Load capacitance: 1.5 pF
  - -Phase noise : Min -115dBc/Hz
  - -Frequency tuning range : Min 100MHz

- ✓ Due: 25 Sep. in class (Hardcopy)