High-Speed Serial Interface Circuits and Systems

Lect. 1 – Introduction

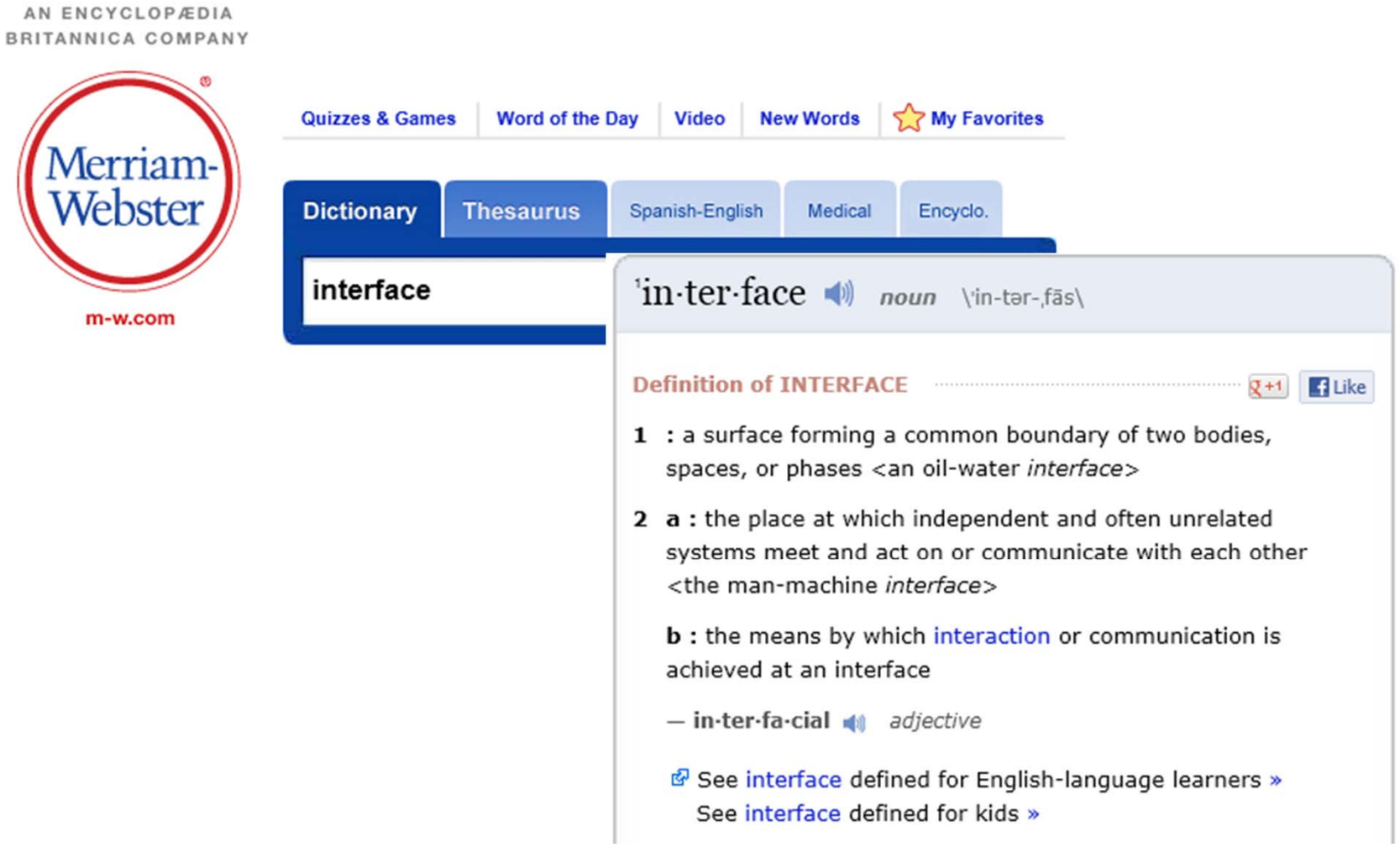
● Lecturer: Prof. Woo-Young Choi (최우영)
Room: B625, Tel: 02-2123-2874
Email: wchoi@yonsei.ac.kr, Web: tera.yonsei.ac.kr

● TA: Minkyu Kim (김민규)
Room: B629, Tel: 02-2123-7709
Email: minkyu226@gmail.com

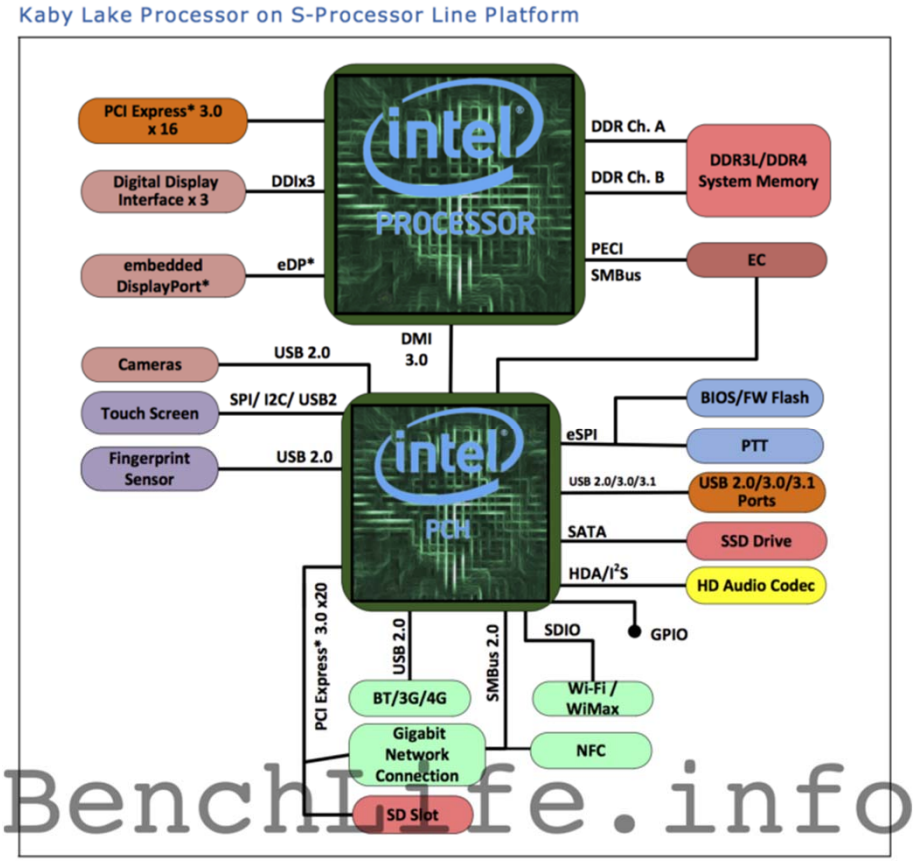
● Goals
- Introduction to high-speed serial interface circuits and systems
- Design practice for high-speed serial interface circuits

● Prerequisite
- Solid background in electronic engineering
- Proficiency in CMOS electronic circuit design

High-Speed Serial *Interface*



Interfaces inside Desktop Computers



PCH: Platform Controller Hub

DMI: Direct Media Interface

Interface between CPU and PCH

DDR: Double Data Rate

DDR4: 17GB/s ~ 25.6 GB/s

DDR5: Double bandwidth of DDR4

PCIe: Peripheral Component Interconnect Express

Interface for video card, network card, etc

PCIe 3.0: 8GT/s per lane

➔ 7.877Gb/s per lane with 128b/130b coding

USB: Universal Serial Bus

USB 2.0 : 480 Mb/s

USB 3.0: 5 Gb/s

USB 3.1 10 Gb/s

SATA: Serial Advanced Technology Attachment

SATA 3.0: 6 Gb/s

SATA 3.2: 16 Gb/s

Interfaces inside Smartphone

mipi: Mobile Industry Processor Interface

D-PHY: 80Mbs to 1Gbps, no symbol coding, no CDR
M-PHY: up to 5Gbps, 8B10B, CDR

LLI: Low Latency Interface
SSIC: Super Speed InterChip
UniPort: Unified Protocol

UFS: Universal Flash Storage
DigRF: Digital RF

DSI: Display Serial Interface
CSI: Camera Serial Interface

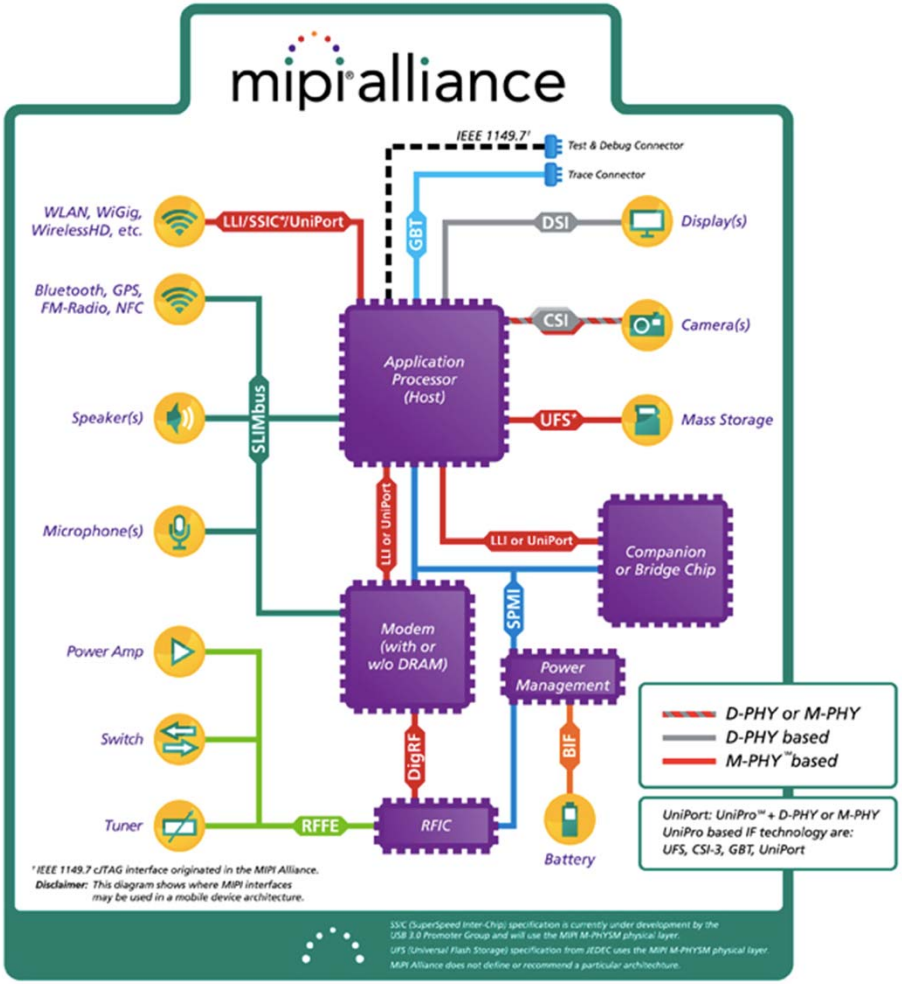
SLIMBus: Serial Low-Power Inter-Chip Media Bus

SPMI: System Power Management Interface

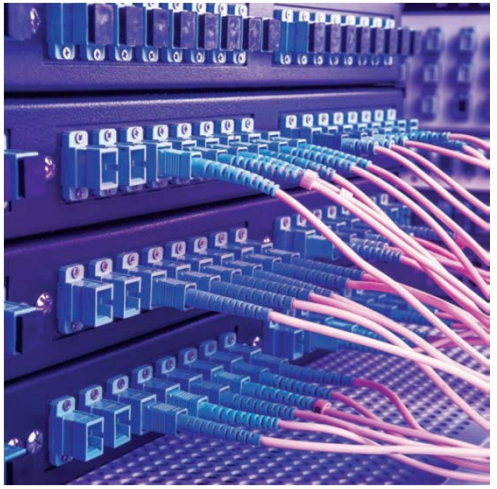
BIF: Battery Interface

GBT: Giga Bit Trace

RFFE: RF Front-End



Interfaces inside Data Centers



Several standards exist:

IEEE 802.3 (Ethernet)

OIF-CEI (Optical Internetworking Forum – Common Electrical Interface)

Fiber Channel

InfiniBand

Ethernet: 400G AUI-16, 26.5625 Gb/s NRZ x 16, Max 10cm (AUI: Attachment Unit Interface

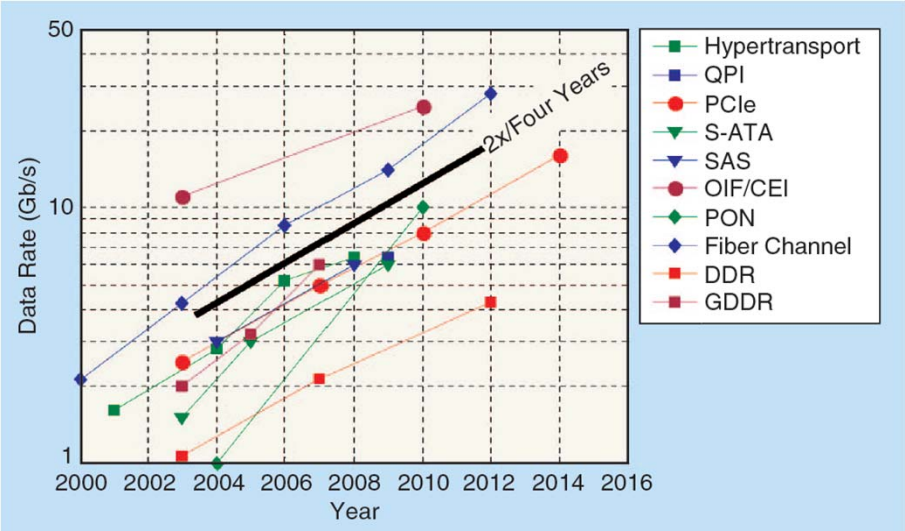
OIF-CEI: CEI-56G-VSR-NRZ, (VSR: Very Short Reach)

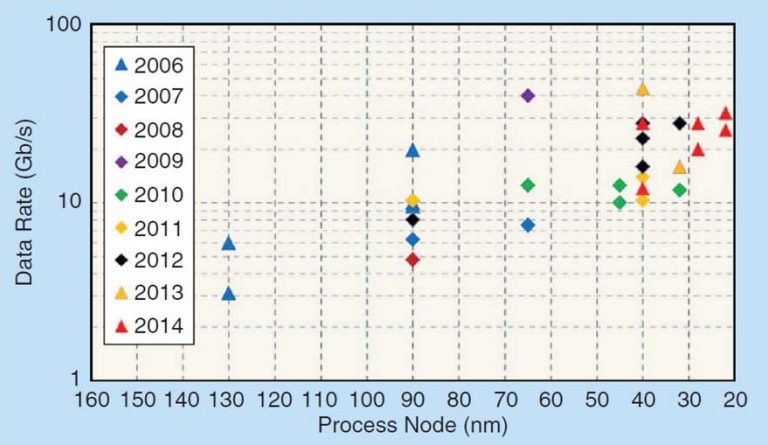
Fiber Channel: 256GFC*, 29.027 GBaud/s, PAM4, 4 lanes,

InfiniBand: 200G HDR, 26.5625 GBaud/s, PAM4, 4 lanes,

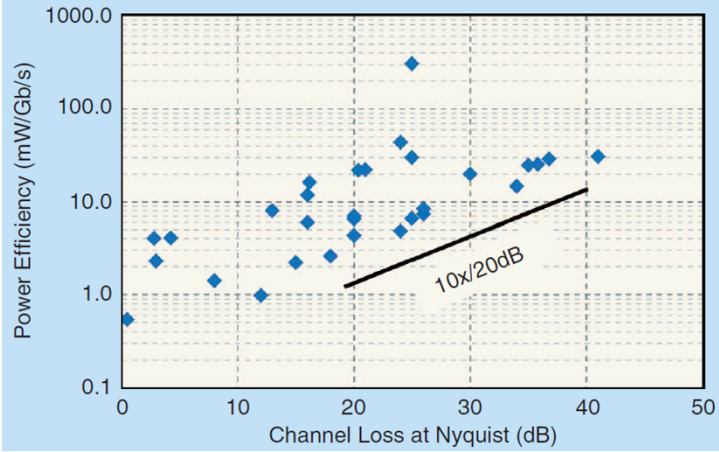
(Fom "Introduction to Digital I/O", IEEE Solid-Sate Circuits Magazine, Fall 2015)

Research Trends



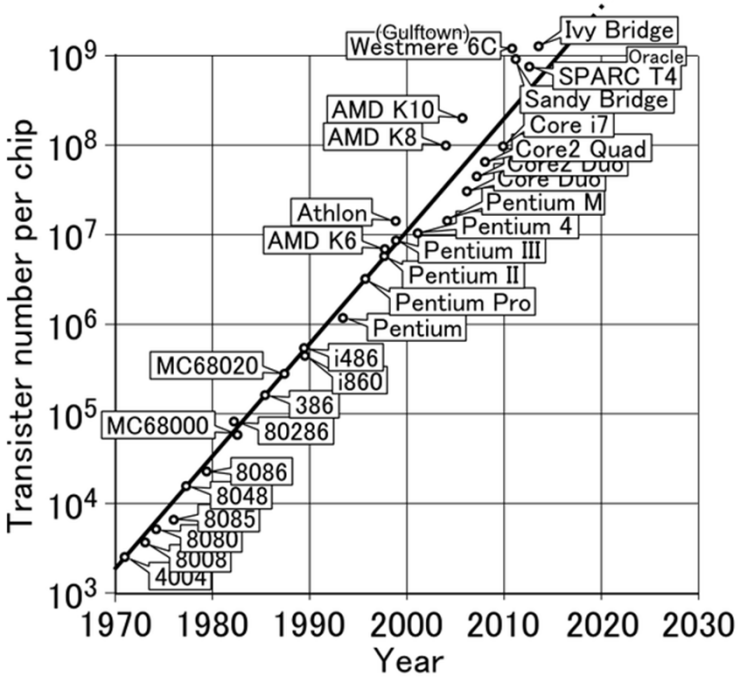


(Based on papers presented at ISSCC)

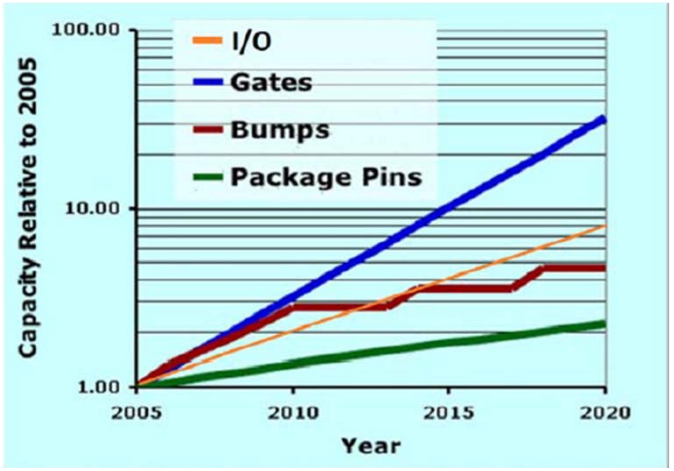


(Based on papers presented at ISSCC)

I/O Bottleneck



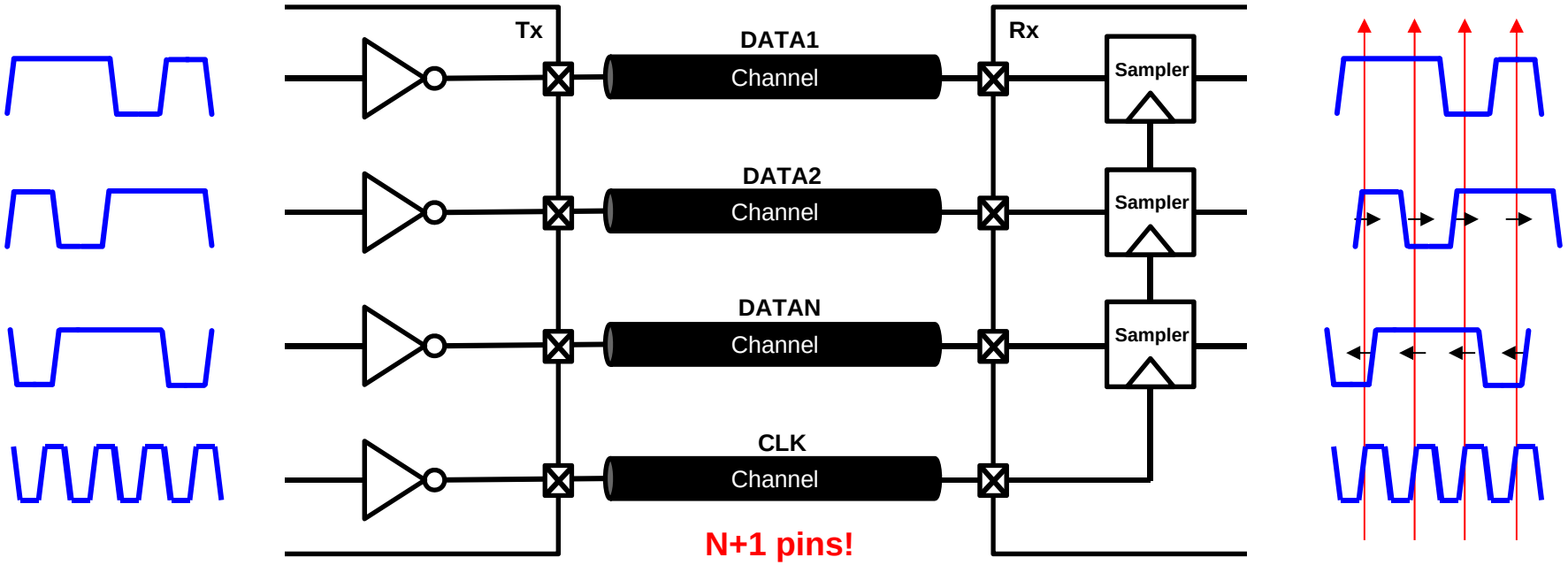
Moore's Law



Scaling of Gates, Bumps, Pins and I/O (Ref. Xilinx, I/O Line added)

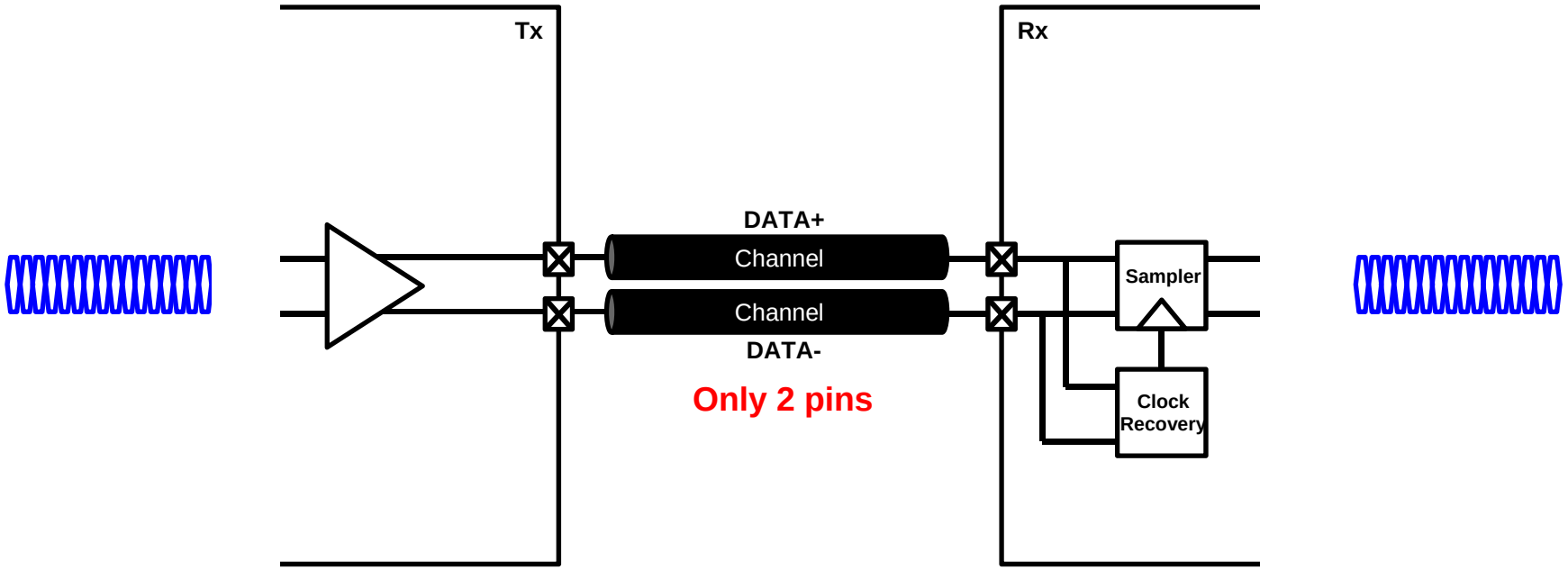
Why “serial”?

- Problems with parallel interface
  - Pin count / package / PCB wiring constraint
  - Skew



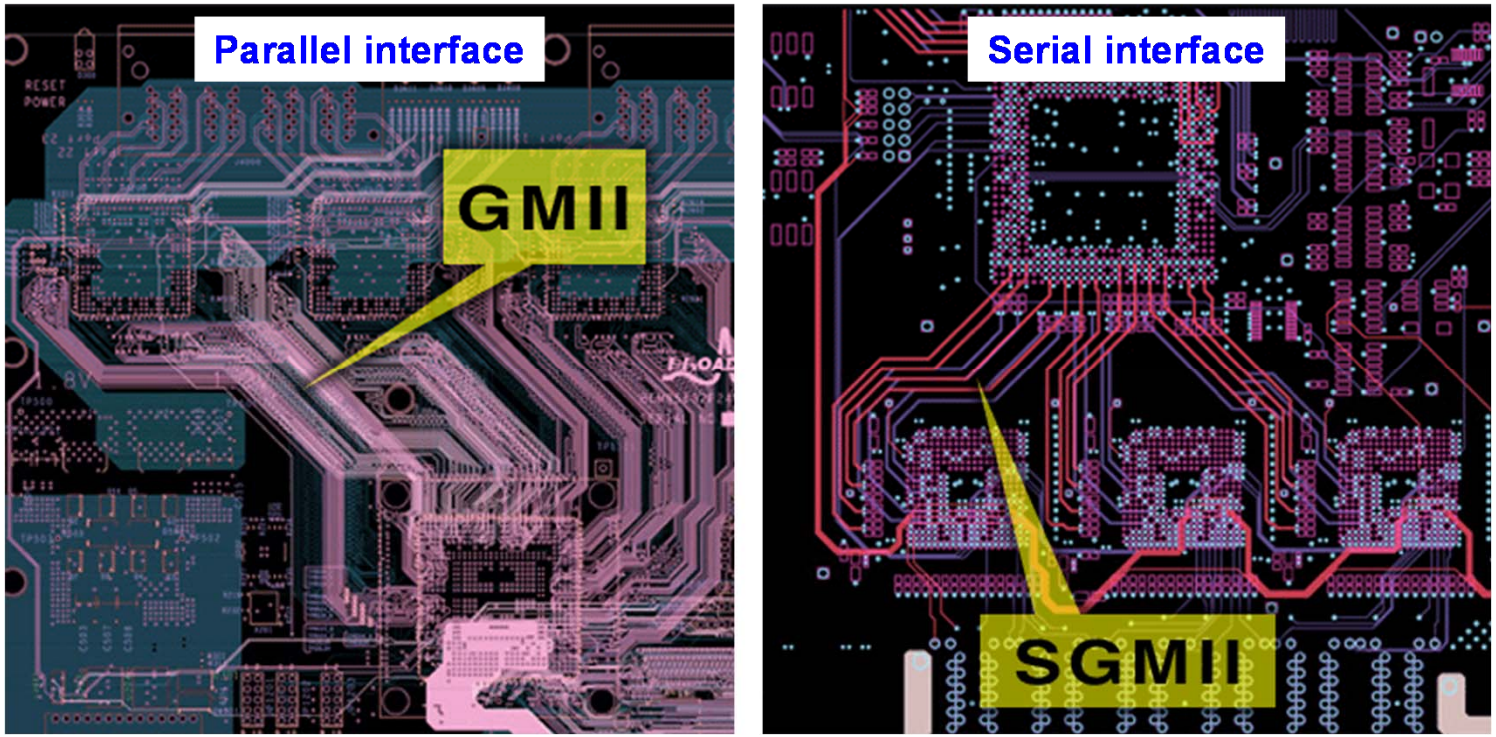
Why “serial”?

- Serial interface
  - To send only high-speed data / to recover clock in Rx side
  - No skew problem / only 2 pin count
  - Often differential signals for common-mode noise, supply noise rejection



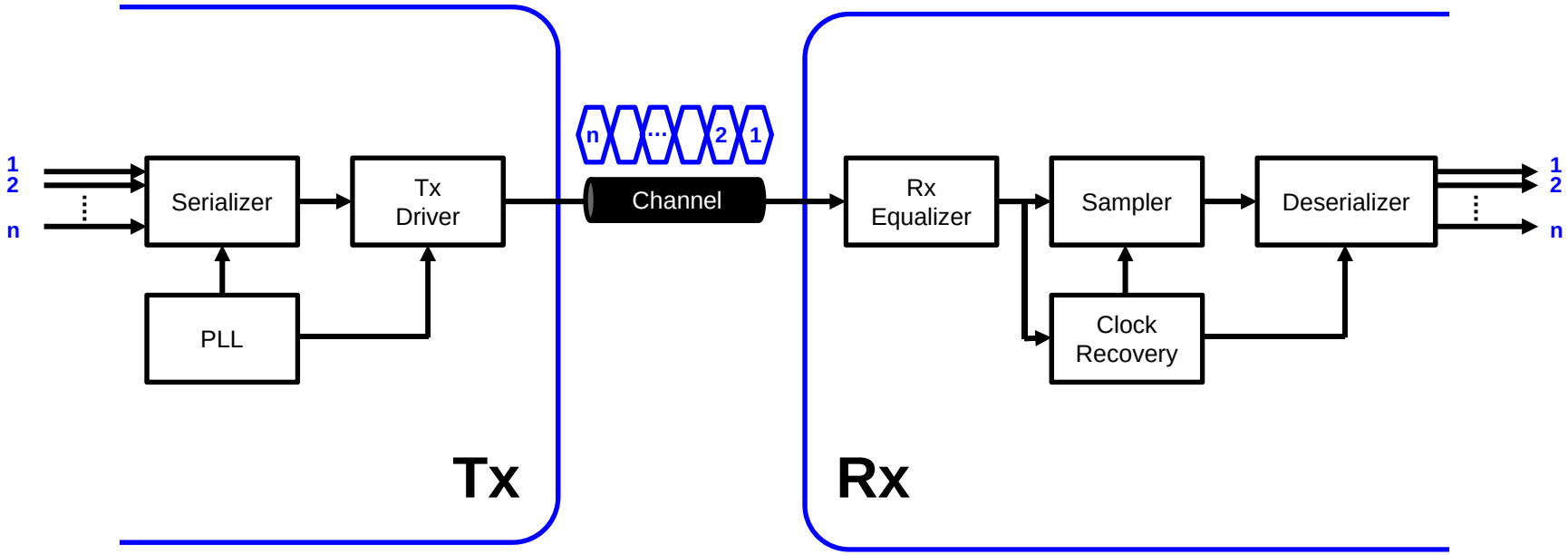
Why “serial”?

- Gigabit Media Independent Interface
- Reduced area, power, complexity → lower cost
- Reduced crosstalk, SSN, EMI → lower BER



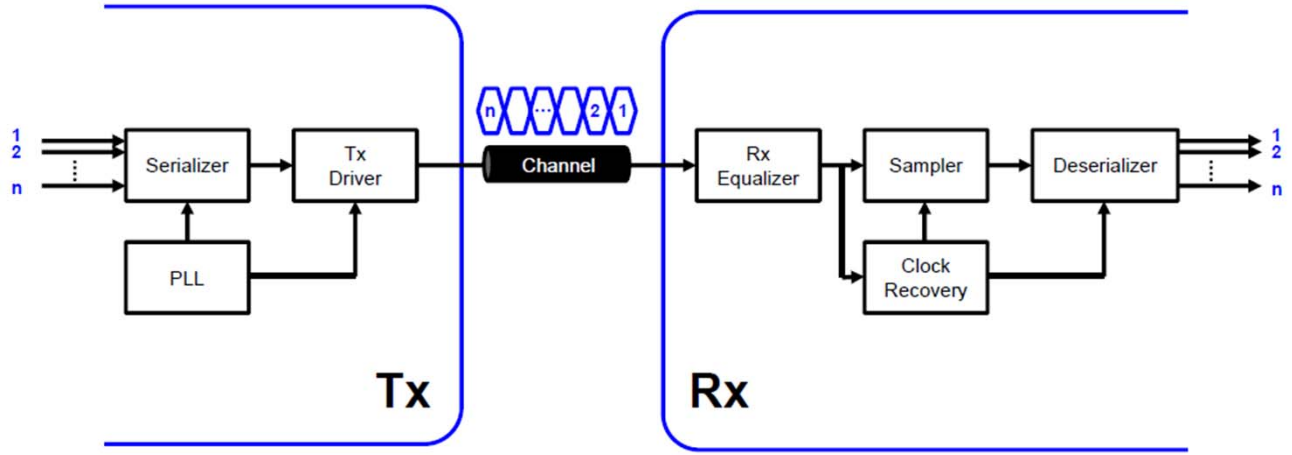
http://www.eetimes.com/design/communications-design/4142422/Going-Serial-in-Gigabit-Ethernet-Designs

Key Block Diagram



- High-speed interface
- High-speed digital I/O
- High-speed serdes (Serializer/Deserializer)

Key Block Diagram



Topics to be cover in this course
- PLL
- Tx Driver, Channel, Equalizer
- Serializer/Deserizer/CDR

References
- "Design of Integrated Circuits for Optical Communications" by Razavi
- Lecture notes for "High-Speed Links Circuits and Systems", Prof. Palermo, TAMU

- Grades
  - Tests (2, 30%)
  - Design Exercise (Almost every week, 30%)
  - Design Projects (2, 30%)
  - Attendance and class participation (10%)

- Mon.: Lecture on a topic
  Wed.: Design Exercise

➔ Class hour changes
Mon: 9:30 – 10:45 am (B701)
Wed: 9:30 – 10:45 am (A125)