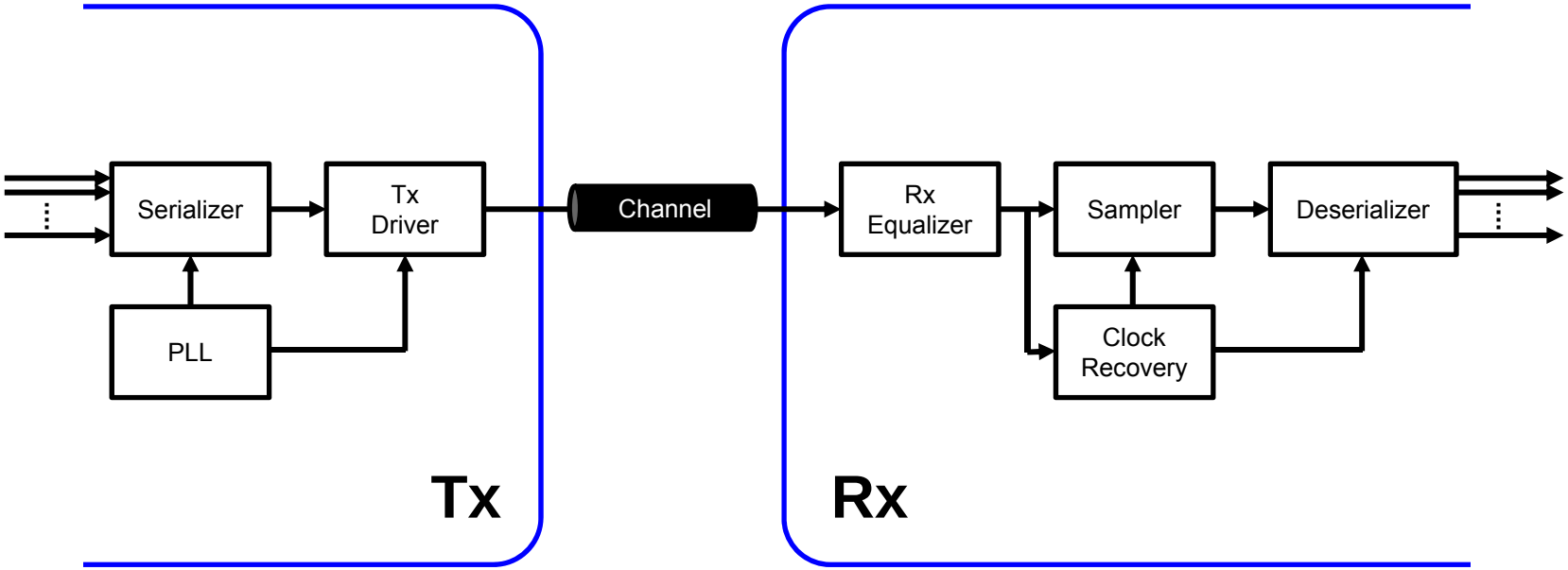
High-speed Serial Interface

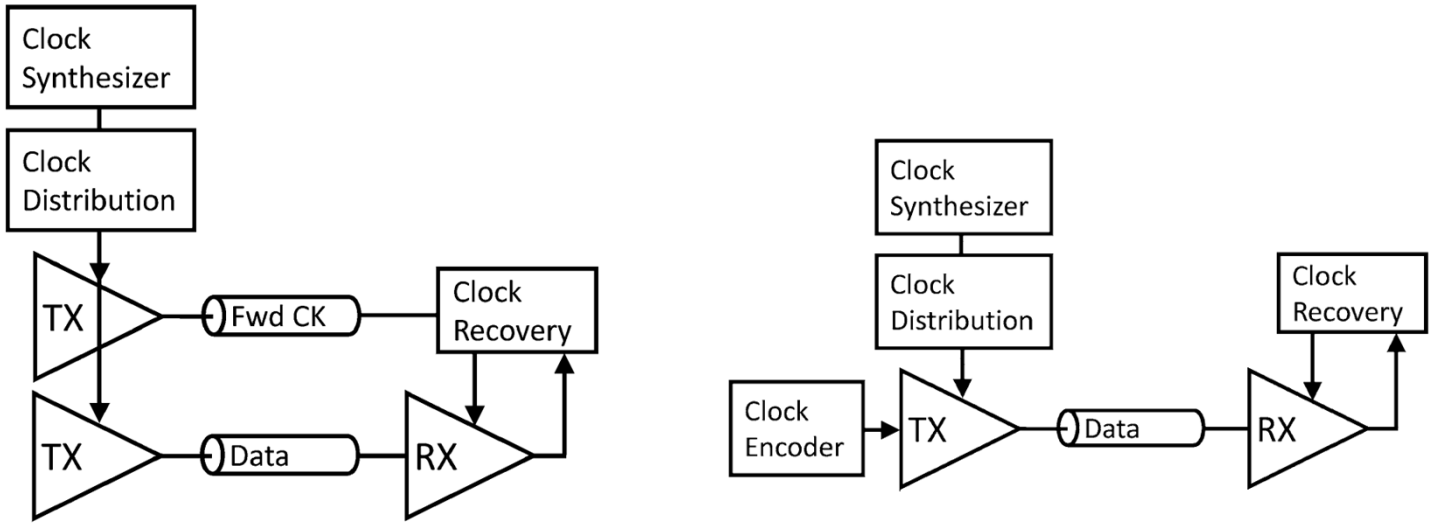
Lect. 10: Clock and Data Recovery

Block diagram



Clock Architecture for Interfaces

– Forwarded clocking vs. embedded clocking

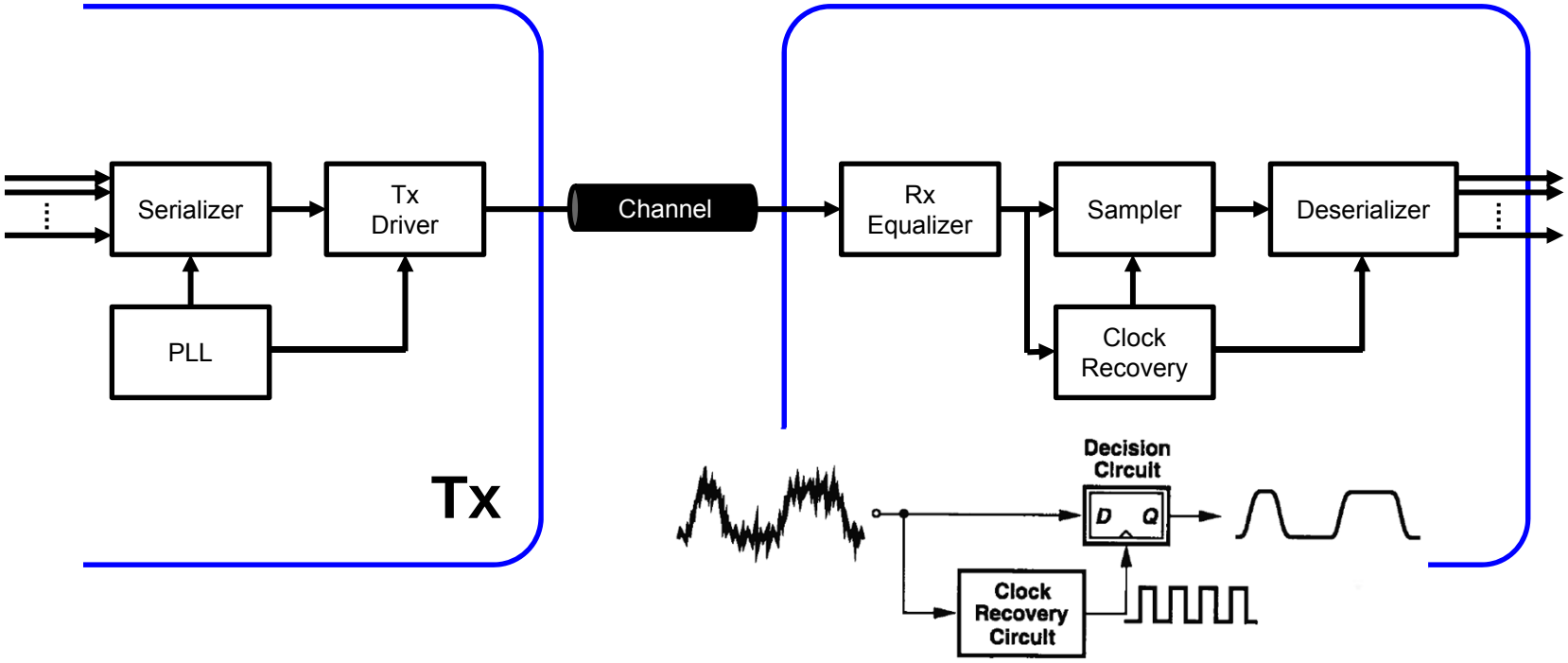


Bryan Casper - “Clocking Analysis, Implementation and Measurement Techniques for High-Speed Data Links—A Tutorial”, 2009 TCAS1

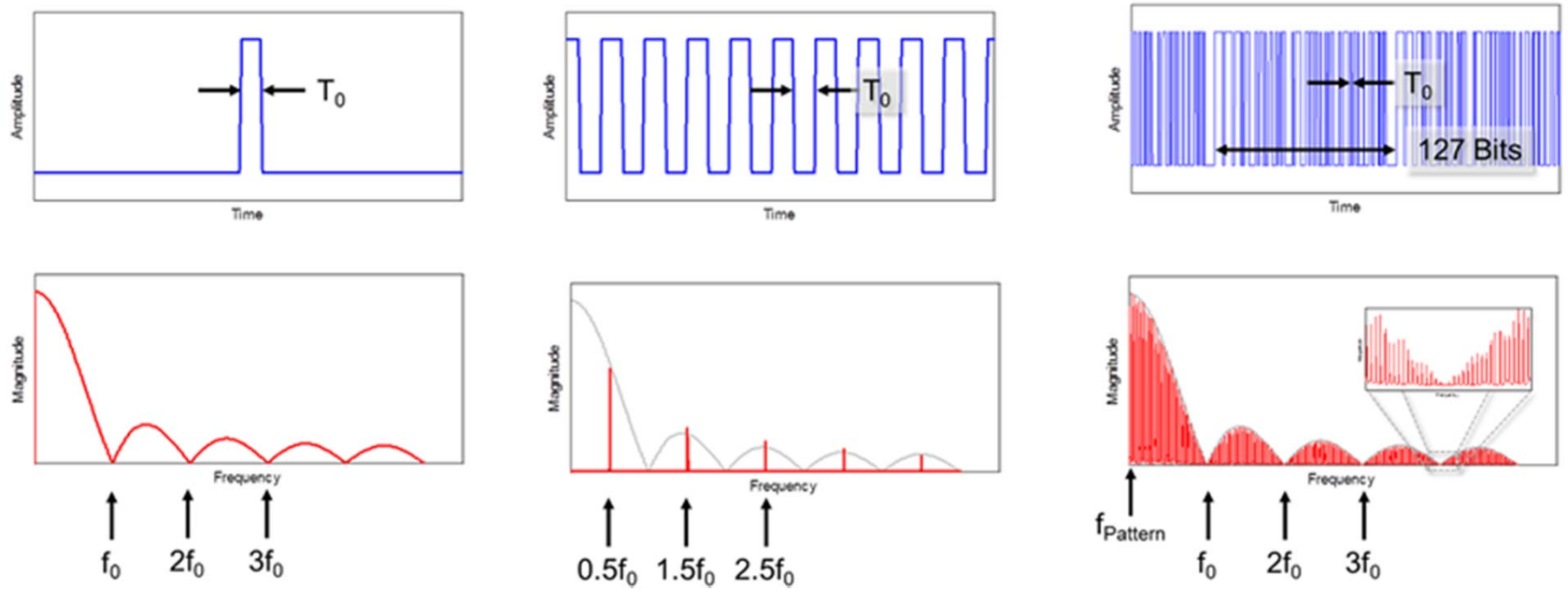
Clock signals in forwarded clocking are corrupted during transmission

Clock recovery is essential

Clock Data Recovery

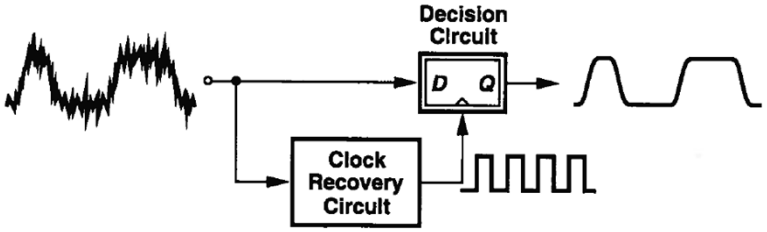


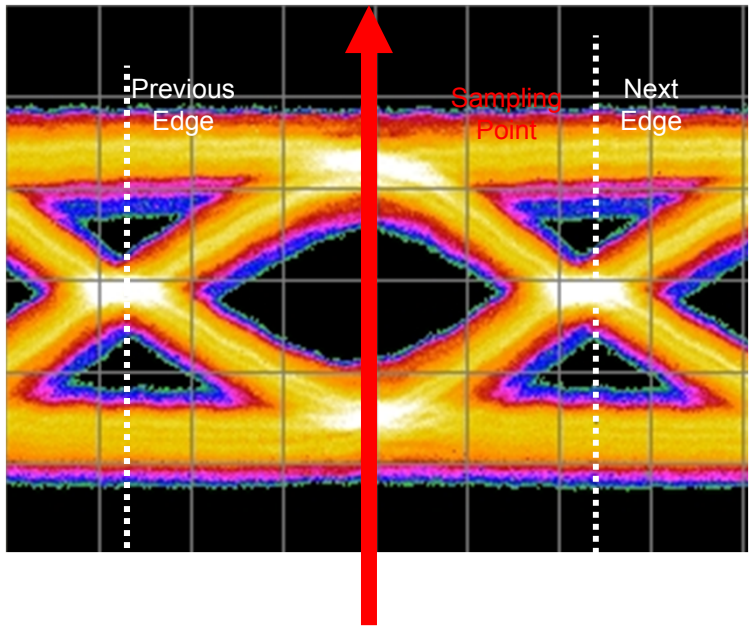
Spectra of NRZ data



- No spectral power at the clock frequency
- Simple filtering cannot provide clock frequency

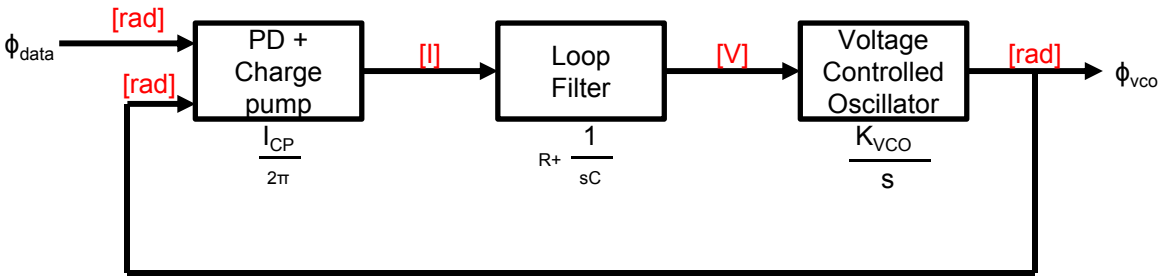
Phase of Recovered Clock





- Clock recovery based on edge detection
- Recovered clock phase should provide the best sampling point for lowest error probability
- Recovered clock and decision circuit should have small jitter

PLL-based CDR

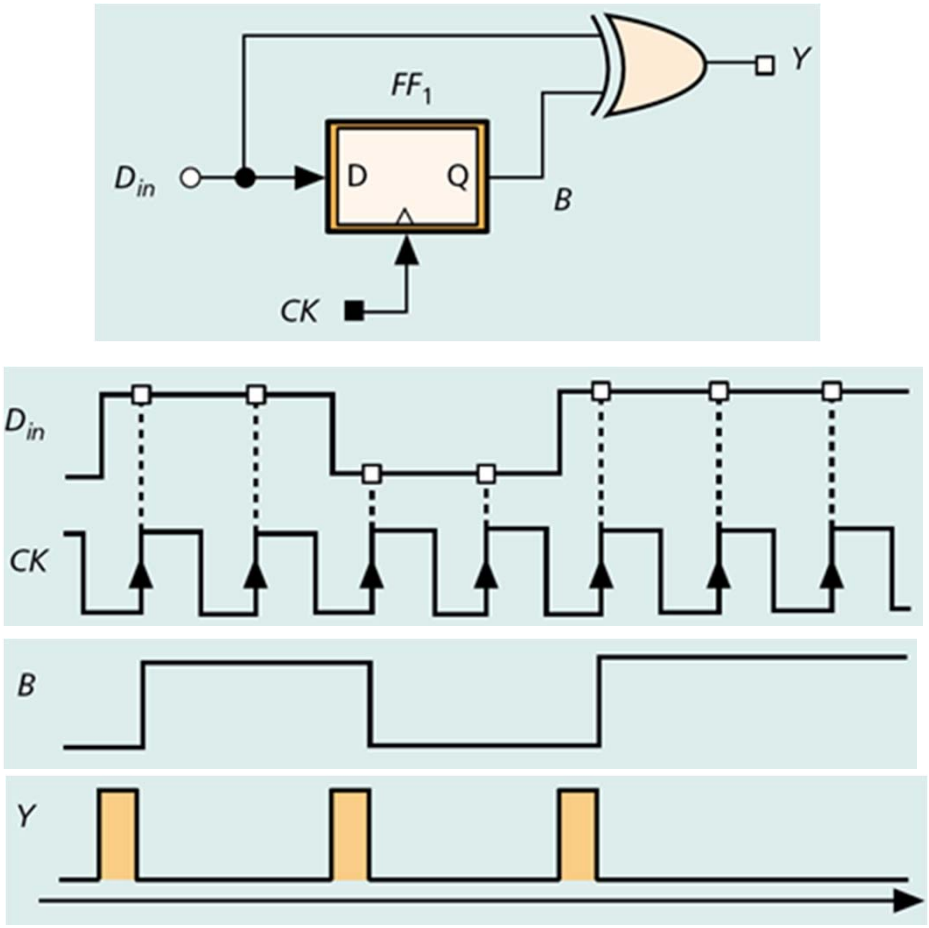


- Difference between PLL and CDR
  - PD input
    - PLL: Reference clock
    - CDR: Data
  - PD in CDR provides the phase difference between input data and the recovered clock
  - No divider

Phase detector

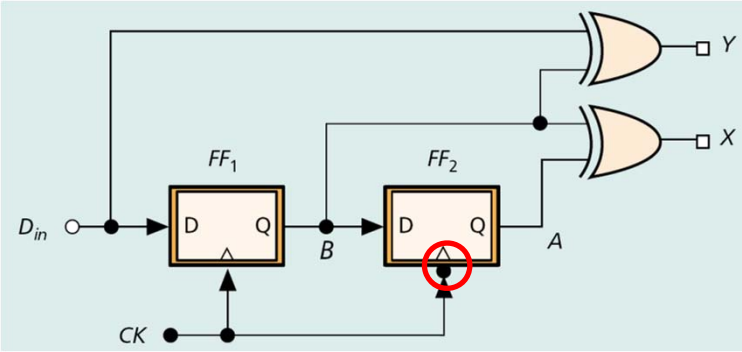
- Linear vs. Bang-Bang
  - Linear phase detector produces output proportional to phase difference ➔ PLL-like behavior
  - Bang-bang phase detector produces only UP or DN signal corresponding to the sign of phase error.

Phase Detector for CDR

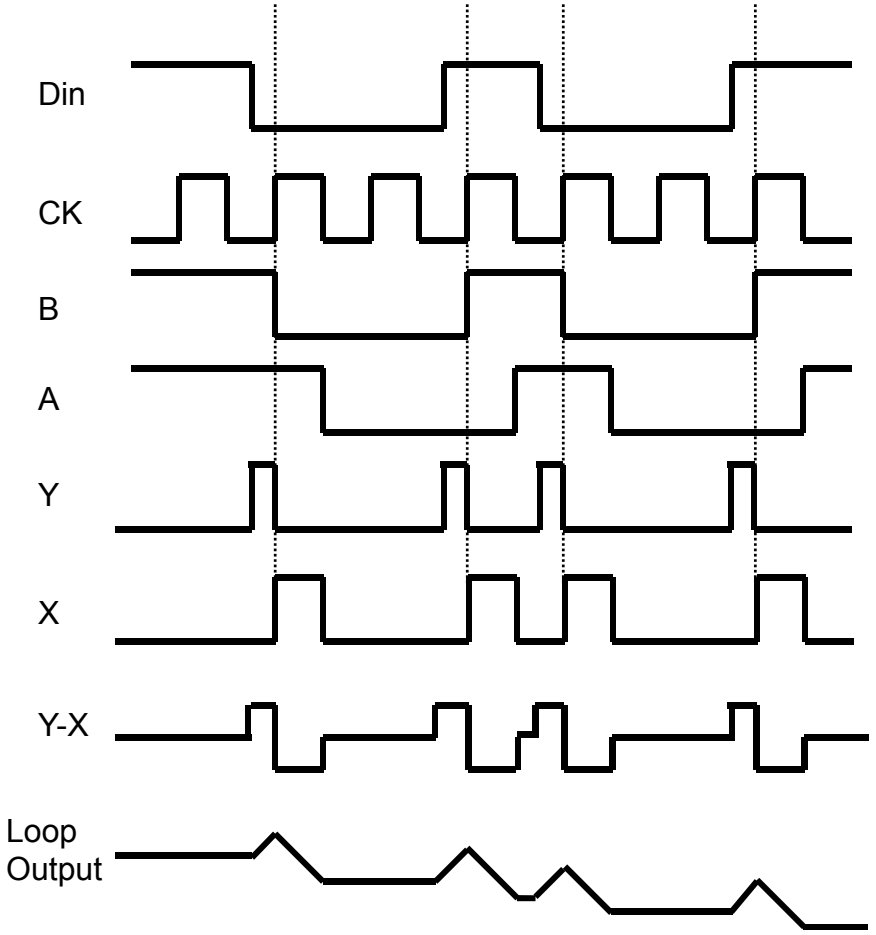


- PD only when there is data transition
- Duration of Y: Phase difference between clock and data transition
- However, Y is only positive and depends on transition density
- A reference value for Y?

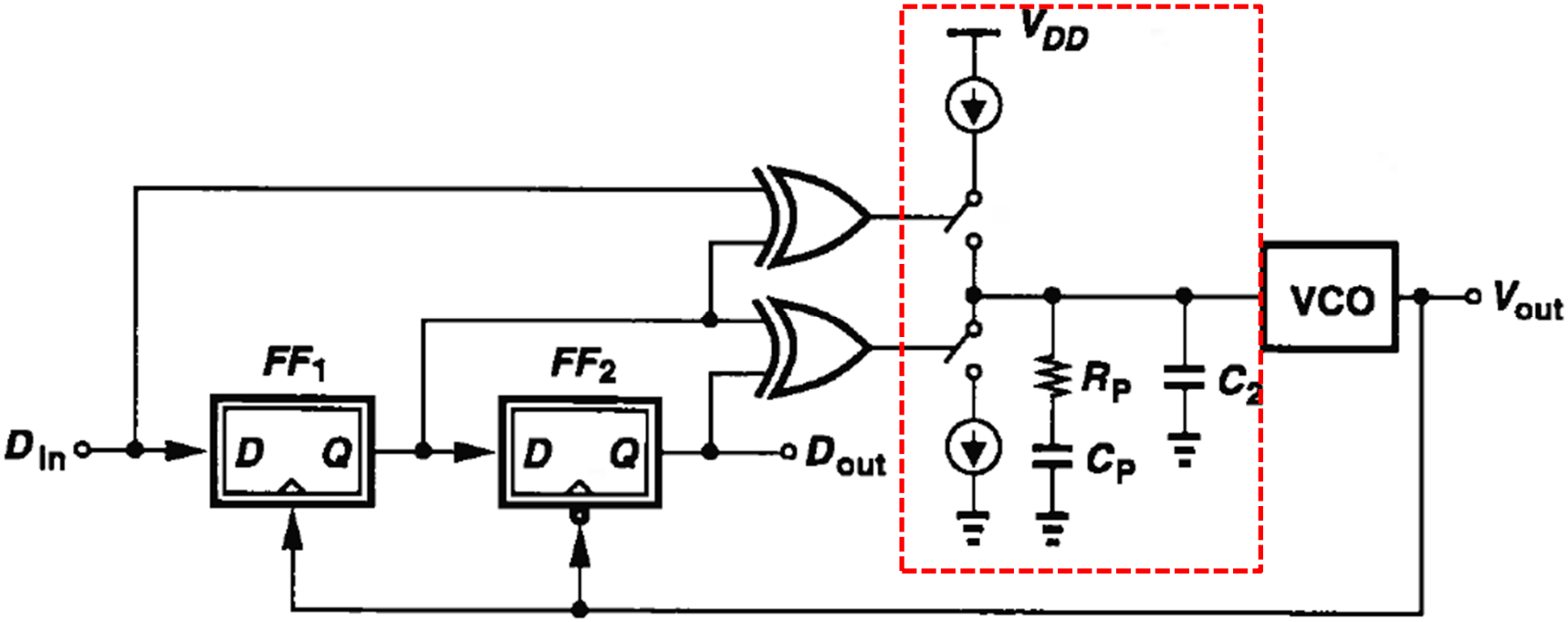
Hogge PD



- Y: Identical to XOR PD output
- X: Reference signal having duration of half the period when there is data transition
- Y used as Up and X as Dn for charge pump
- CK slows down until X and Y have the same duration
- Data are sampled at the optimal time and A and B provide recovered data



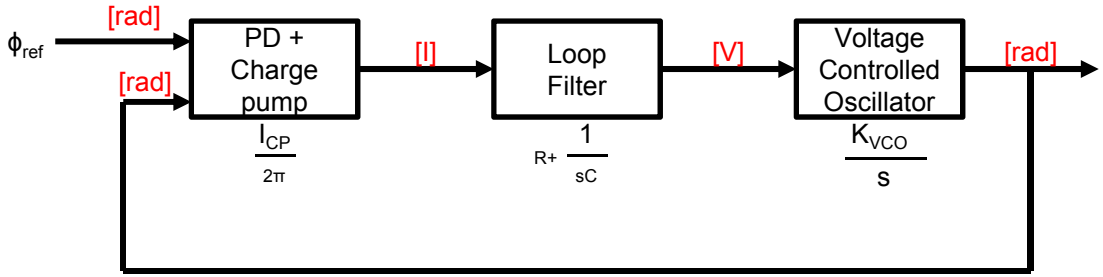
Hogge PD based CDR



- XOR outputs can directly drive the charge pump
- Need a relatively high-speed charge pump

CDR Dynamics

– Very Similar to PLL



$$T(s) = \frac{\alpha \frac{I_{cp}}{2\pi}\left(R + \frac{1}{sC}\right)\frac{K_{VCO}}{s}}{1 + \alpha \frac{I_{cp}}{2\pi}\left(R + \frac{1}{sC}\right)\frac{K_{VCO}}{s}} = \frac{\frac{\alpha I_{cp}(sRC+1)K_{VCO}}{2\pi C}}{s^2 + \frac{\alpha I_{cp} R K_{VCO}}{2\pi M}s + \frac{\alpha I_{cp} K_{VCO}}{2\pi C}}$$

– α represents data transition density

➔ CDR dynamics depends on data pattern

Limitation of Hogge PD

- For high-speed application, reliable realization of Hogge (Linear) PD becomes challenging
  - Short pulses for representing phase differences

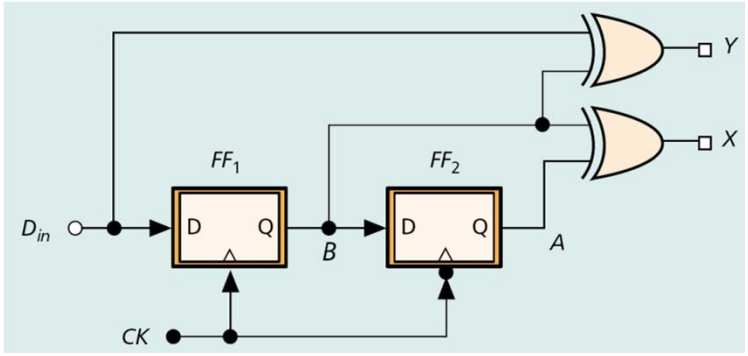
  ➔ XOR has to be fast

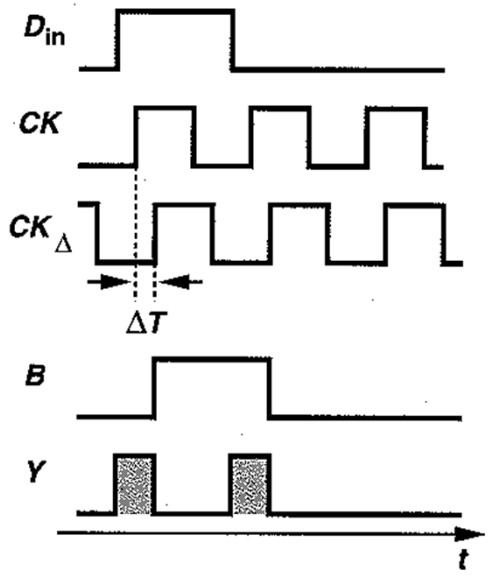
  Otherwise, distorted pulse shapes

  - When locked, charge pump output voltage becomes triangular wave

Limitation of Hogge PD

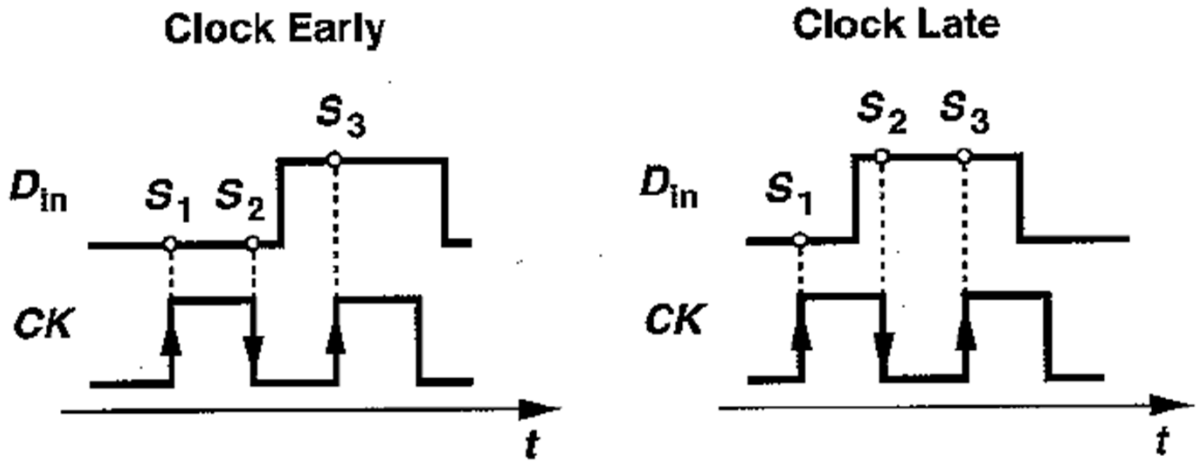
- For high-speed application, reliable realization of Hogge (Linear) PD becomes challenging
  - Static phase offset
    - Clk-to-Q delay (ΔT) for FF1 results in wider Y ➔ phase offset





Bang-Bang Phase detector

– Determine whether there is data transition and whether clock is early or late by three consecutive sampling

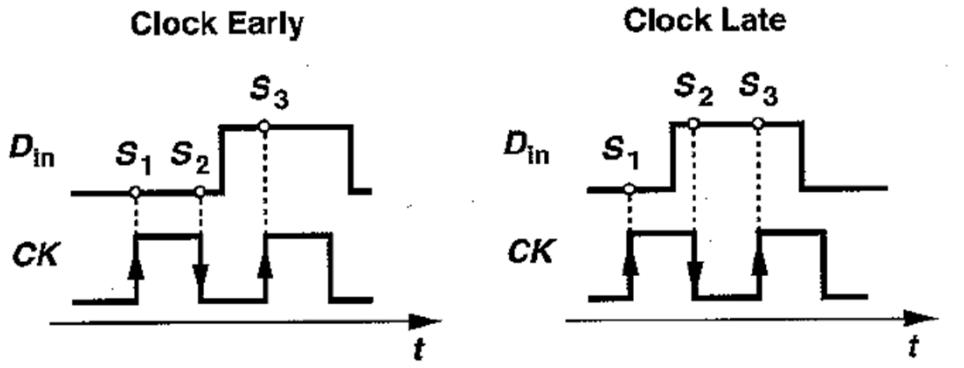


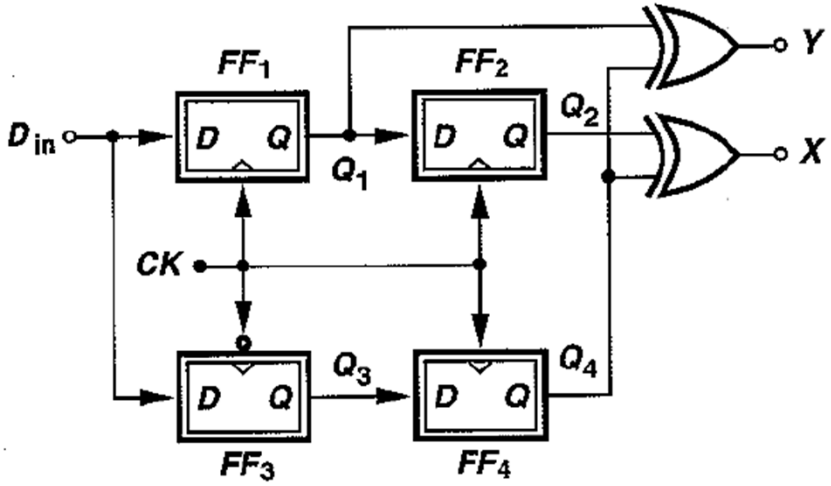
– Same signs for S_1,S_2,S_3: No transition

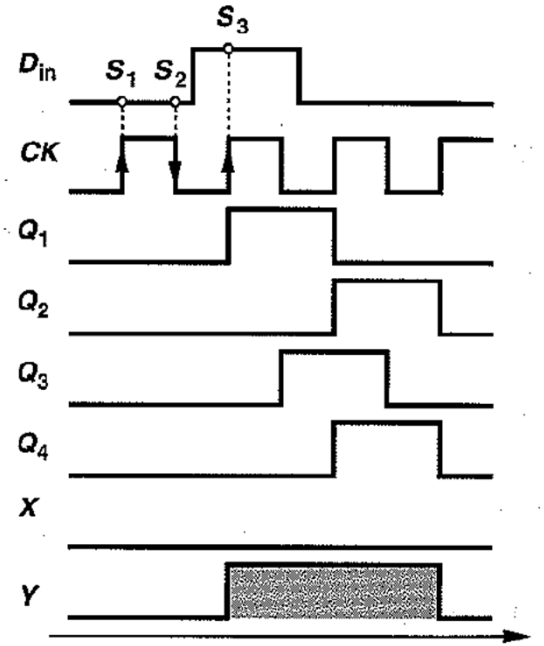
– Same signs for S_1,S_2 but different for S_3: Clock early

– Same signs for S_2,S_3 but different for S_1: Clock late

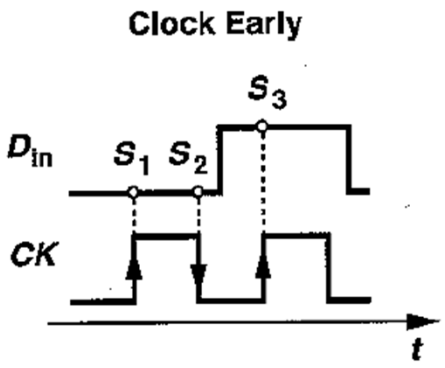
Alexander Phase Detector

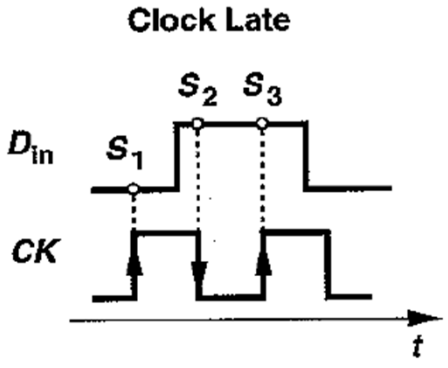


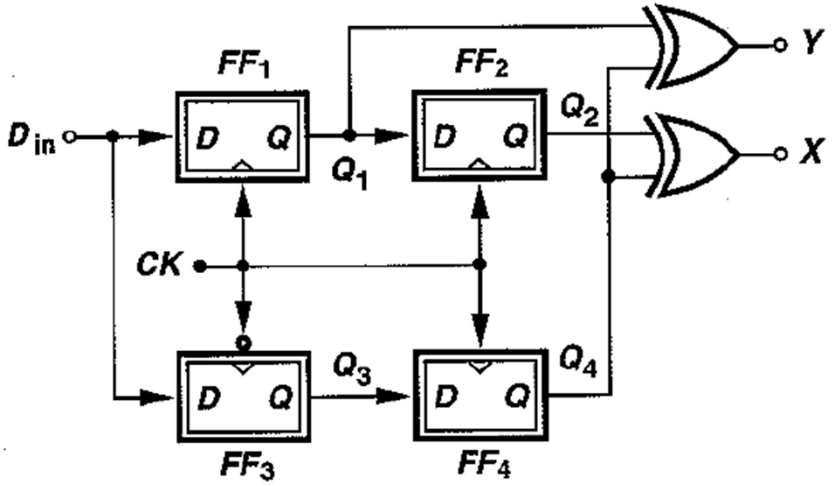


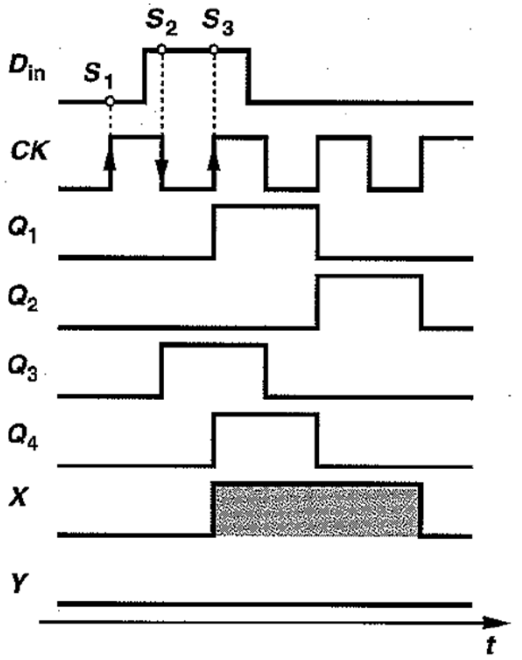


Alexander Phase Detector

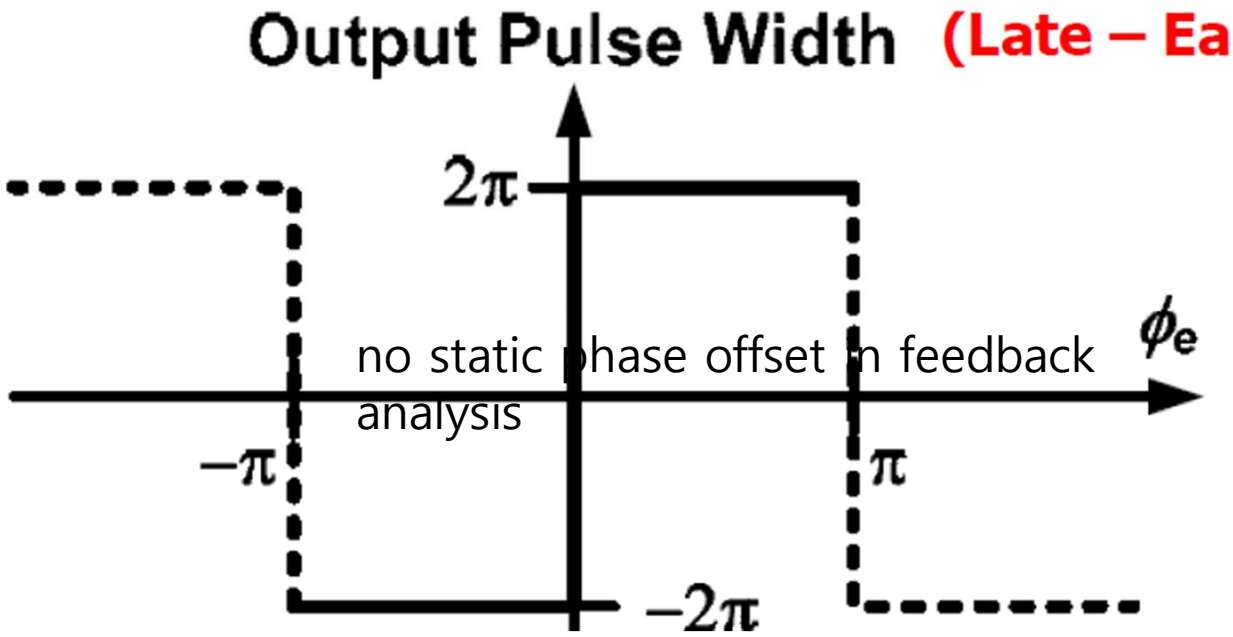






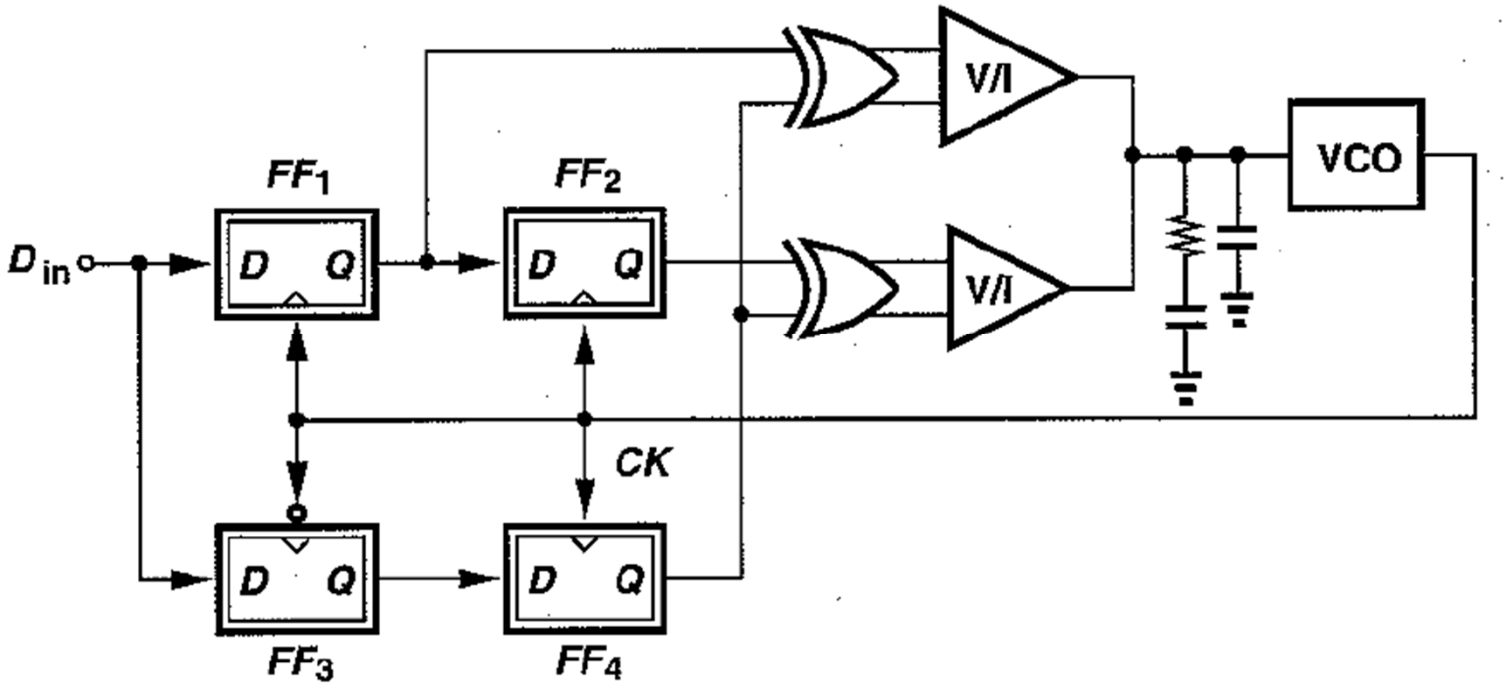


Alexander Phase Detector



- PD produces output whose width does not change (two periods)
- PD gain is infinite at $\Delta\phi = 0$ (No phase offset)

CDR with Alexander PD



- No charge pump: PD gain is very high
- Simple linear loop analysis not possible
- In reality, input jitter affects PD gain