### High-Speed Serial Interface Circuits and Systems

Lect. 5 – Phase-Locked Loop (PLL) 2

## Limitation of Type I PLL



- Locking range is very narrow

Step response simulations:

 $f_{in} = 1Hz, K_{PD} = 5V / rad, K_{VCO} = 2\pi \times 0.01 rad / s / V, and f_p = 0.032Hz$ 



## Limitation of Type I PLL

Problem lies in the very narrow linear phase detection range





With a large frequency difference, phase difference can become too large to be reliably detected

#### Phase and Frequency Detector (PFD)





D Flip-flop:

Q becomes D at the rising clock edge Q resets when R is HIGH

## **Charge Pump**





- Linear continuous-time model for charge-pump PLL?
- Charge pump operation is not continuous but discrete
- But make an approximation

Transfer function for PFD + Charge Pump:



Max 
$$\Delta \phi$$
:  $2\pi \rightarrow V_C(\mathbf{s})$ :  $I_{CP} \frac{1}{sC_1}$   
For any  $\Delta \phi$ :  $V_C(s) = \frac{\Delta \phi}{2\pi} I_{CP} \frac{1}{sC_1}$   
 $T(s) = \frac{V_C}{\Delta \phi}(s) = \frac{I_{CP}}{2\pi} \frac{1}{sC_1}$ 



Linear continuous-time model for charge-pump PLL





## **Stability**







 $G(s) = \frac{1}{2\pi} I_{CP} K_{VCO} \frac{1}{s^2 C_1}$ 

How to improve phase margin?

Introduce a zero

## **Stability**





Open loop gain:

$$G(s) = \frac{1}{2\pi} I_{CP} K_{VCO} \frac{sRC_1 + 1}{s^2 C_1}$$

However, there are ripples during transients for the step response



Qualitatively, changes in charge pump currents directly affect  $V_C$ 

Solution



→ Ripple reduction with small  $C_2$  ( <  $C_1/10$ )



→ 3rd order system

For dynamics analysis, 2<sup>nd</sup>-order PLL without C<sub>2</sub> is often used

Solution



$$G(s) = \frac{1}{2\pi} I_{CP} K_{VCO} \frac{sRC_1 + 1}{s^2 C_1}$$

$$H(s) = \frac{\frac{I_{CP}K_{VCO}}{2\pi C_1}(RC_1s+1)}{s^2 + \frac{I_{CP}}{2\pi}K_{VCO}Rs + \frac{I_{CP}}{2\pi C_1}K_{VCO}}$$

$$H(s) = \frac{2\zeta \omega_n s + \omega_n^2}{s^2 + 2\zeta \omega_n s + \omega_n^2} \qquad \qquad \omega_n = \sqrt{\frac{I_{CP} K_{VCO}}{2\pi C_1}} \qquad \qquad \zeta = \frac{R}{2} \sqrt{\frac{I_{CP} C_1 K_{VCO}}{2\pi}}$$

C<sub>2</sub> does affect PLL dynamics: It introduces an additional pole, which reduces the phase margin

Careful simulation is required for real PLL design

#### **CP PLL Step Responses**



➔ Optimization for desired performance!

#### **Charge Pump PLL with a Divider**

#### **PLL Phase Errors**



- Phase error due to phase step?

$$\phi_e(t=\infty) = \lim_{s \to 0} \left[ sH_e(s) \frac{\Delta \phi}{s} \right]$$

- Phase error due to frequency step?

**p?** 
$$\phi_e(t=\infty) = \lim_{s\to 0} \left[ sH_e(s) \frac{\Delta\omega}{s^2} \right]$$

## **Input-Noise Transfer Function**

• Input noise



$$H(s) = \frac{\phi_{out}}{\phi_{noise}} = \frac{(2\varsigma\omega_n s + \omega_n^2)M}{s^2 + 2\varsigma\omega_n s + \omega_n^2}$$

## **VCO-Noise Transfer Function**

VCO phase noise



## **Optimal PLL Bandwidth**



- Optimal PLL bandwidth depends on characteristics of each noise source
  - ➔ Design Project 1