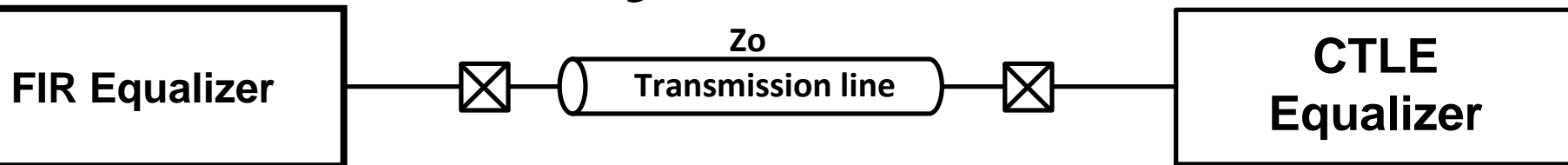


High-Speed Serial Interface Circuits and Systems

Project 2 – Equalizers

Project Goals



• 4Gb/s FIR and CTLE equalizers design

- Transmission line
 - Analyze transmission line impedance and loss
 - Need impedance matching
- CTLE equalizer
 - R_{load} : 1Kohm & C_{load} : 50fF and Current limit : 600uA
- FIR Equalizer
 - Make sure to use pre-cursor(s)
- Input data condition
 - Swing voltage 600mV and rising & falling time 10ps

• The report must contain:

1. Show schematic(size), transmission line characteristic(Z_o , loss), output eye diagram (including simulation time), current for each circuit (FIR and CTLE).
2. Explain how you come up with your circuit design.
3. Evaluation standard
 - EYE diagram height and width (Differential output): Simulate at least 10us for eye-diagram
 - Total Current consumption

• Due date : 18 Dec. AM 10:00 @ B629 Hardcopy

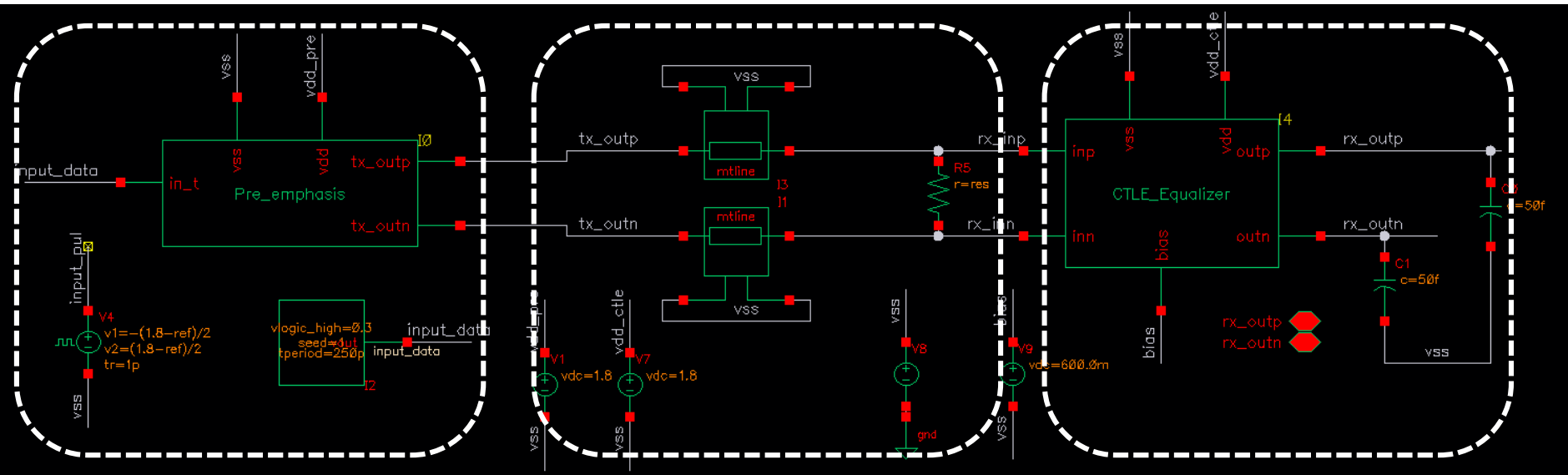
Schematic

FIR Equalizer

Z_0

Transmission line

CTLE Equalizer



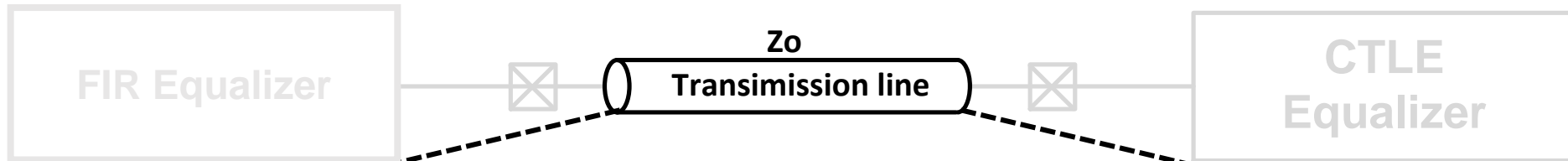
< Pre-emphasis >

< Transmission-line >

< CTLE Equalizer >

- Design 4Gb/s FIR and CTLE equalizers.
- Analyze transmission line impedance and loss.

Transmission Line



CDF Parameter	Value	Display
Num of lines (excluding ref.)	1	off
Physical length	10 M	off
Multiplicity factor	1	off
Max signal frequency		off
Type of Input	FieldSolver	off
Transmission line type	microstrip	off
Model type	wideband	off
Rel dielectric const of layers(er)	4.8	off
Dielectric layer thickness (d)	360u	off
Signal line width	447u	off
Signal line thickness	17.78u	off

- Type of Input : FieldSolver
- Transmission line type : microstrip
- Model type : wideband
- Real dielectric const of layers : 4.8 (FR4)
- Dielectric layer thickness : 360u (H)
- **Signal line width : 447u (W)**
- Signal line thickness : 17.78u (T)
- **Physical length : 10 M**
- Analyze transmission line impedance and loss
- Need impedance matching

FIR Equalizer

FIR Equalizer

Z_0
Transmission line

CTLE
Equalizer

Main-cursor

2nd Post-cursor

Pre-cursor

3rd Post-cursor

1st Post-cursor

4th Post-cursor

- Make sure to use pre-cursor(s)
- You can use any number of post-cursor(s)
- But power consumption should also be considered.
- Need to match transmission line impedance.

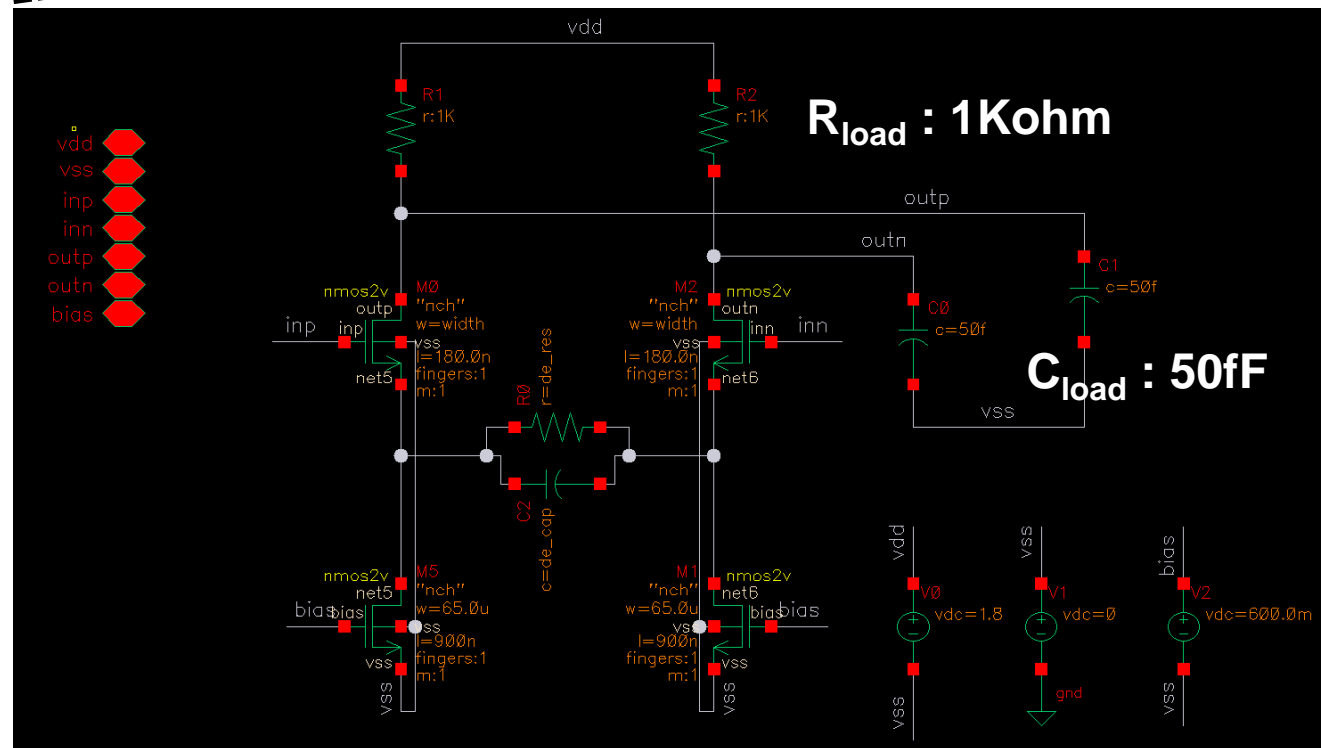
CTLE

FIR Equalizer

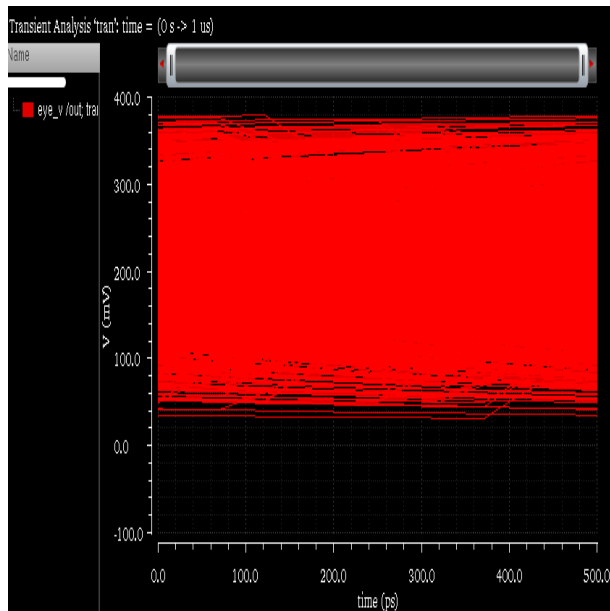


CTLE
Equalizer

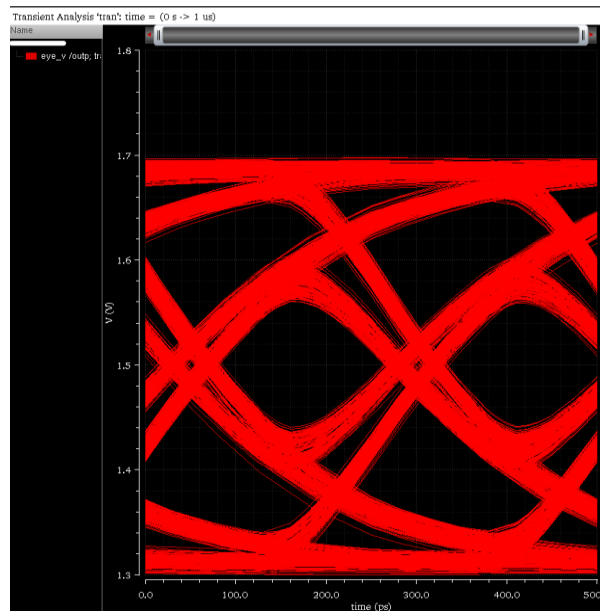
- $R_{load} : 1K\Omega$
- $C_{load} : 50fF$
- Current limit : 600uA
- Tuning location of pole and zero
- Tuning DC gain



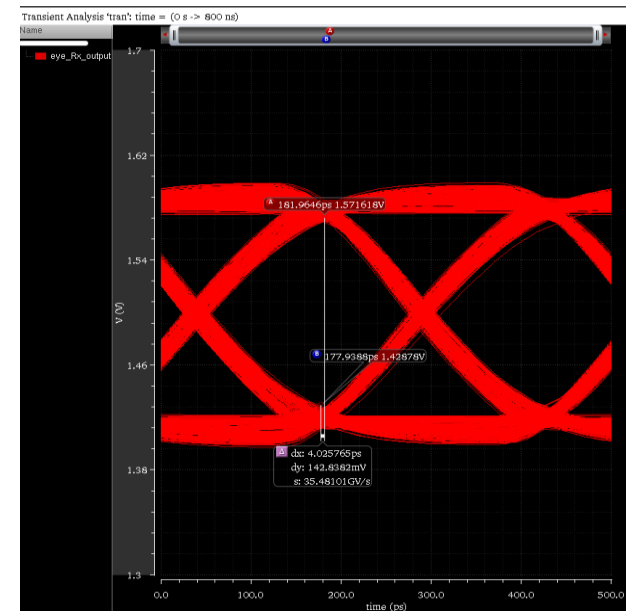
Simulation Result



< Transmission Line >

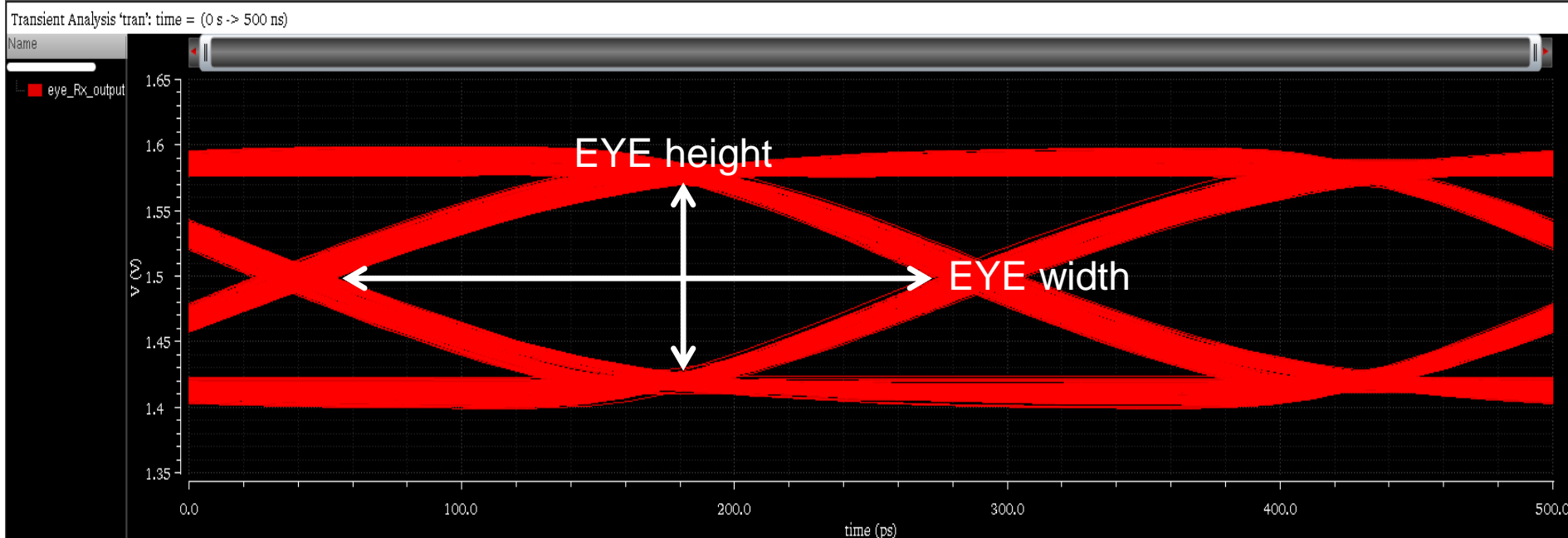


< CTLE >



< CTLE + FIR Equalizer >

EYE Diagram



- Pre-cursor and 3rd post-cursor FIR Equalizer
- CTLE Equalizer
- EYE Diagram
 - EYE width* : 219ps & height : 142mV
 - EYE Area* : 31210.58 (mV * ps)
- Current consumption
 - Pre-emphasis : 28.222mA & CTLE Equalizer : 600uA
 - Total current : 28.822mA

*These results are single-ended