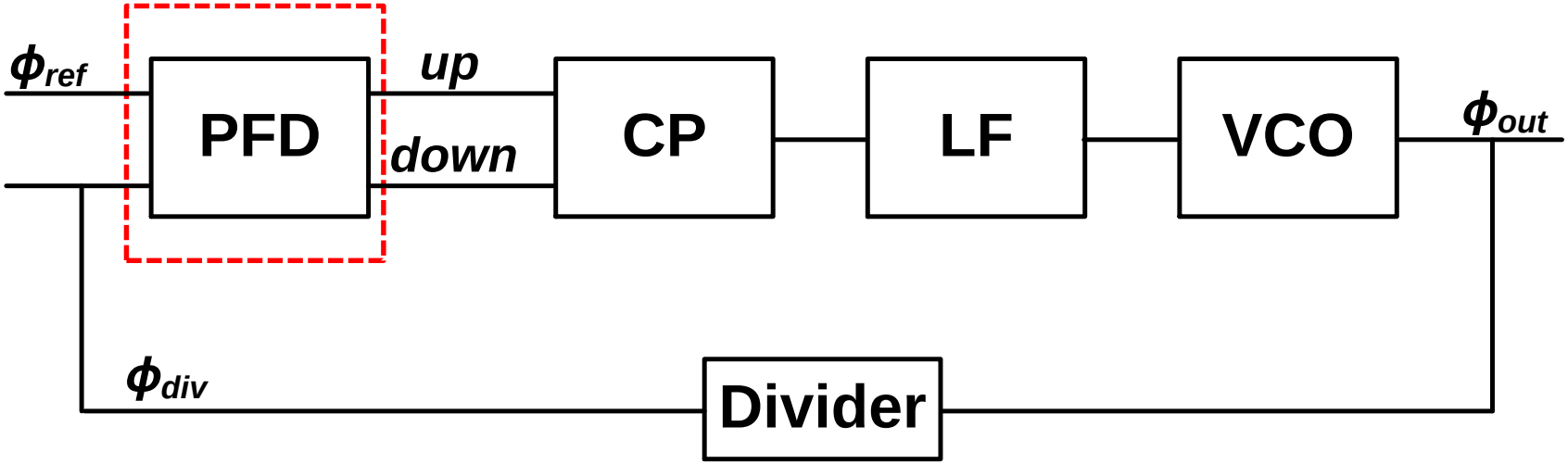
High-Speed Serial Interface Circuits and Systems

Design Exercise 4-2

Phase Frequency Detector

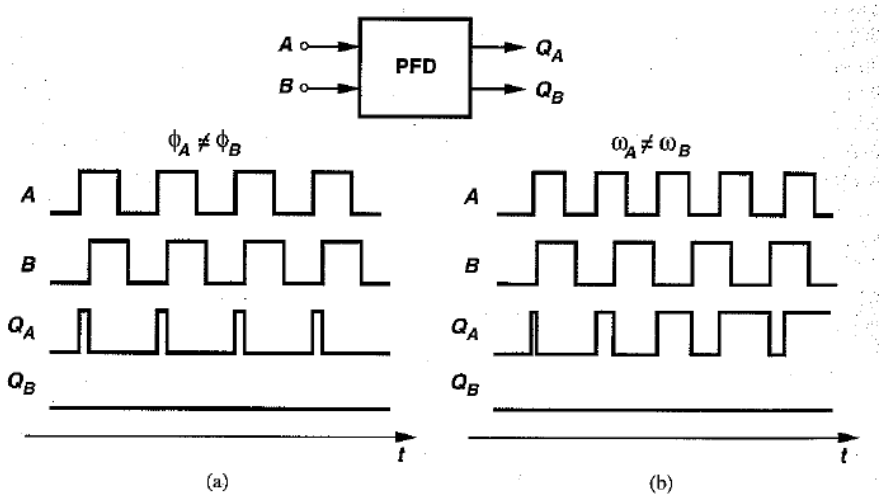
Charge Pump PLL



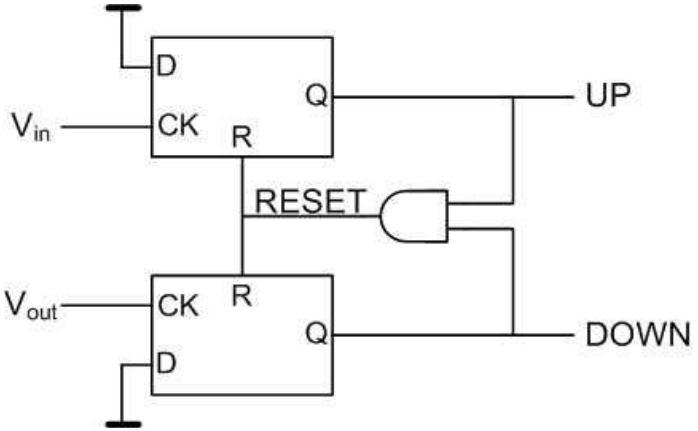
- ✓ VCO (Week 2-3)
  - Generates the actual clock used by the system
- ✓ Charge Pump (Week 4)
  - Adjusts the frequency control signal of the VCO by charging and discharging the loop filter using the up and down signals of the PFD.
- ✓ PFD (Today)

  - Compares the reference clock to the VCO clock to determine whether the charge pump will charge or discharge the loop filter.

Phase Frequency Detector



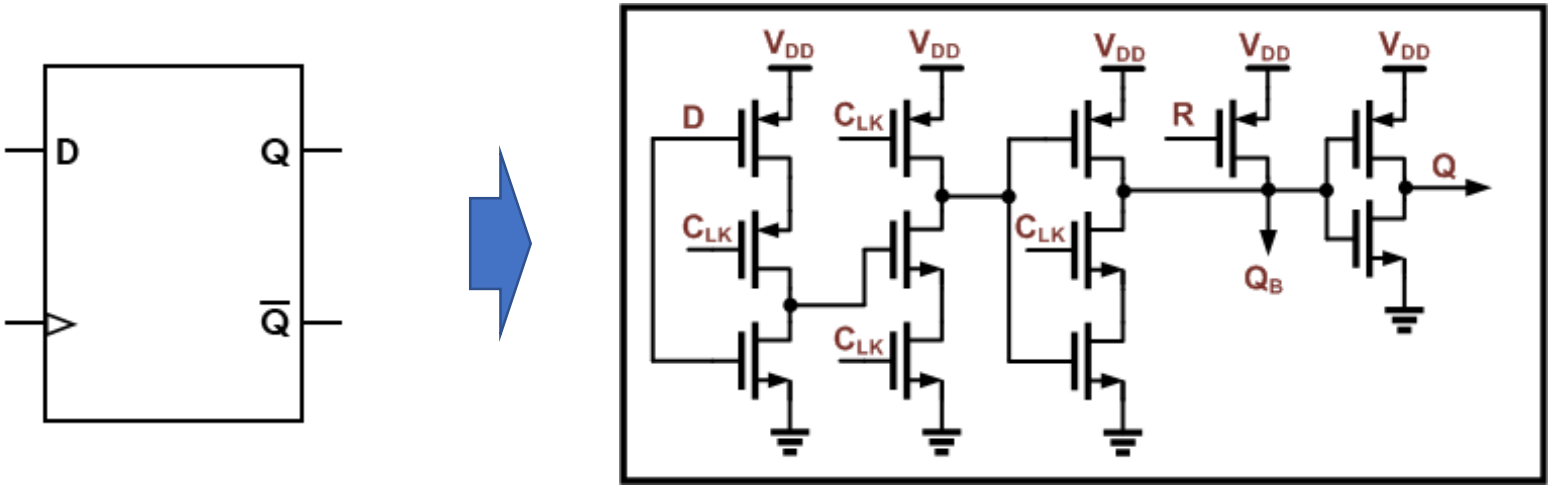
<PFD operation>



<PFD structure>

- ✓ Phase detector can't detect frequency difference.
- ✓ Using PFD, both phase lead/lag conditions and frequency lead/lag conditions can be calculated.

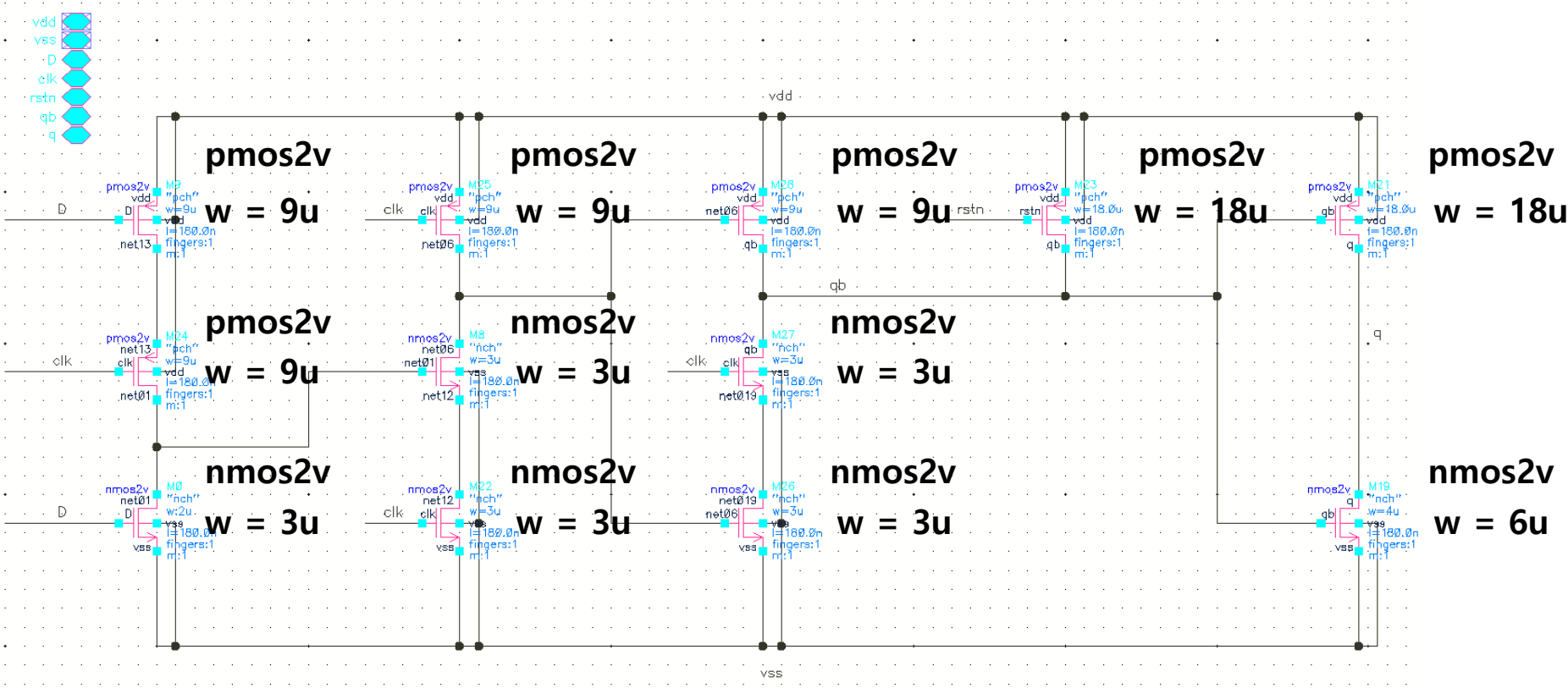
TSPC D flip flop



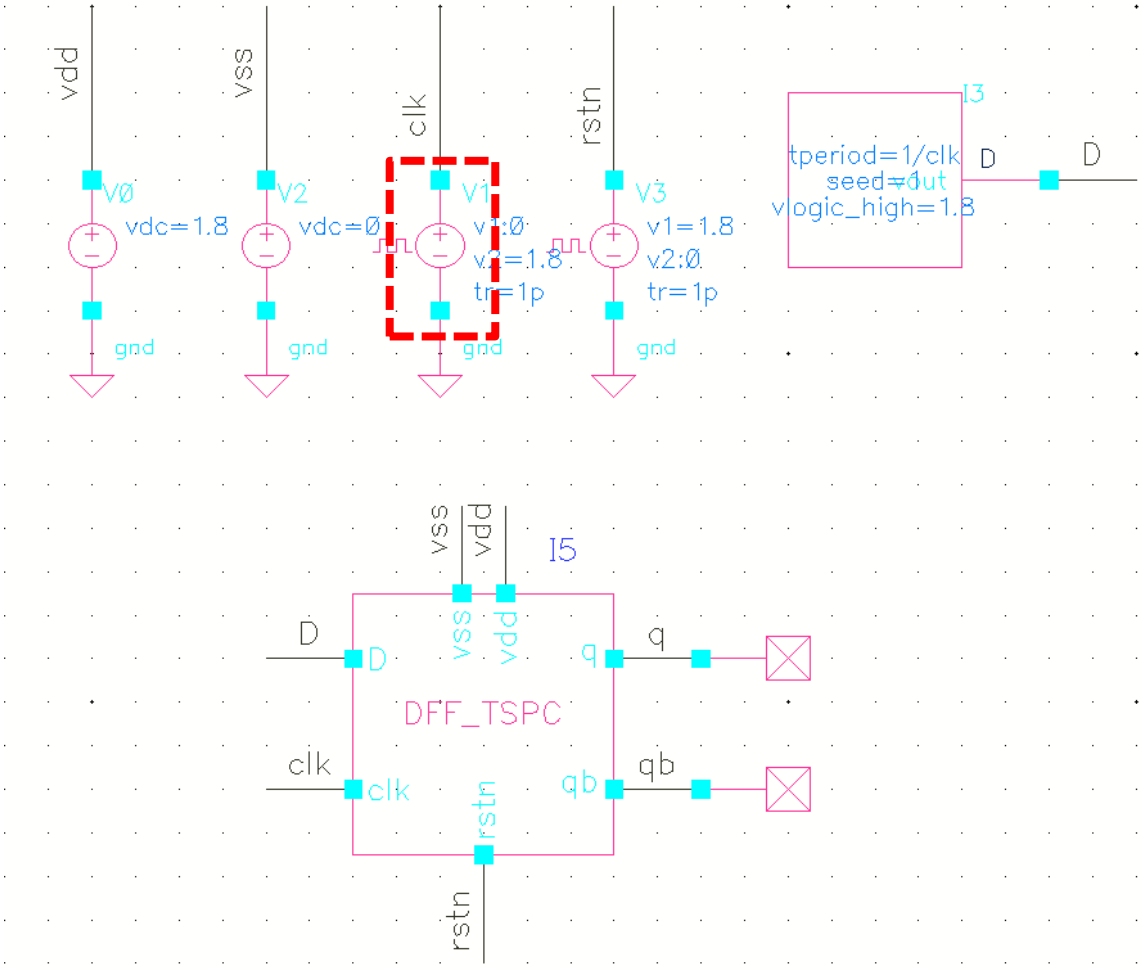
- ✓ True single-phase clock DFF (Developed in the 80s')
- ✓ Using dynamic logic gate topology.
- ✓ Widely used structure for high speed applications.
- ✓ Detailed explanation
  : B. Razavi, "TSPC Logic," *IEEE Solid-State Circuits Magazine*, Fall 2016

TSPC DFF Schematic

– MOS Length
  - 모두 180 nm로 고정

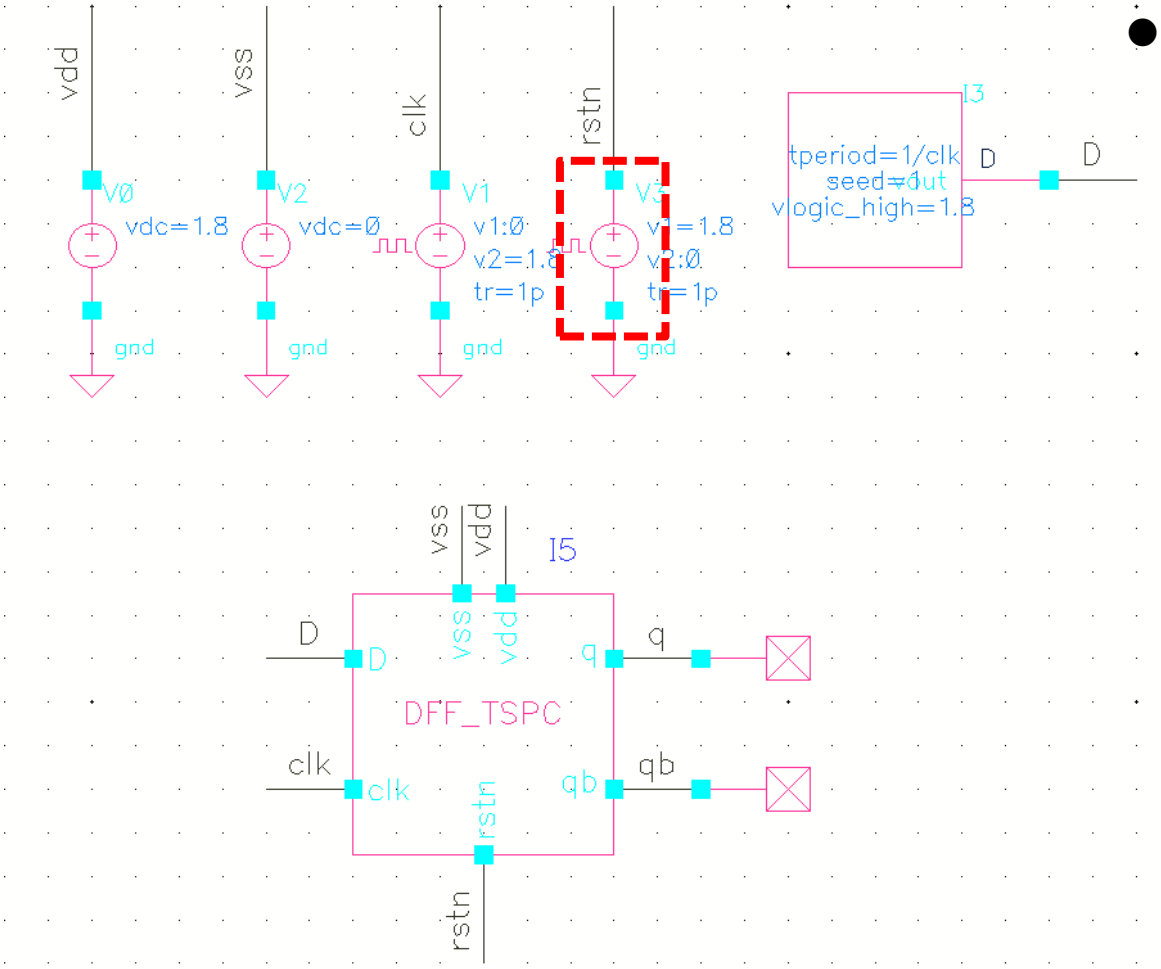


Simulation Setup



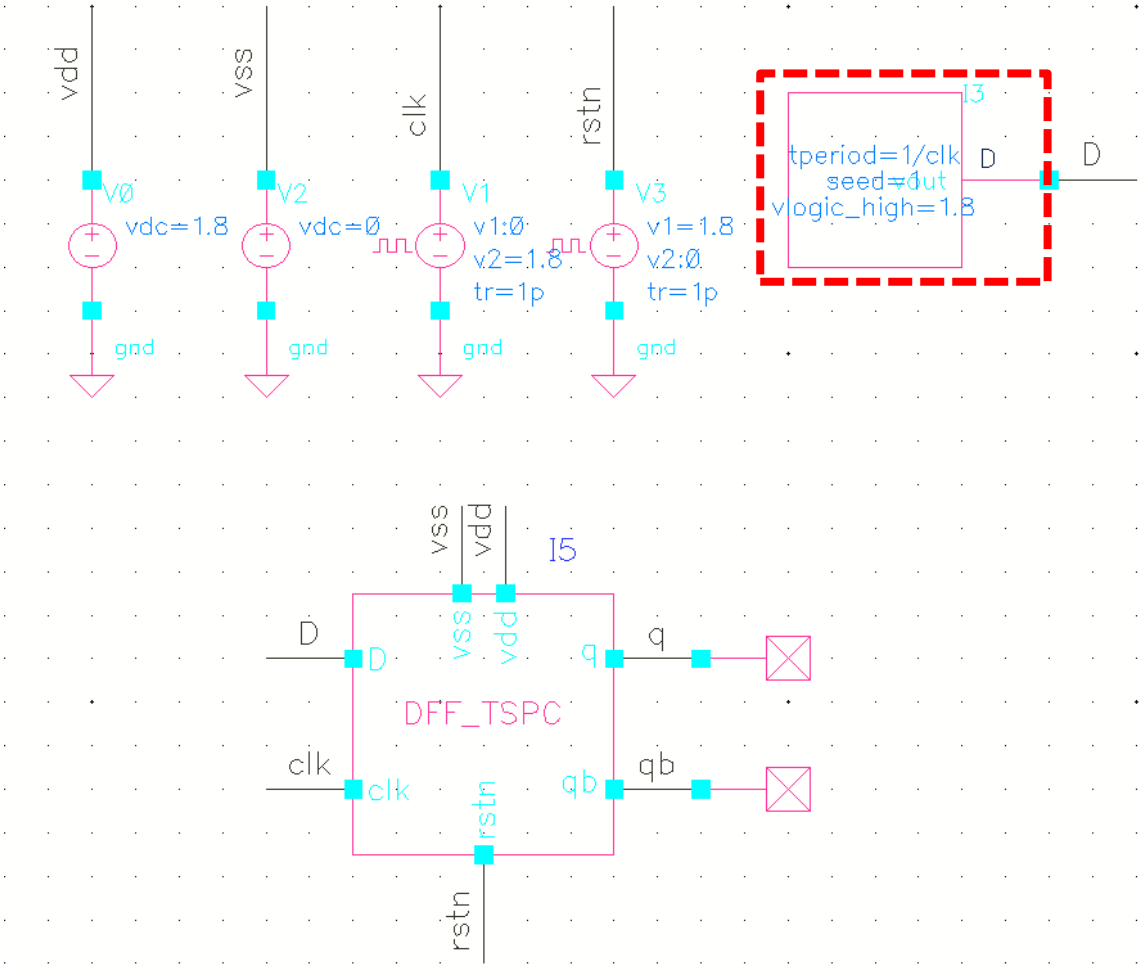
- 'clk' node
  - ✓ use 'vpulse'
  - ✓ Voltage 1 = 0
  - ✓ Voltage 2 = 1.8
  - ✓ Period = 1/clk
  - ✓ delay time = delay
  - ✓ rise time = 1p
  - ✓ Fall time = 1p
  - ✓ Pulse width = 0.5/clk

Simulation Setup



- 'rstn' node
  - ✓ use 'vpulse'
  - ✓ Voltage 1 = 1.8
  - ✓ Voltage 2 = 0
  - ✓ Period = 500m
  - ✓ delay time = reset_start
  - ✓ rise time = 1p
  - ✓ Fall time = 1p
  - ✓ Pulse width = 250m

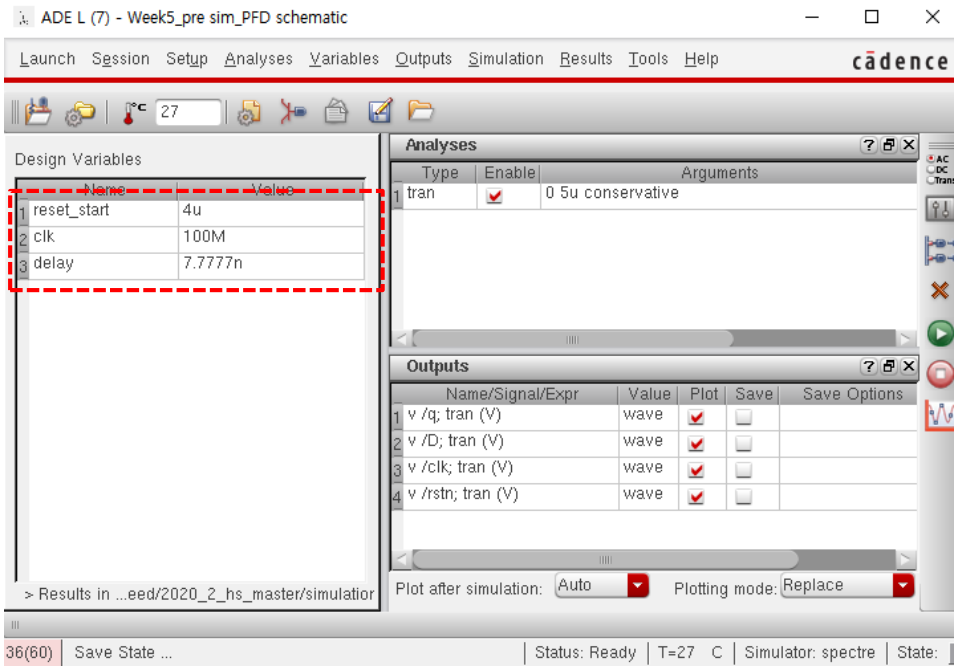
Simulation Setup



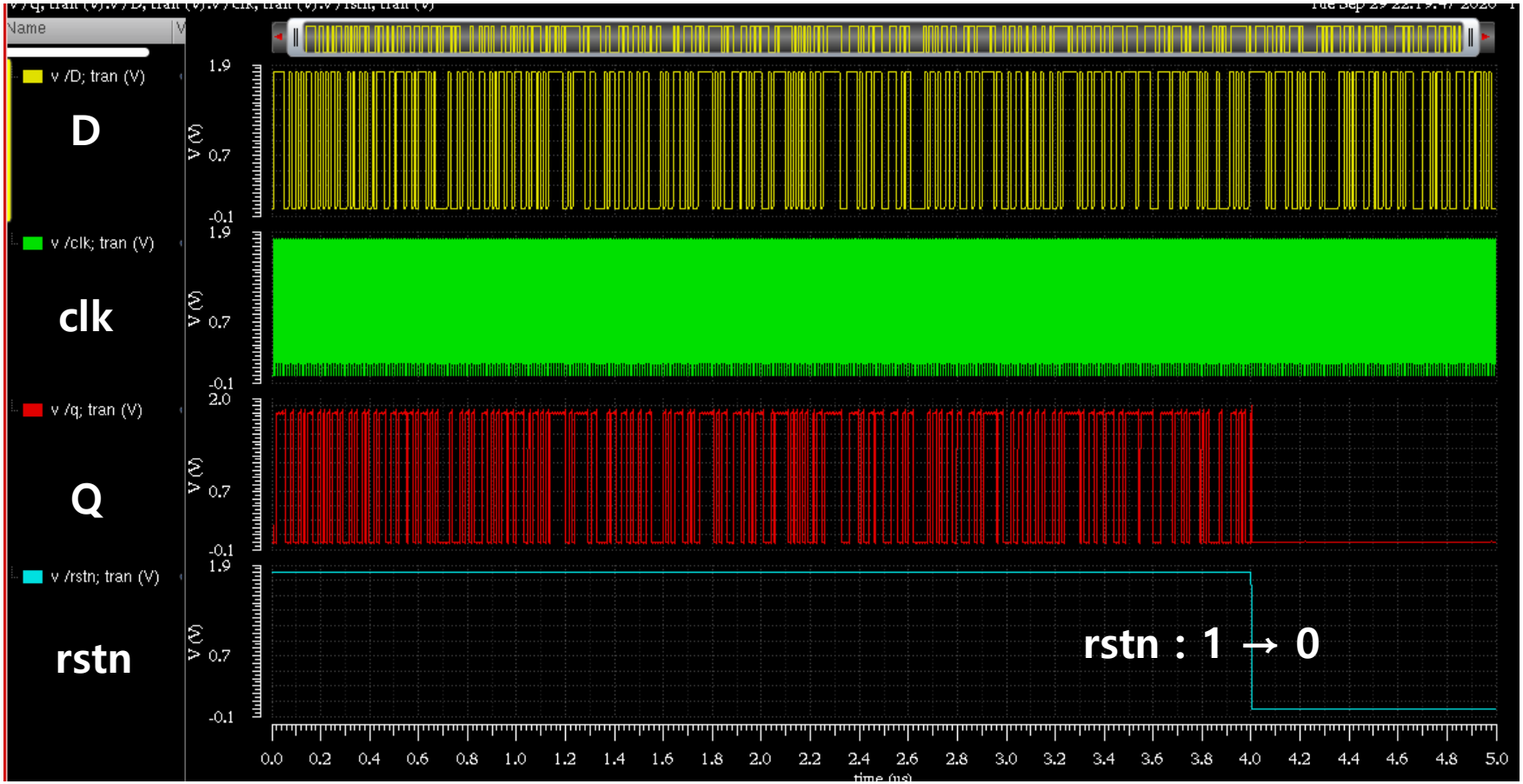
- 'D' node
  - ✓ use 'rand_bit_stream'
  - ✓ tperiod = 1/clk
  - ✓ seed = 1
  - ✓ vlogic_high = 1.8
  - ✓ vlogic_low = 0
  - ✓ tdel = 1p
  - ✓ trise = 1p
  - ✓ tfall = 1p

Simulation Condition

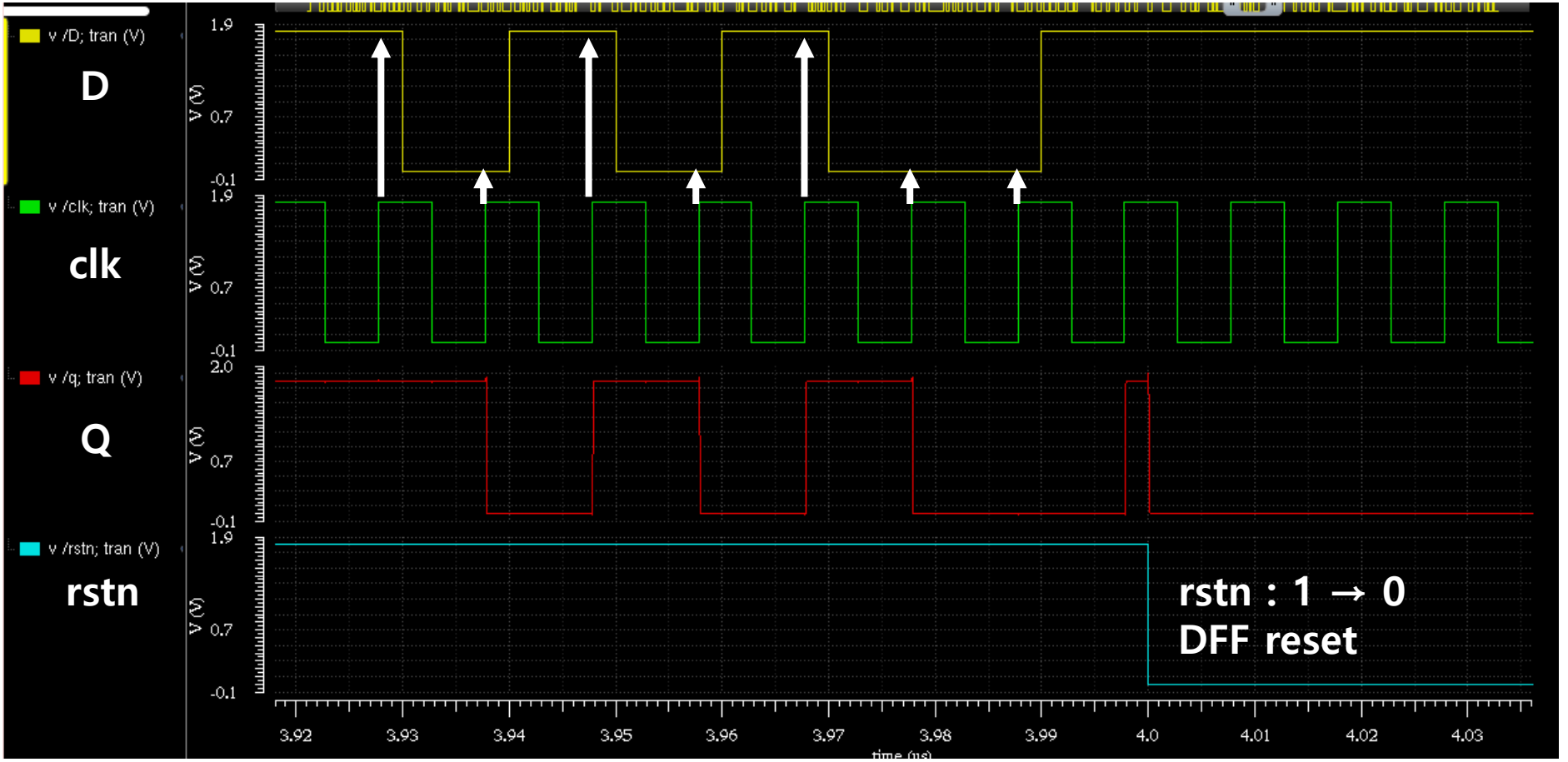
- Simulation condition setting
  - Choose analysis
  - Analysis : tran
  - transient sim. time = 5u
  - Design variable :
    - reset_start = 4u
    - clk = 100M
    - delay = 7.7777n
- check output node to plot
  - Q
  - clk
  - D
  - rstn



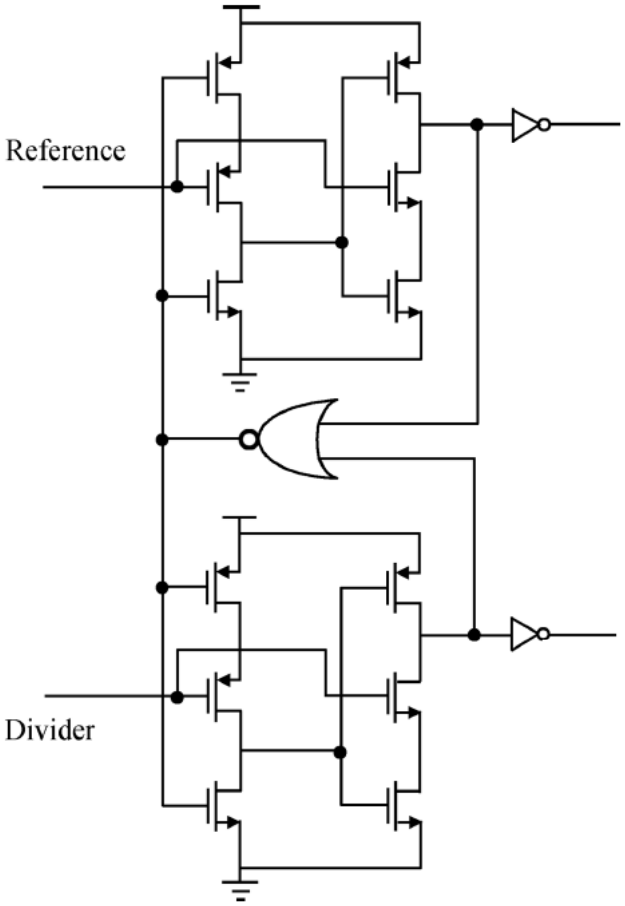
Simulation result



Simulation result



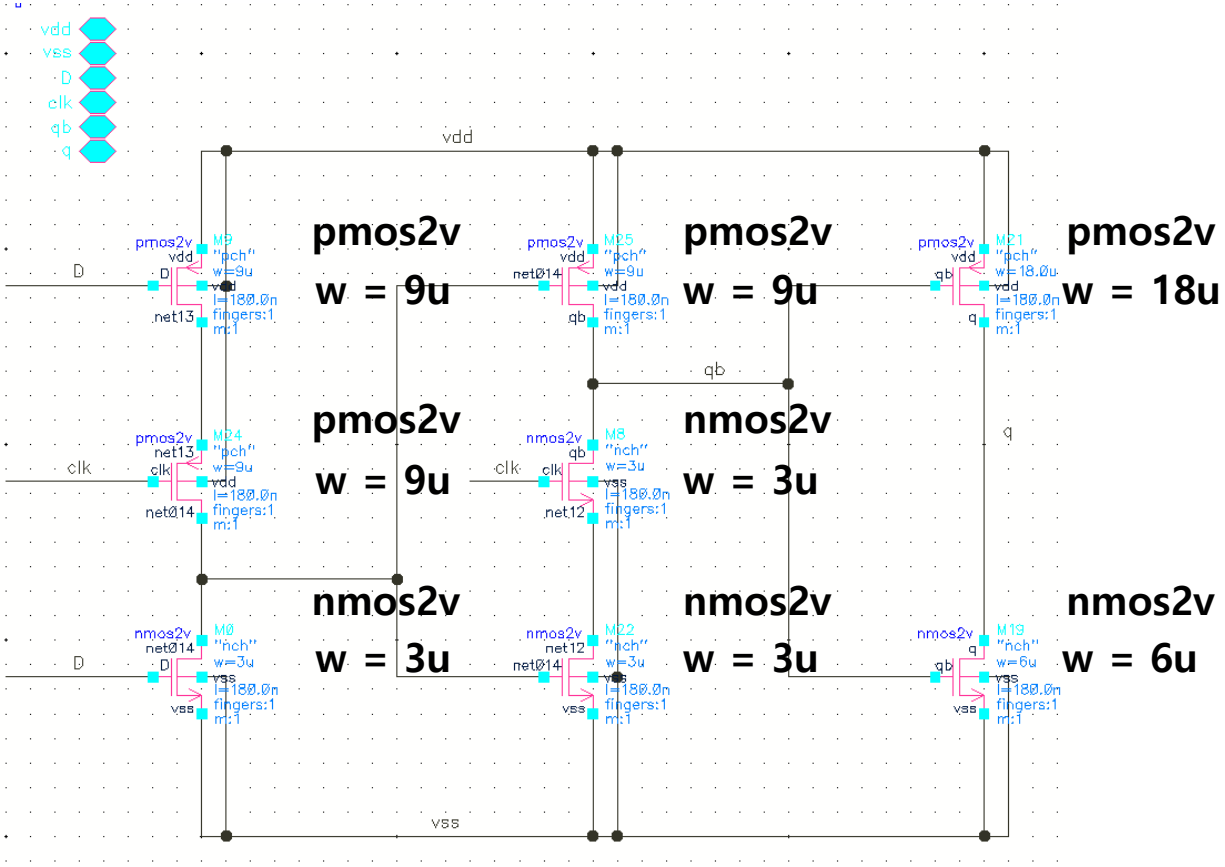
Modified structure of TSPC for PFD



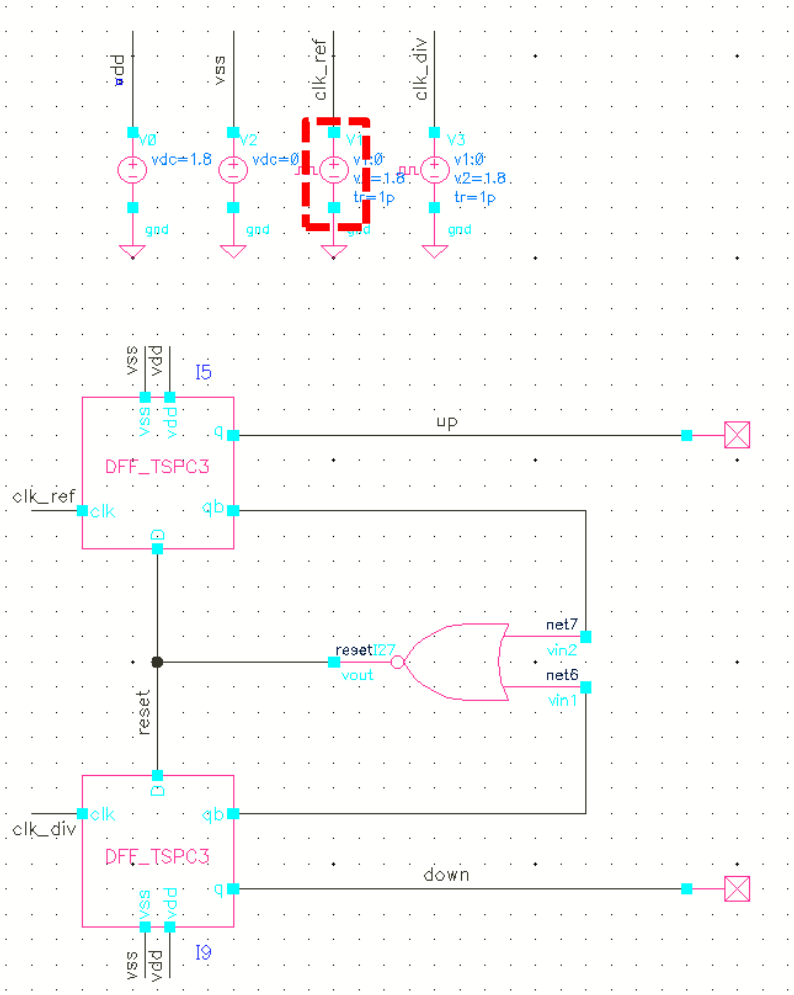
- ✓ Precharge type PFD
- ✓ Required MOS for sampler : 12 → 8
- ✓ D + reset → set
- ✓ Widely used for PFD design
- ✓ Detailed explanation
  : Sungjoon Kim et al, "A 960-Mb/s/pin interface for skew-tolerant bus using low jitter PLL," *IEEE Journal of Solid-State Circuits*, May 1997

Modified TSPC DFF Schematic

– MOS Length
  - 모두 180 nm로 고정

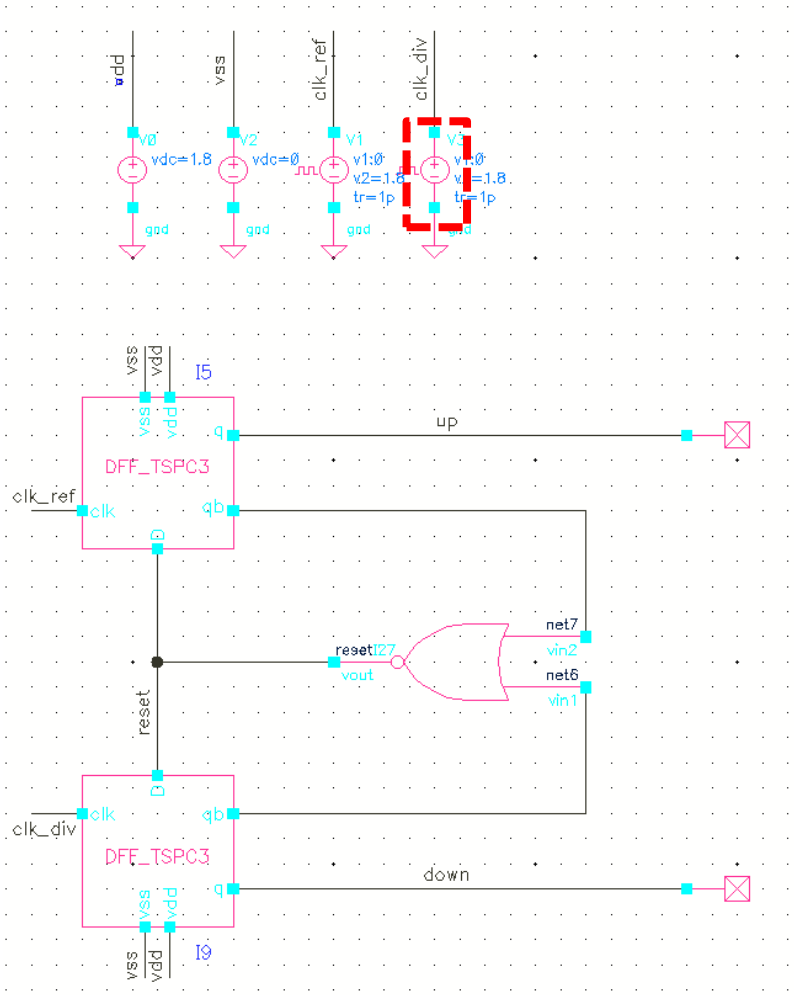


Simulation Setup



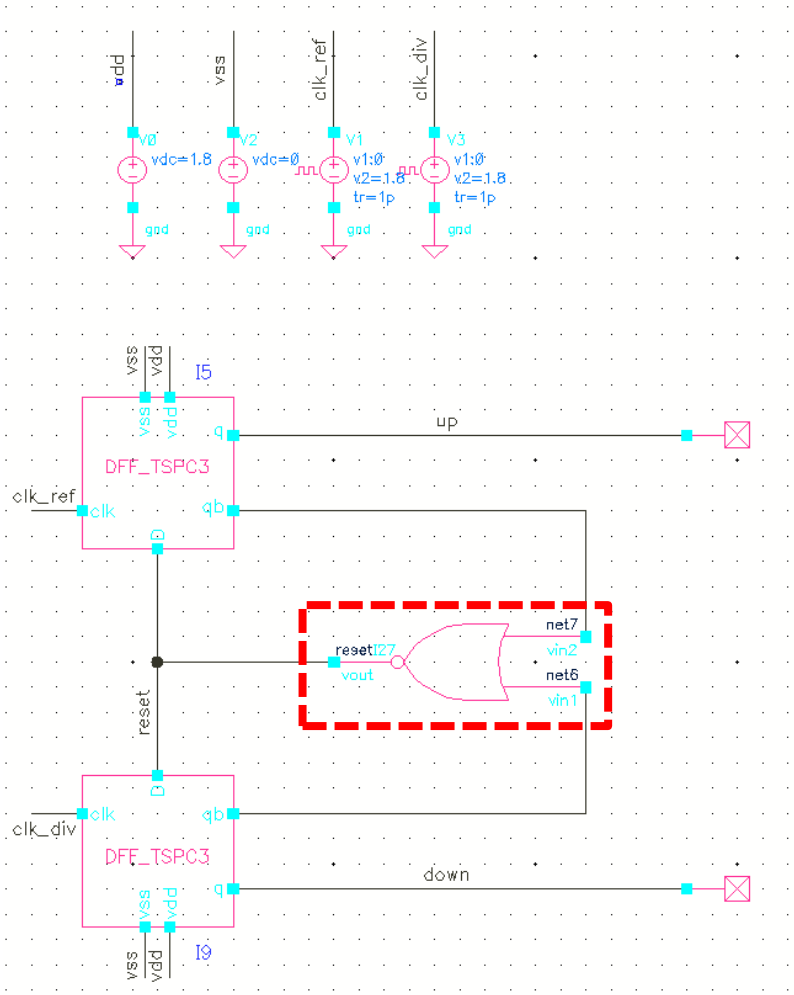
- 'clk_ref' node
  - ✓ use 'vpulse'
  - ✓ Voltage 1 = 0
  - ✓ Voltage 2 = 1.8
  - ✓ Period = 1/clk_ref
  - ✓ delay time = delay_ref
  - ✓ rise time = 1p
  - ✓ Fall time = 1p
  - ✓ Pulse width = 0.5/clk_ref

Simulation Setup



- 'clk_div' node
  - ✓ use 'vpulse'
  - ✓ Voltage 1 = 0
  - ✓ Voltage 2 = 1.8
  - ✓ Period = 1/clk_div
  - ✓ delay time = delay_div
  - ✓ rise time = 1p
  - ✓ Fall time = 1p
  - ✓ Pulse width = 0.5/clk_div

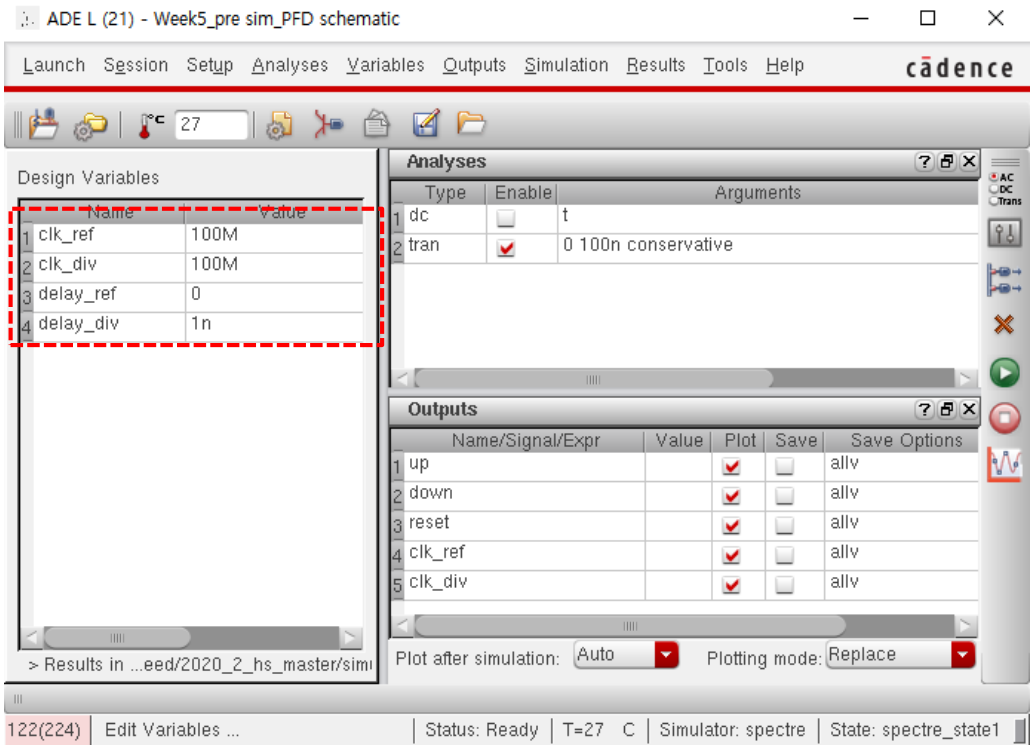
Simulation Setup



- 'nor_gate'
  - ✓ vlogic_high = 1.8
  - ✓ vlogic_low = 0
  - ✓ vtrans = 0.9
  - ✓ tdel = 1p
  - ✓ trise = 1p
  - ✓ tfall = 1p

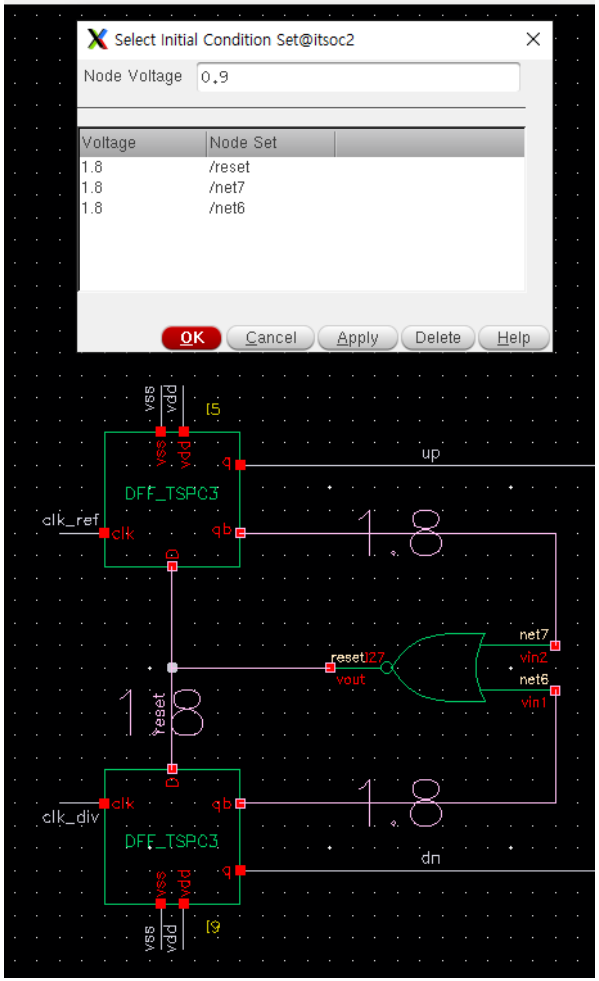
Simulation Condition

- Simulation condition setting
  - Choose analysis
  - Analysis : tran
  - transient sim. time = 100n
  - Design variable :
    - clk_ref = 100M
    - clk_div = 100M
    - delay_ref = 0n / 1n
    - delay_div = 1n / 0n
- check output node to plot
  - clk_ref
  - clk_div
  - up
  - down

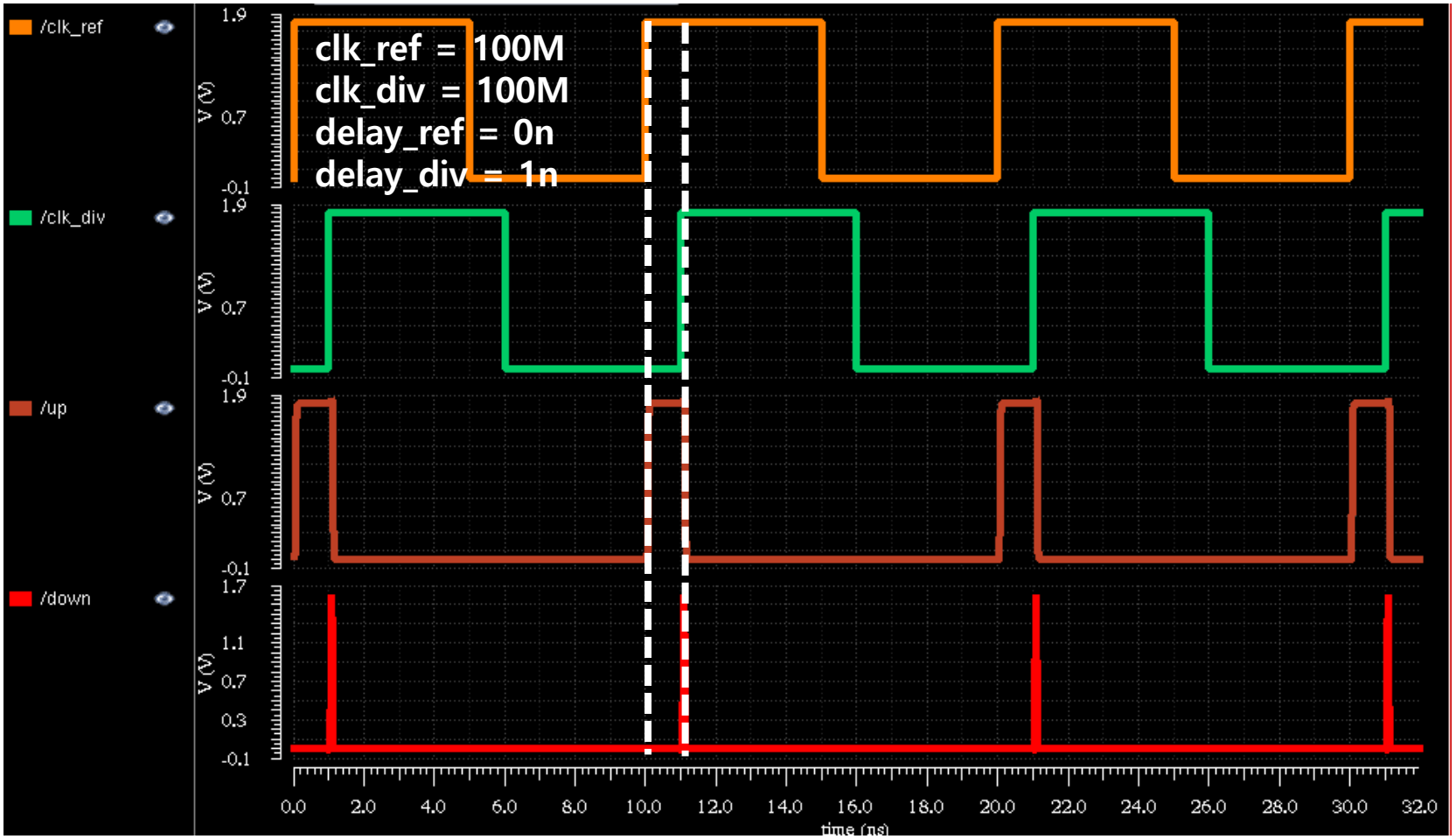


Simulation Condition

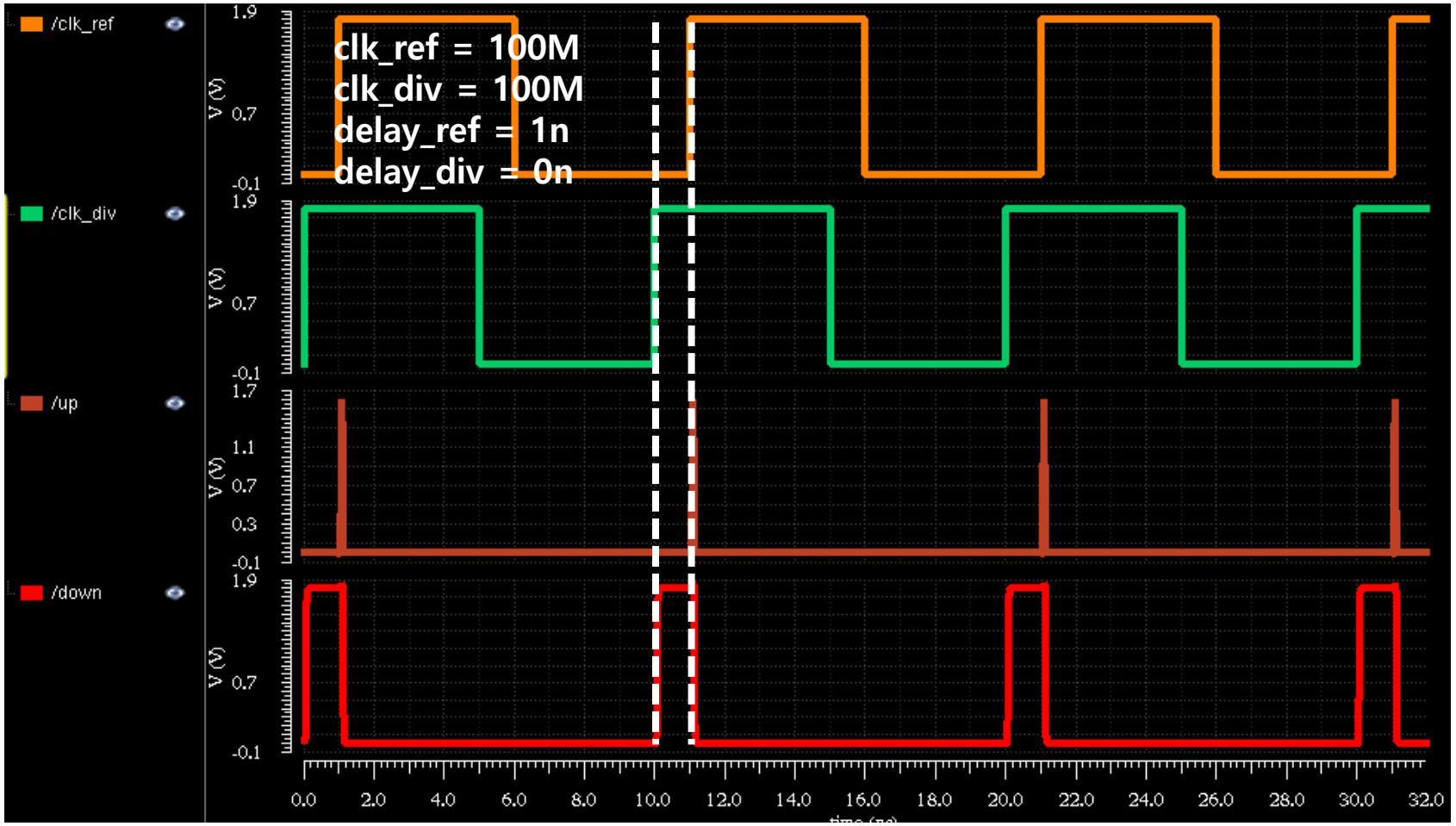
- Initial Condition
- Nodes
  - SET = 1.8
  - QB_ref 1.8
  - QB_div = 1.8



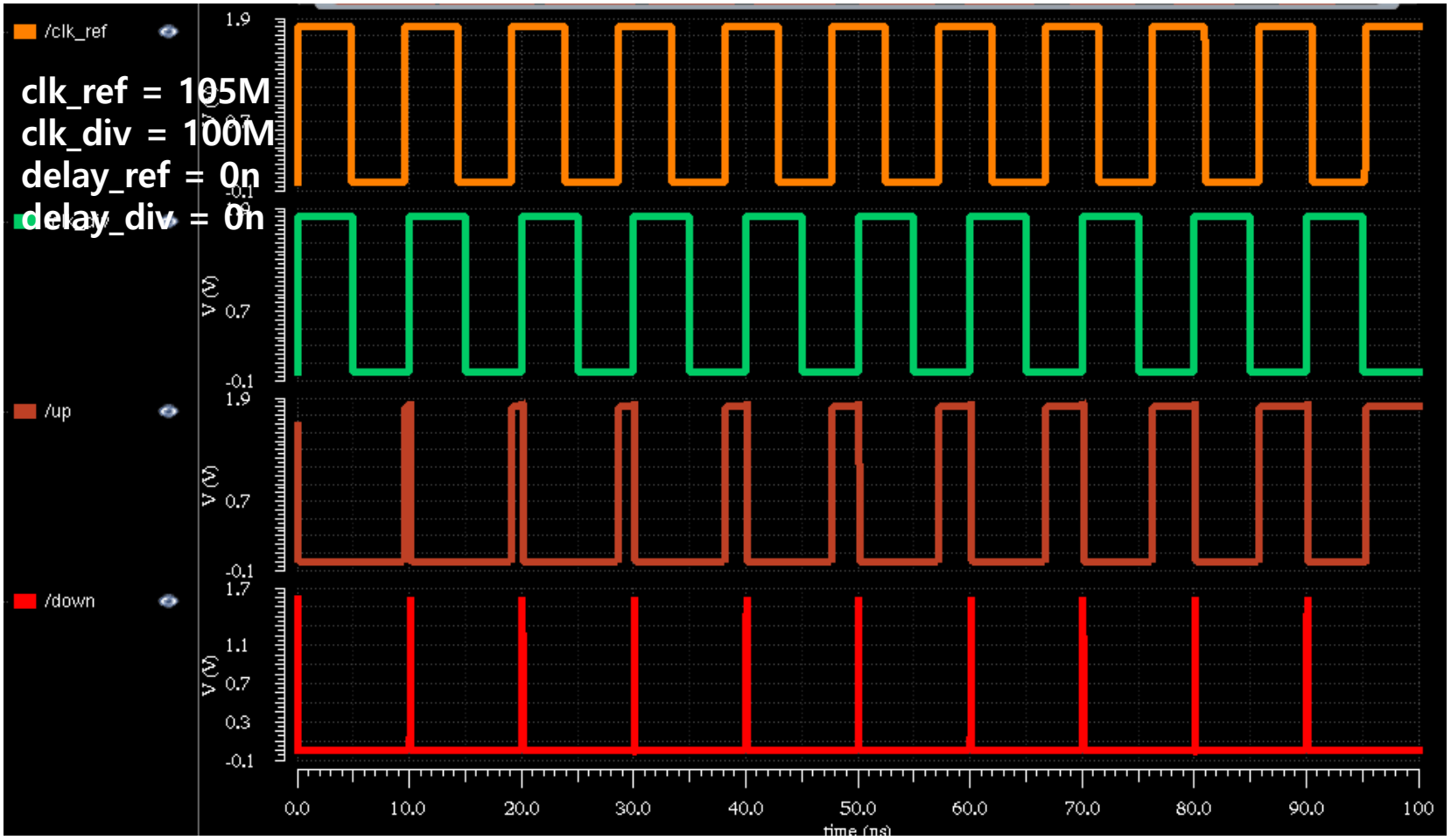
Phase lead


/clk_ref
/clk_div
/up
/down
clk_ref = 100M
clk_div = 100M
delay_ref = 0n
delay_div = 1n
1.9
0.7
-0.1
1.7
1.1
0.3
V(V)
0.0
2.0
4.0
6.0
8.0
10.0
12.0
14.0
16.0
18.0
20.0
22.0
24.0
26.0
28.0
30.0
32.0
time (ns)

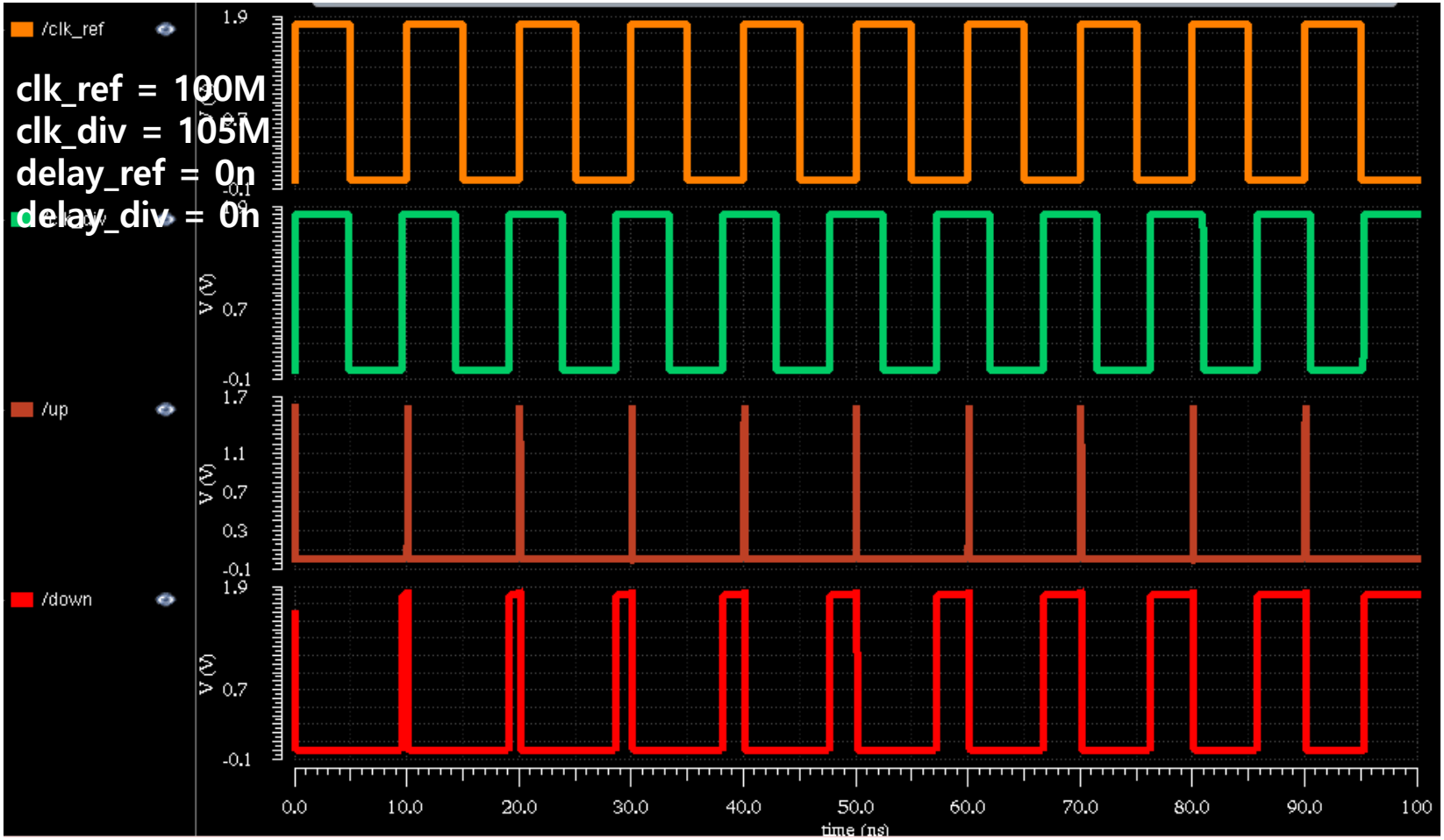
Phase lag


/clk_ref
/clk_div
/up
/down
clk_ref = 100M
clk_div = 100M
delay_ref = 1n
delay_div = 0n
1.9
0.7
-0.1
1.7
1.1
0.3
V (V)
0.0
2.0
4.0
6.0
8.0
10.0
12.0
14.0
16.0
18.0
20.0
22.0
24.0
26.0
28.0
30.0
32.0

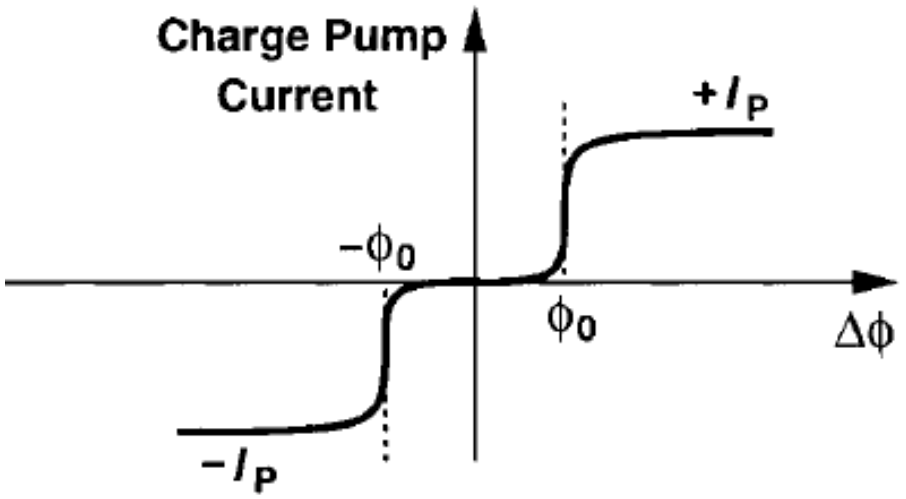
Frequency lead



Frequency lag

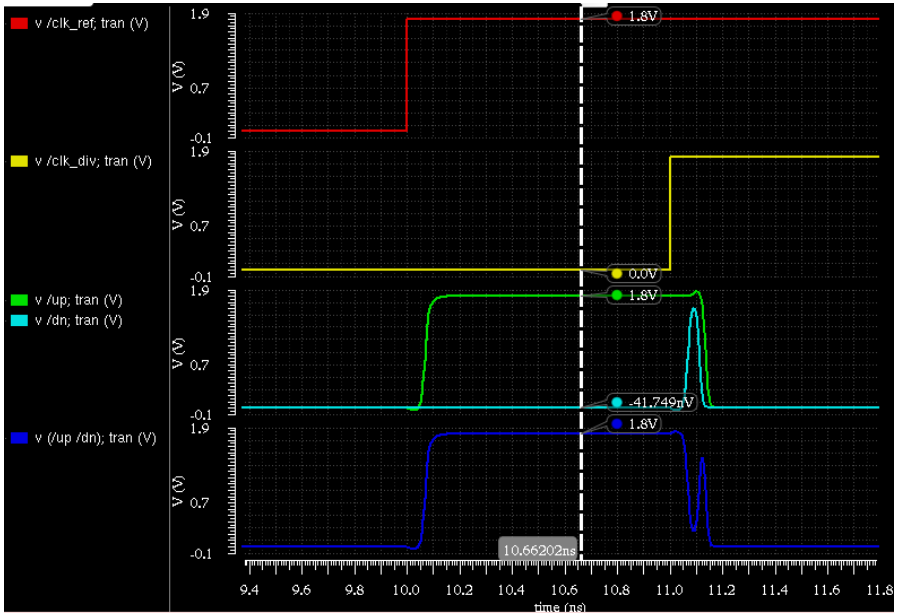


Dead zone of PFD

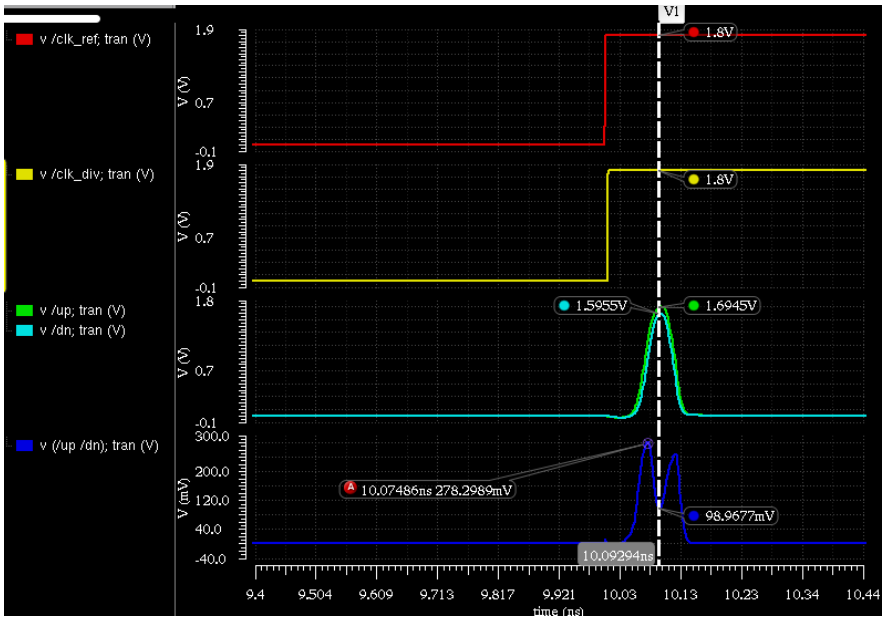


- ✓ PFD cannot detect the phase difference in a certain area:
  - Dead zone of PFD
- ✓ Caused by finite rising/falling time of DFF output
- ✓ The larger the dead zone, the worse the jiiter performance of the PLL.

Dead zone of PFD



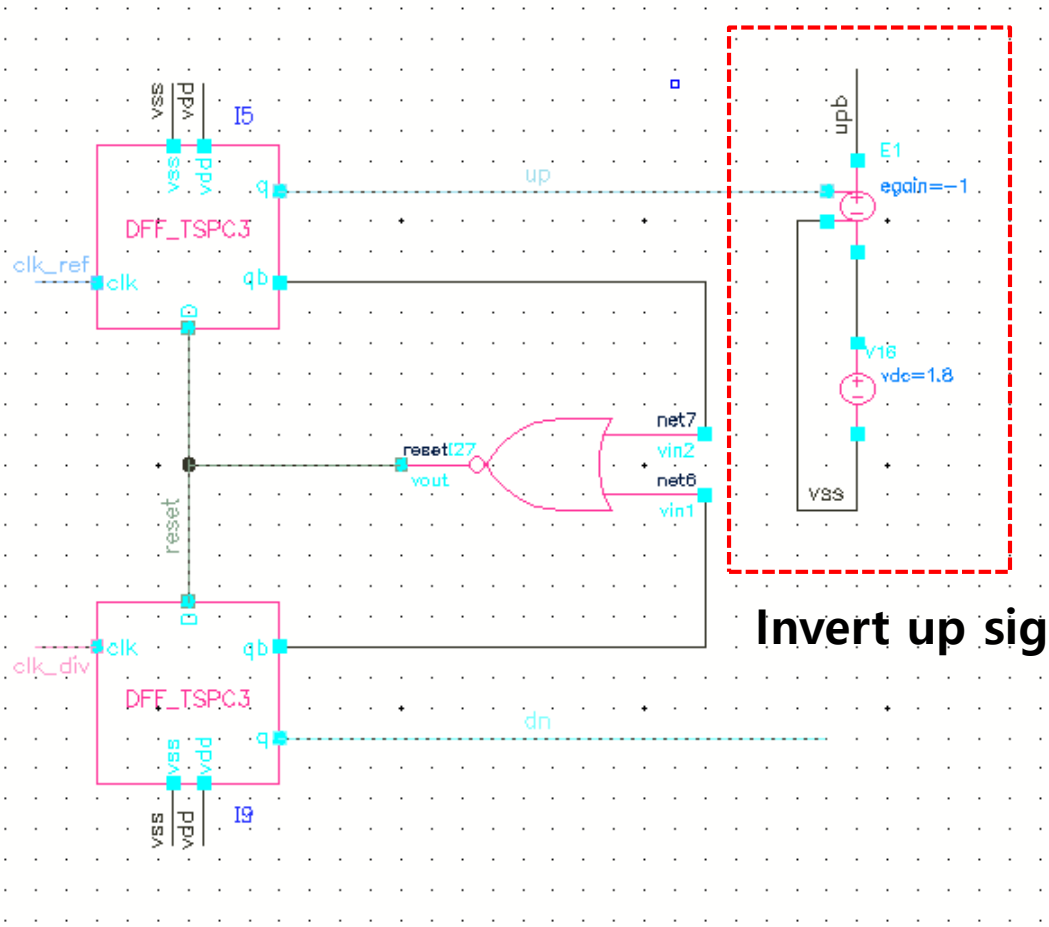
< delay= 1n >



< delay= 5p >

✓ PFD output can’t rise to logic high.

Connect to Charge Pump



Invert up signal to upb

Homework

- ✓ Simulate Vcont with co-simulation of PFD and CP.
- ✓ Use charge pump cirucit made in 4th week.
- ✓ Loop filter for charge pump : 10p capacitor load
- ✓ Initial Condition : Charge pump output (Vcont) = 0.9
- ✓ Check for all conditions : Phase lead/lag, Frequency lead/lag
- ✓ Deadline : 10/08(Thu) 19:00
  - ➢ Upload pdf file to YSCEC