

High-Speed Serial Interface Circuits and Systems

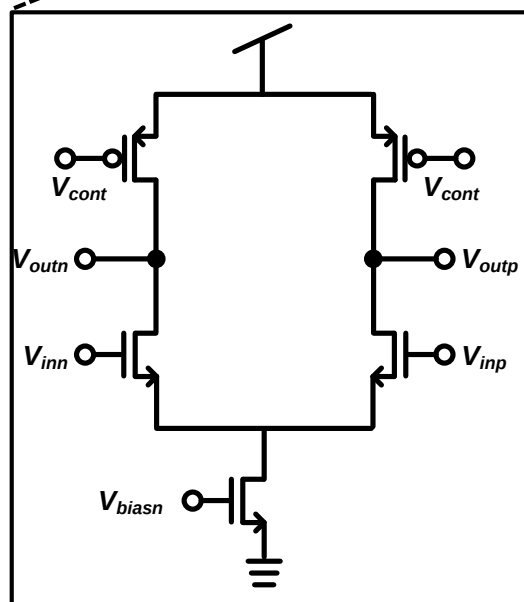
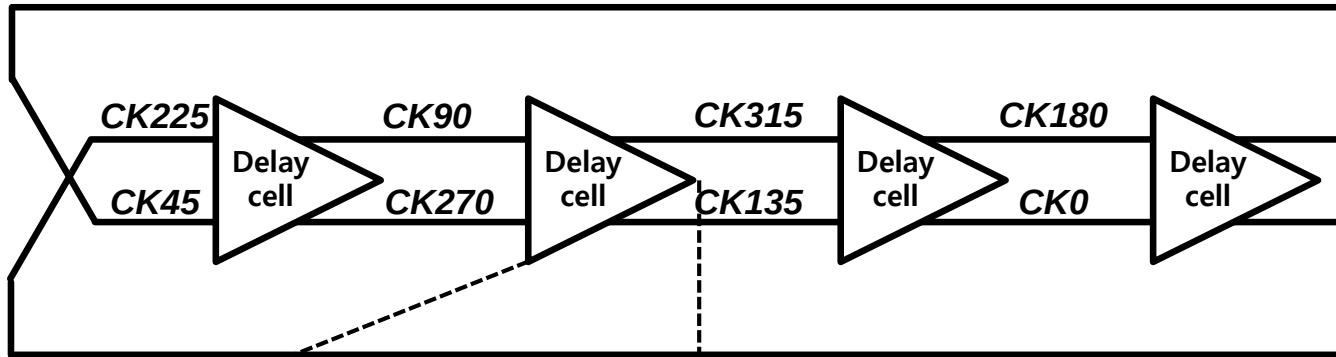
Design Exercise2 – Ring Voltage Controlled Oscillator (VCO)

Design Example

- ✓ 8-phase, 4-stage voltage controlled oscillator (VCO)
 - Supply voltage: 1.8V
 - Minimum voltage swing: 300mV
 - Frequency tuning range: 100 ~ 200 MHz
with range of V_{cont} as 0~0.5V
 - Oscillation frequency : 700 ~ 900 MHz

Oscillator Structure

- ✓ 4-stage Ring VCO using differential delay cell



$$\omega_0 = \frac{1}{RC}$$

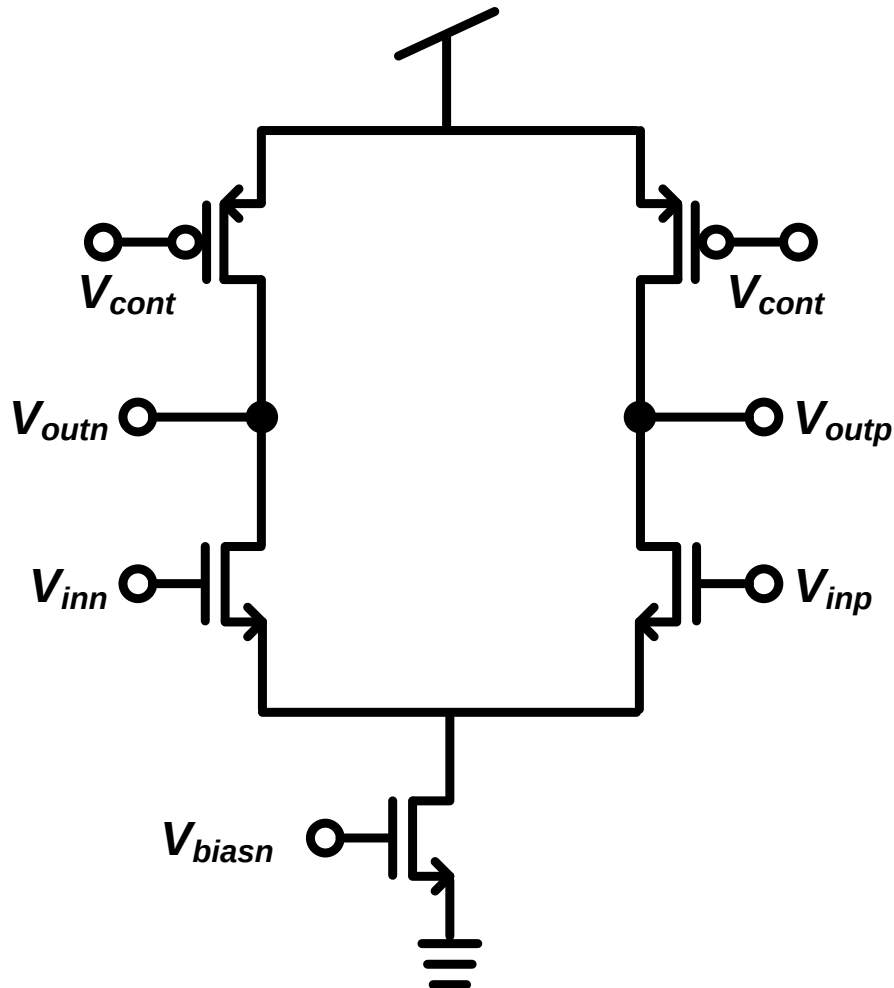
$$R_{on} = \frac{1}{\mu_n C_{ox} W/L (V_{gs} - V_{th})}$$

$$H(s) = \frac{A_0^4}{\left(1 + \frac{s}{\omega_0}\right)^4} \quad / \quad \tan^{-1} \frac{\omega_{osc}}{\omega_0} = 45^\circ$$

$$\Rightarrow \omega_{osc} = \omega_0 (A_0 = \sqrt{2})$$

Details of Delay Cell

✓ Differential type delay cell



► PMOS

- Length : 1u
- Width : 40u (finger : 4)

► INPUT NMOS

- Length : 0.180u
- Width : 20u (finger : 2)

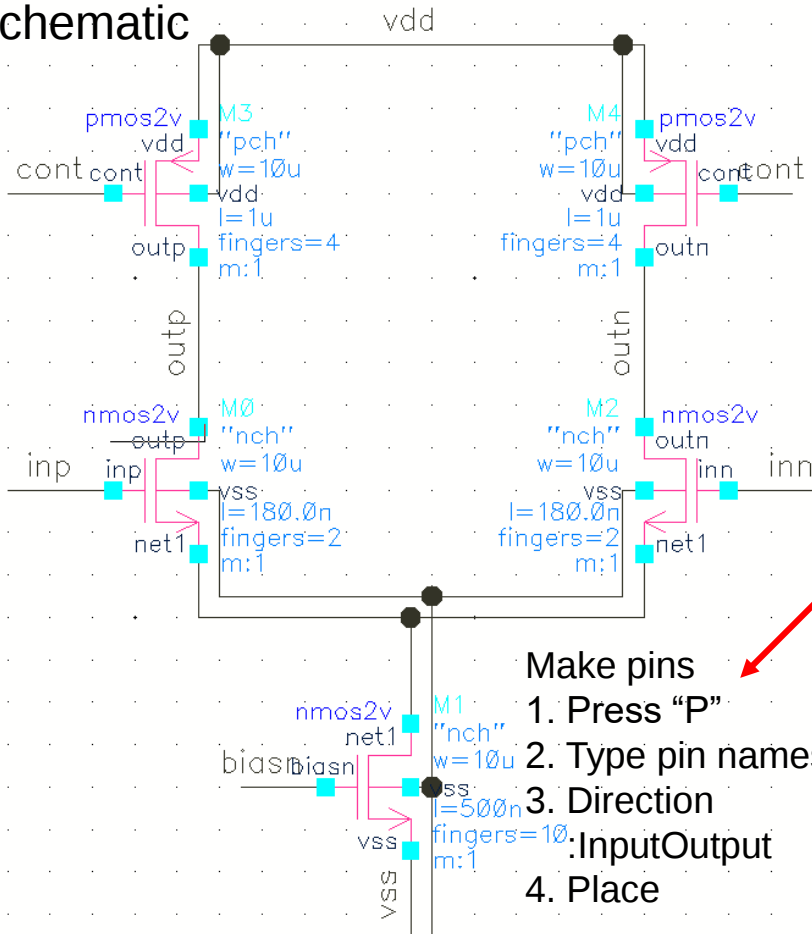
► Source NMOS

- Length : 0.500u
- Width : 100u (finger : 10)

► $V_{biasn} = 600 \text{ mV}$

Schematic & Symbol of Delay Cell

① Schematic



Pins

vdd
vss

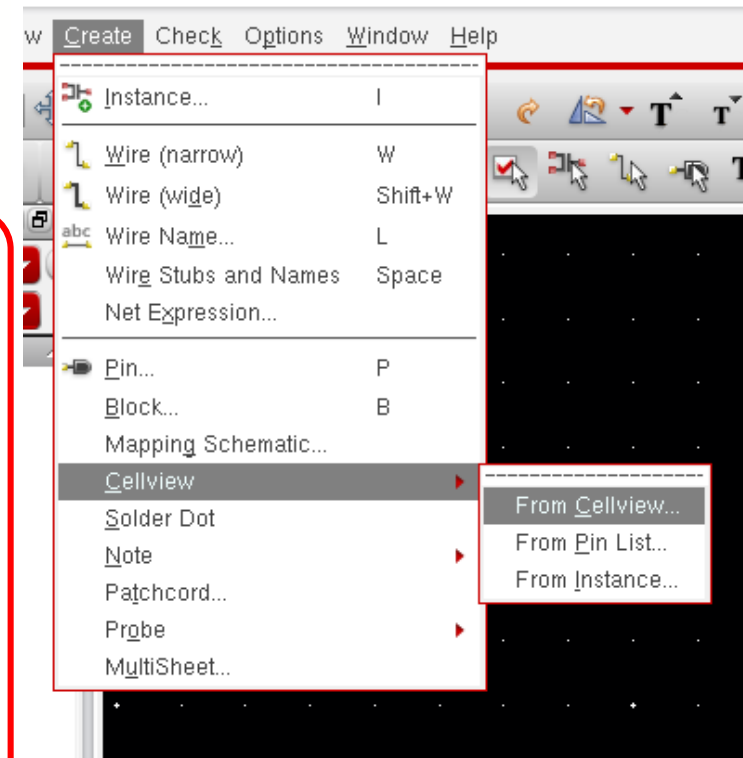
inp
inn

outp
outn

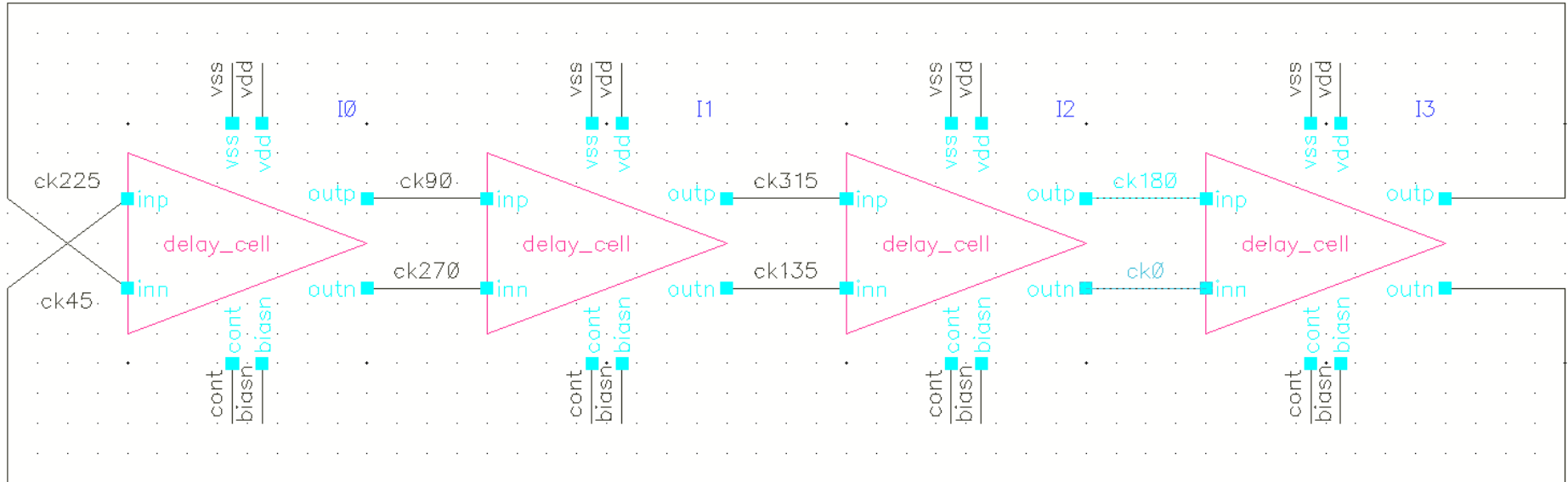
cont
biasn

② Make symbol of schematic

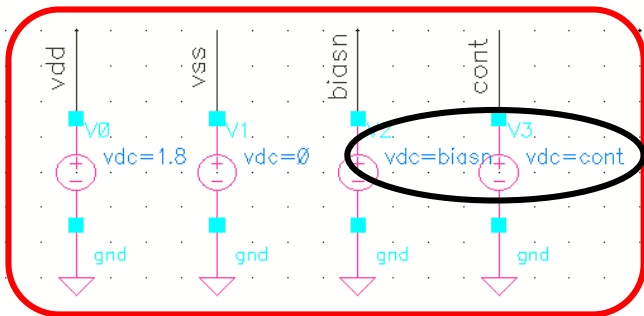
tor L Editing: Week2_pre delay_cell schematic



Simulation Testbench Schematic



Sources

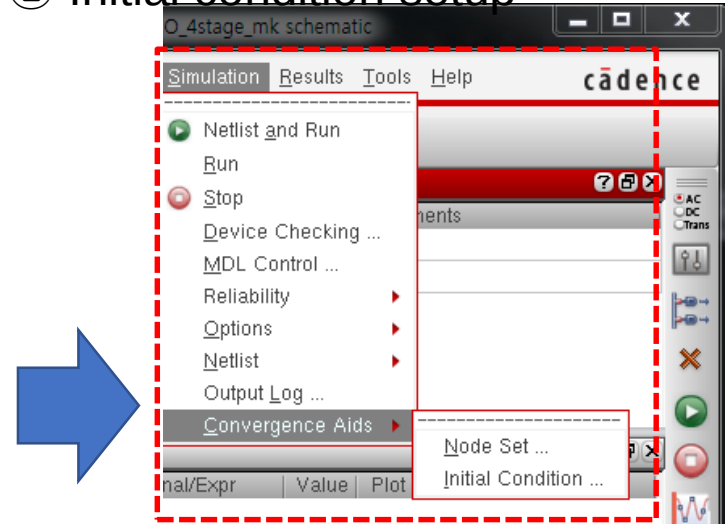
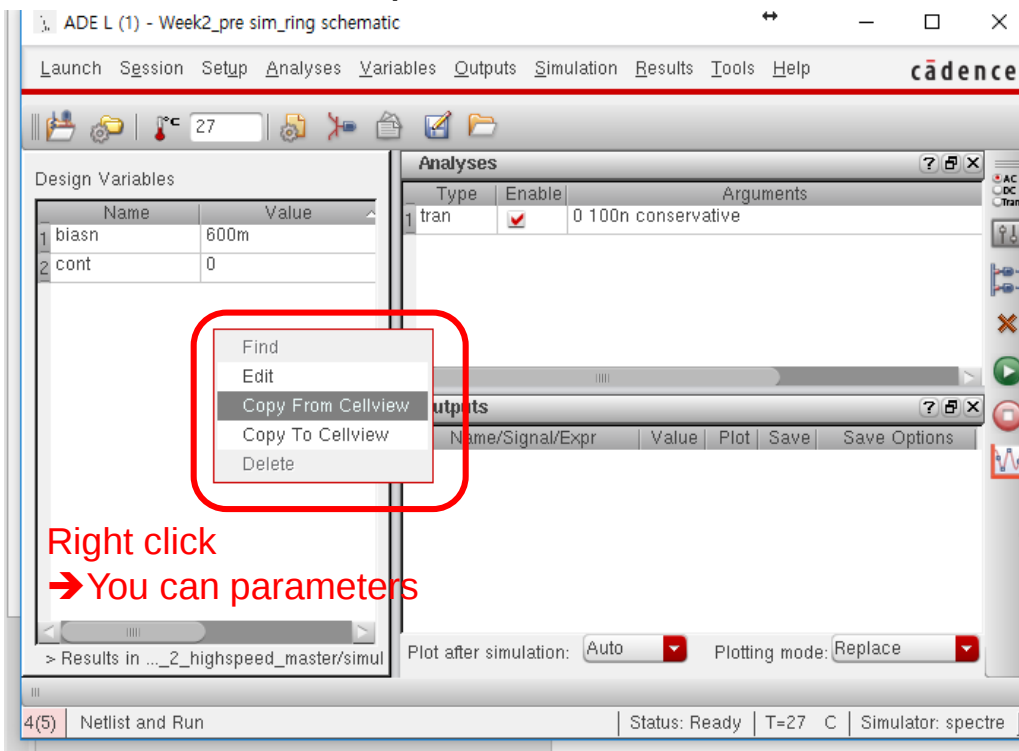


You can parameterize values using text for your convenience

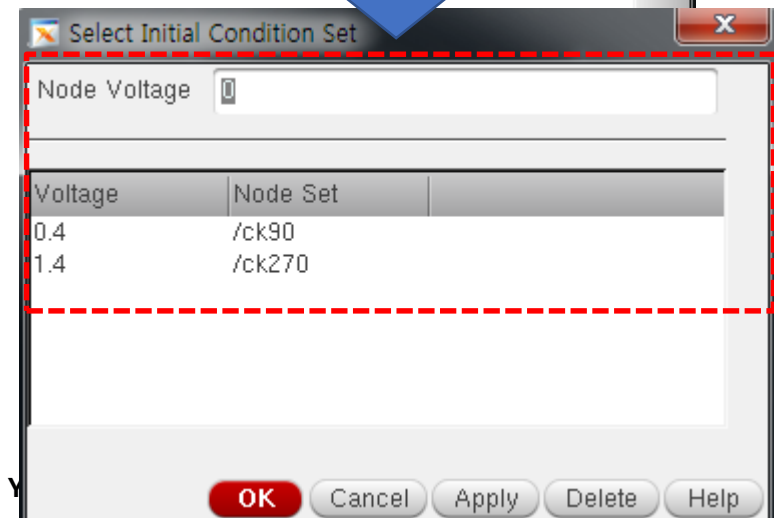
Transient Simulation

② Initial condition setup

① Simulation setup

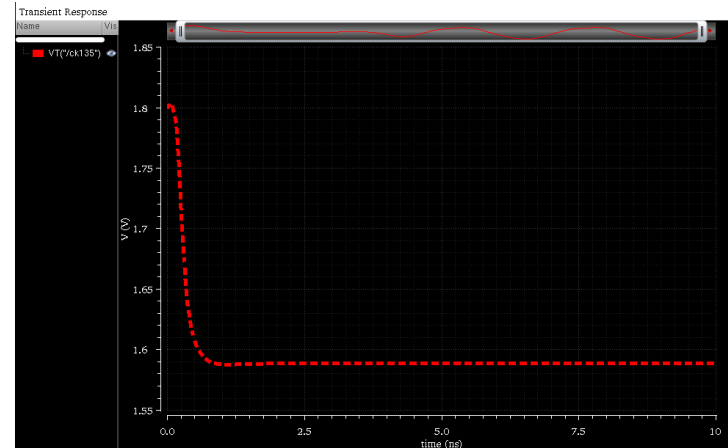
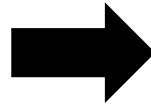
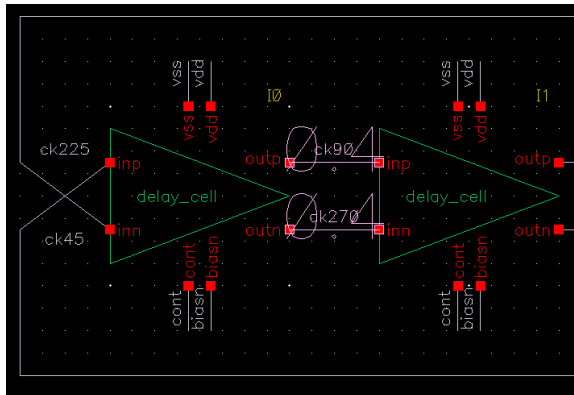


③ Initial condition

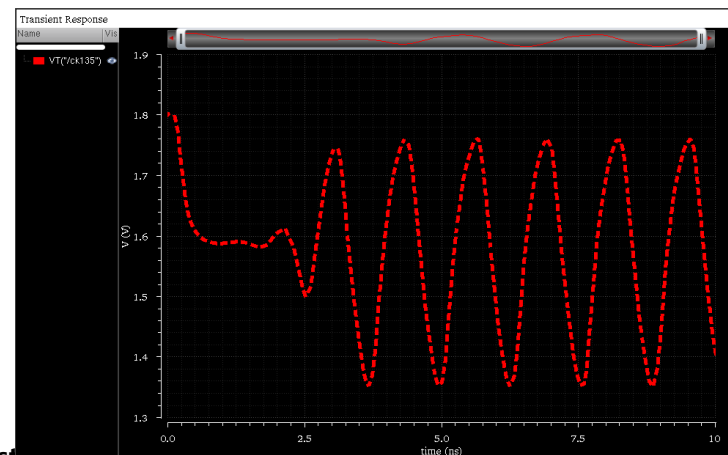
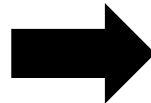
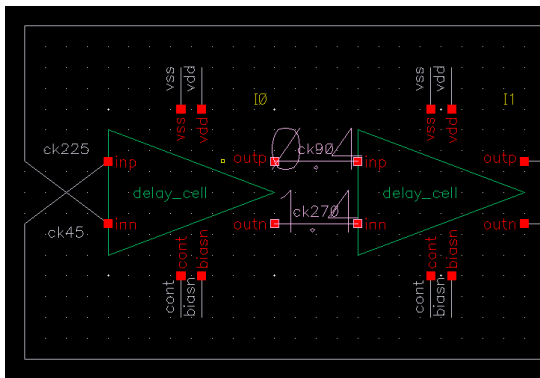


Initial Condition Value Examples

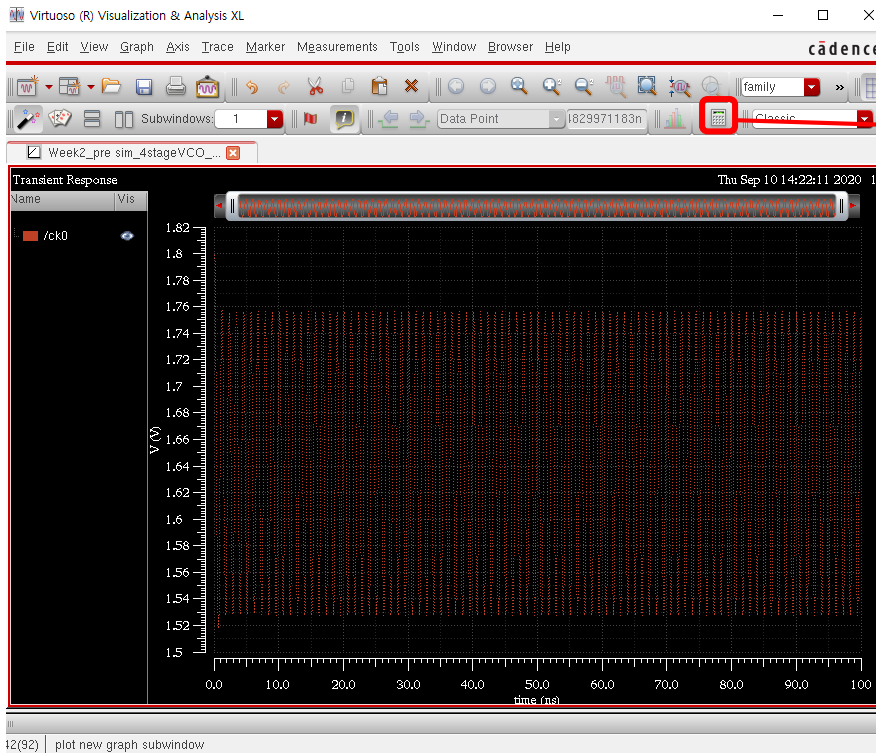
- ✓ Initial condition change
 - CK90 : 0.1V & CK270 0.1V



- CK90 : 0.4V & CK270 1.4V



Frequency calculation



In Context Results DB: 4stageVCO_tran/spectre/schematic/psf

Key ...: frequency(v("/ck0") ?result "tran")

Stack:

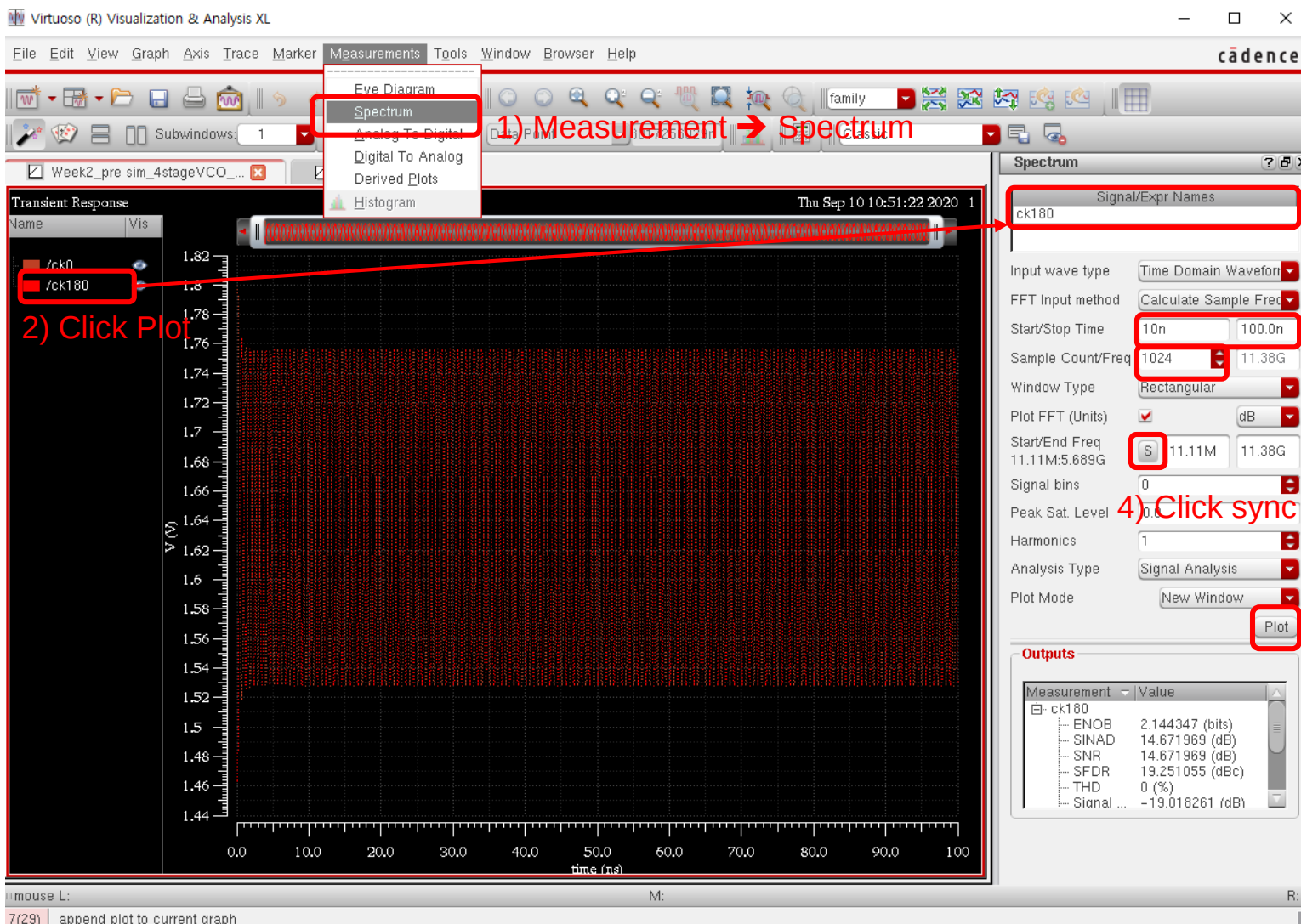
- 901.1E6
- frequency(getData("/ck0" ?result "tran"))
- getData("/ck0" ?result "tran")
- dB20(getData("/C_D" ?result "ac"))
- dB20(getData("/C_D" ?result "ac"))

Function Panel:

- freq
- freq_jitter
- nc_freq
- unityGainFreq
- frequency
- gac_freq
- gpc_freq
- harmonicFreq
- lfreq

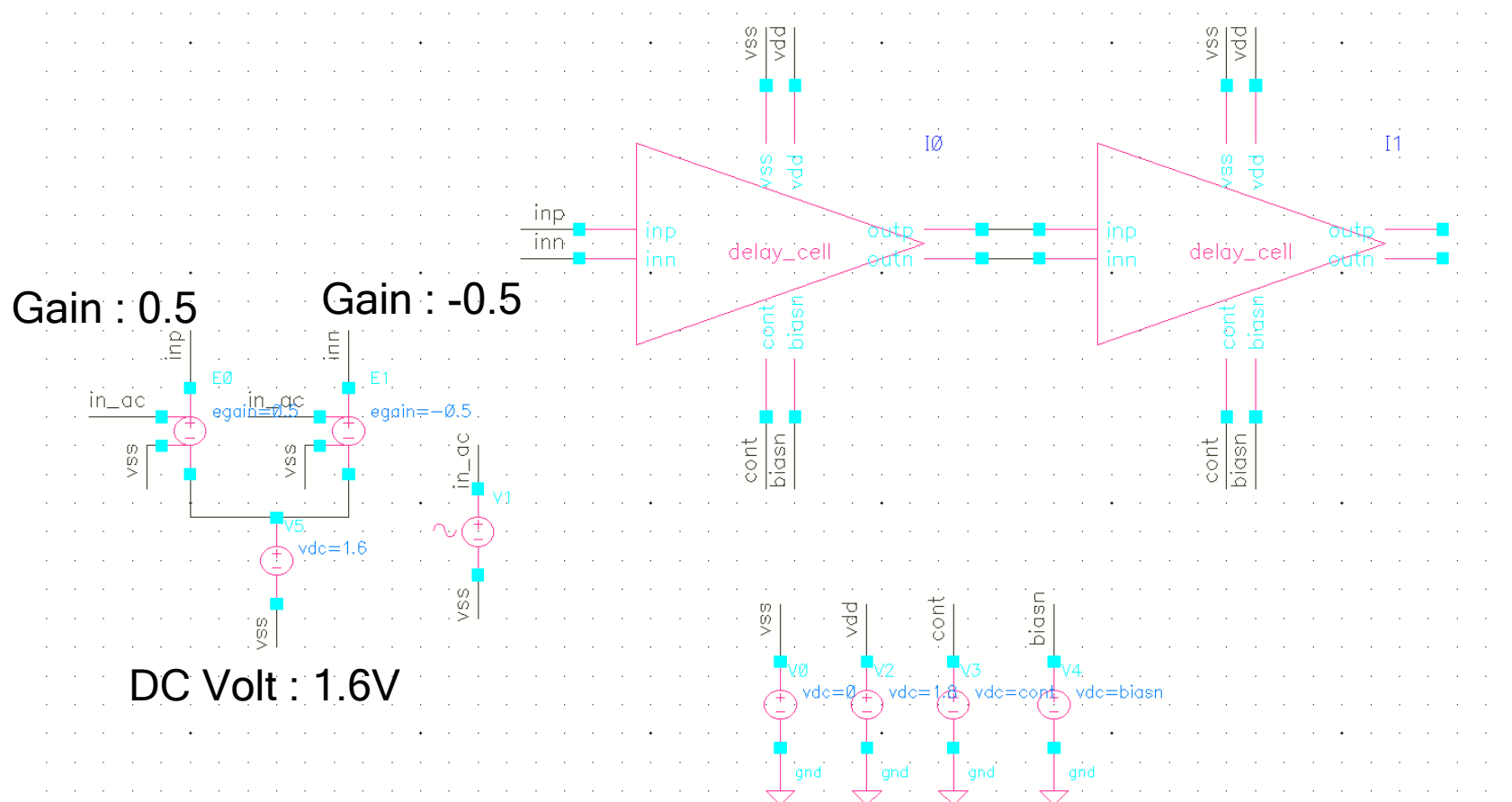
Trace: /ck0; Context: /class/2020_2_highspeed/2020_2_hs_master/simulation

Spectrum Analysis

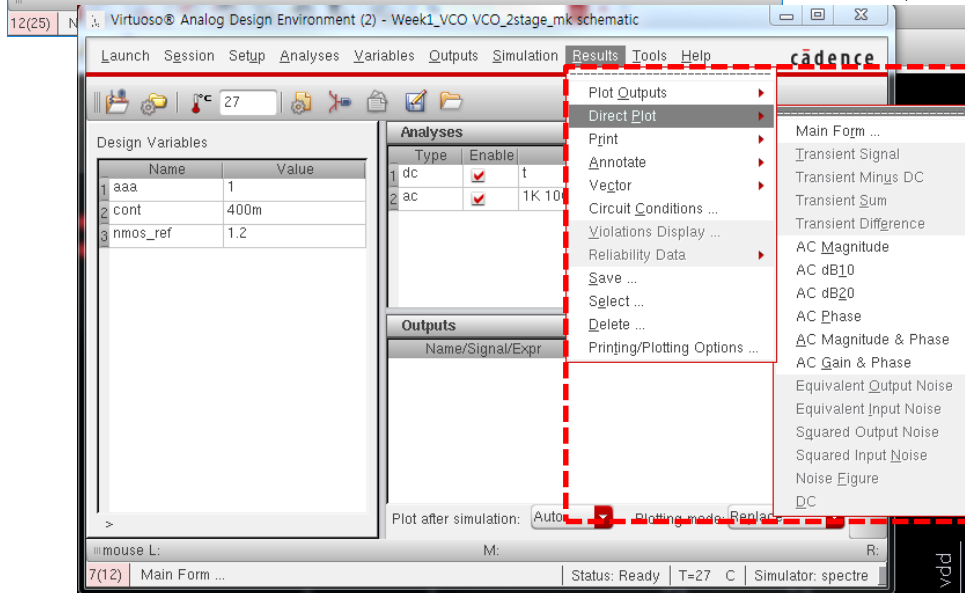
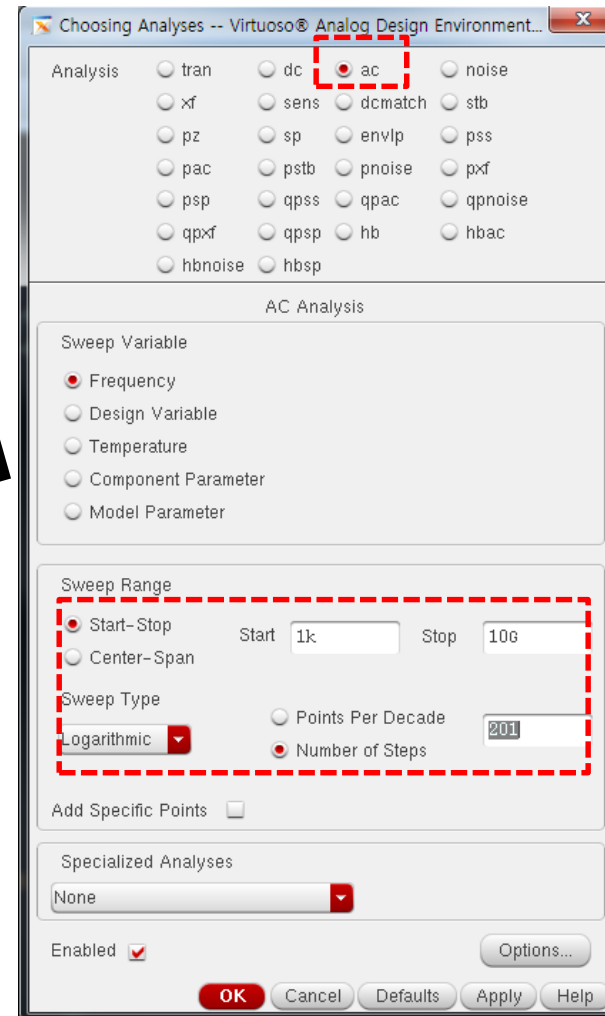
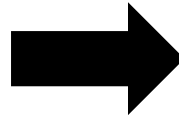
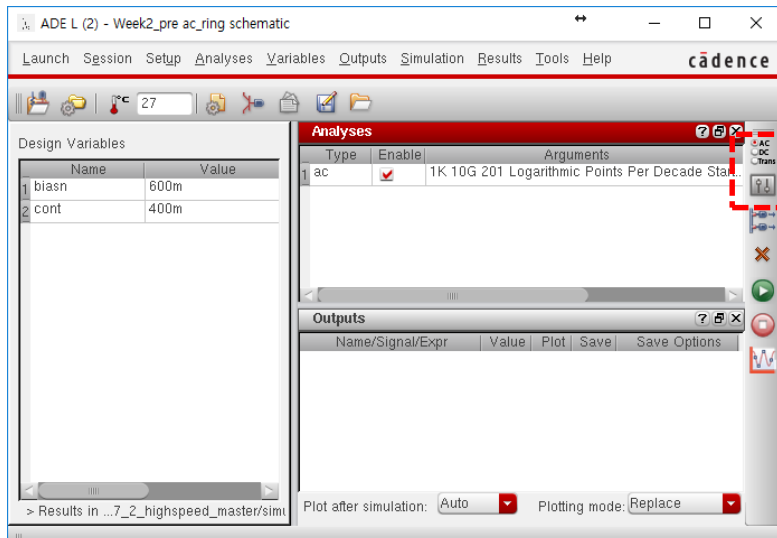


Small-Signal Simulation (AC)

- ✓ Schematic design
 - 2-stage delay cell 구성
 - Vsin source 이용 (AC magnitude 1)

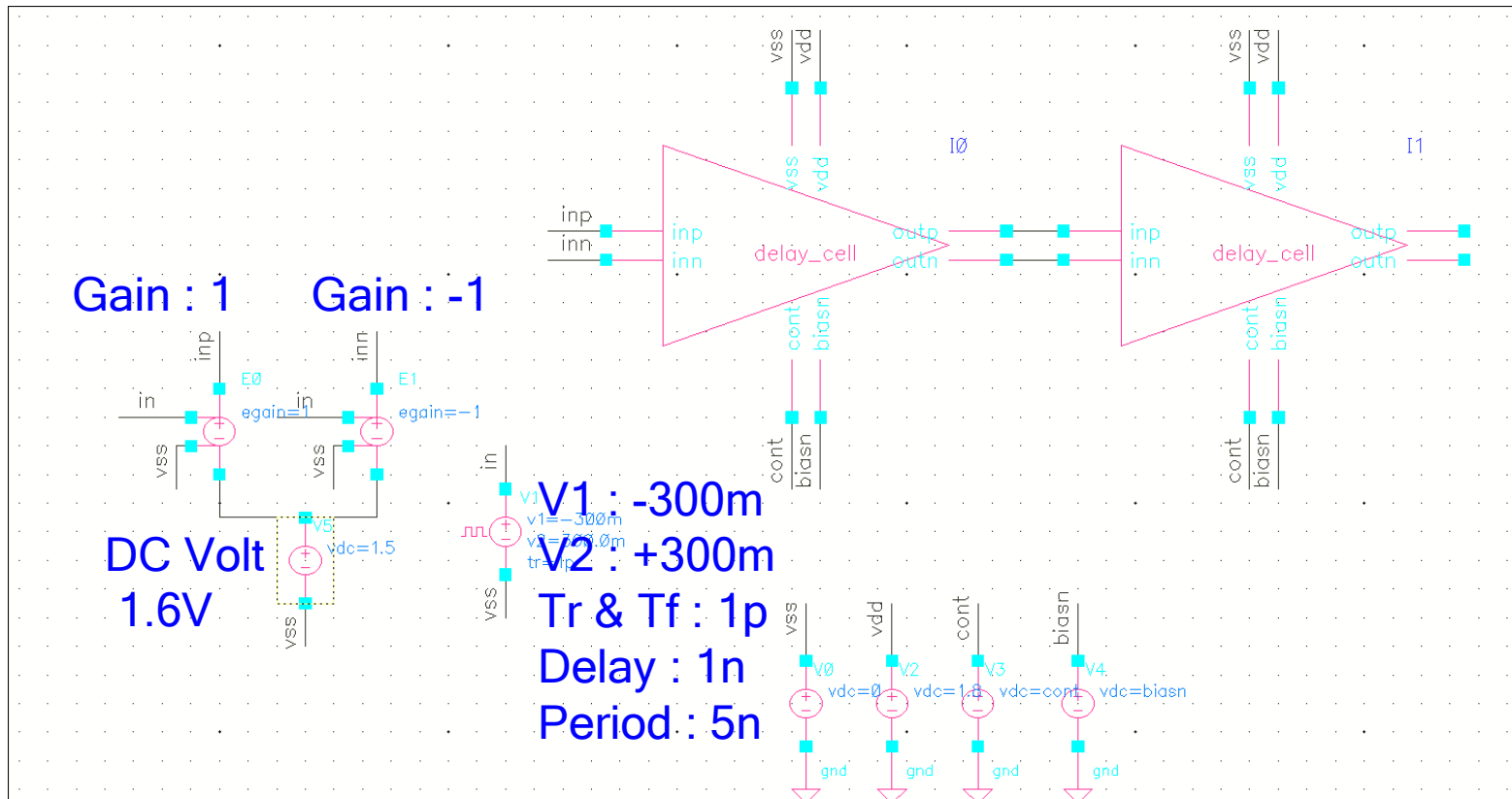


AC Simulation



Pulse Response Simulation

- ✓ Schematic design
 - 2-stage delay cell 구성
 - Vpulse source 이용



Parameter Sweep

The image shows two windows from the Cadence ADE L environment. The top window is titled 'ADE L (10) - Week2_pre sim_4stageVCO_tran schematic'. It displays the 'Design Variables' table and the 'Analyses' table. The 'Tools' menu is open, showing 'Parametric Analysis ...' as the selected option. A large black arrow points from this menu item to the bottom window.

The bottom window is titled 'Parametric Analysis - spectre(9): Week2_pre sim_4stageVCO_tran schematic'. It shows the 'Parametric Simulation Completed' dialog. The 'Sweeps & Ranges' tab is active, displaying a table with the following data:

Variable	Value	Sweep?	Range Type	From	To	Step Mode	Step Size
cont	0	☒	From/To	0	0.5	Linear Steps	0.05

The status bar at the bottom of the window indicates 'Parametric Simulation Completed' and '78 | Save the specifications to a parametric file'.

Homework

- ✓ Verify and plot 8-phase output of VCO, and derive K_{VCO} by changing V_{cont} from 0V to 0.5V

- ✓ Compare and analyze frequency of oscillator with small-signal analysis (pole, phase response) and large-signal analysis (pulse response) and transient simulation result. (And why K_{VCO} is negative?)

- ✓ Deadline : 09/17(Thu) 19:00
 - Upload pdf file to YSCEC