High-Speed Serial Interface Circuits and Systems

Design Exercise2 –

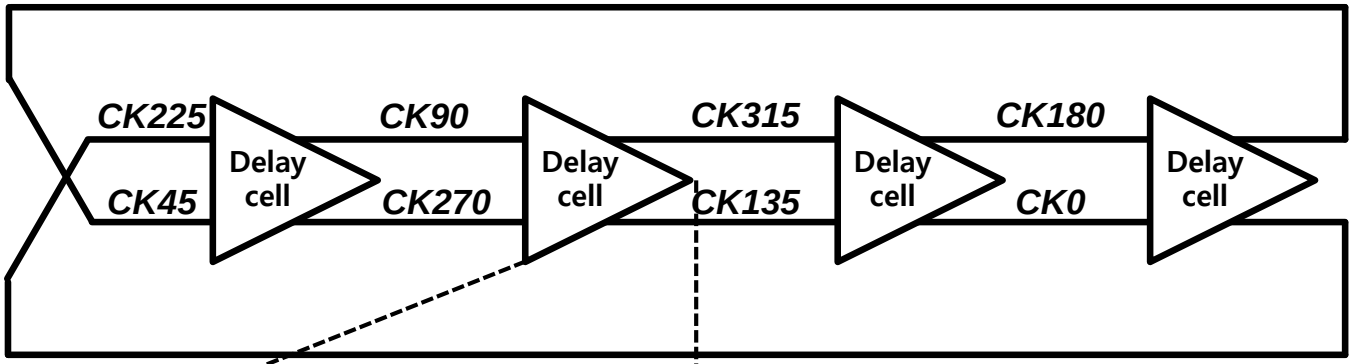
Ring Voltage Controlled Oscillator (VCO)

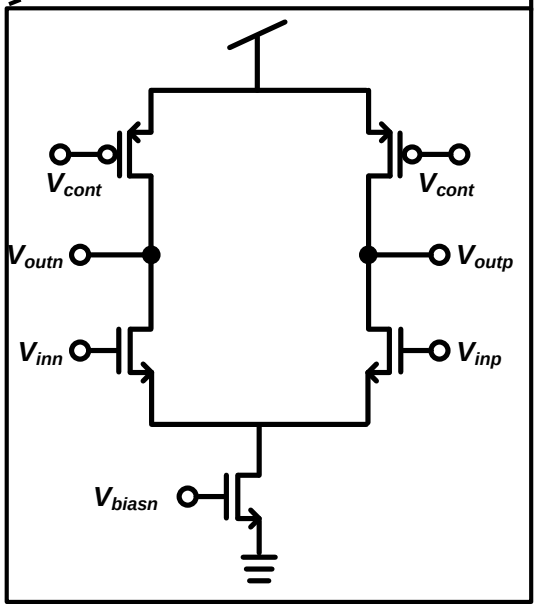
Design Example

- ✓ 8-phase, 4-stage voltage controlled oscillator (VCO)
  - Supply voltage: 1.8V
  - Minimum voltage swing: 300mV
  - Frequency tuning range: 100 ~ 200 MHz
    with range of V_{cont} as 0~0.5V
  - Oscillation frequency : 700 ~ 900 MHz

Oscillator Structure

✓ 4-stage Ring VCO using differential delay cell





$$\omega_0 = \frac{1}{RC}$$

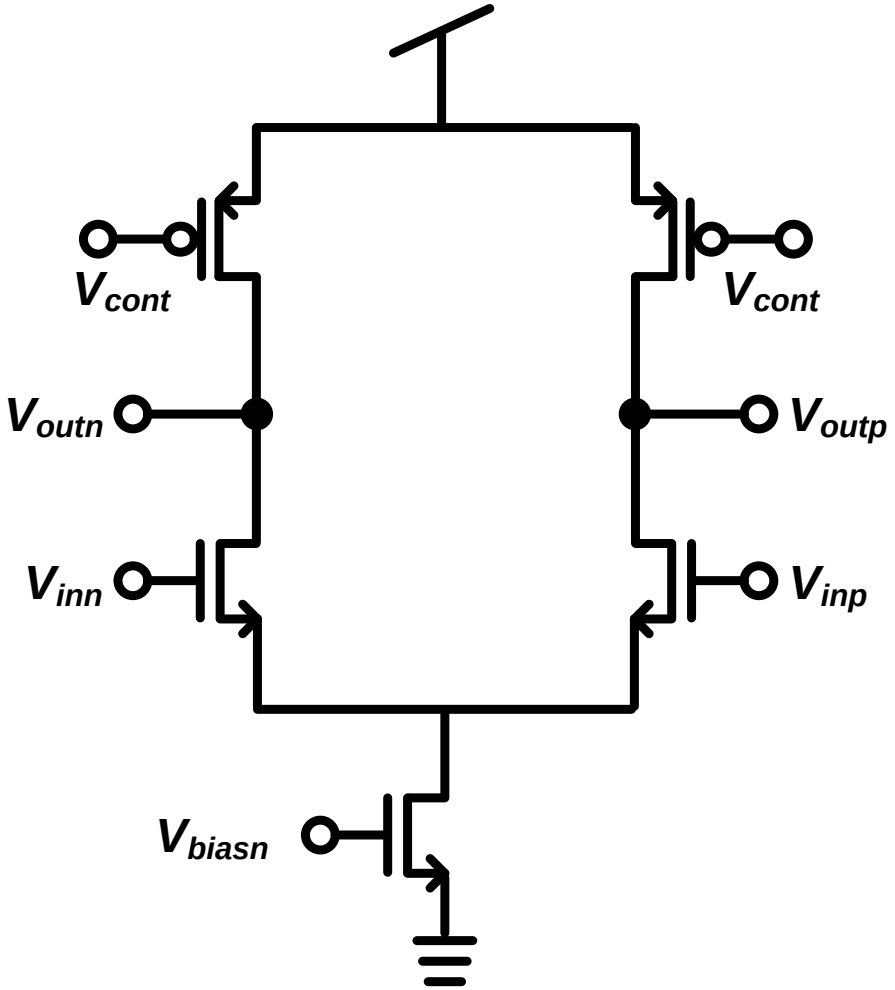
$$\text{Ron} = \frac{1}{\mu_n C_{ox} W/L(Vgs - Vth)}$$

$$H(s) = \frac{A_0^{\,4}}{\left(1+\frac{s}{\omega_0}\right)^4} \quad / \quad \tan^{-1}\frac{\omega_{osc}}{\omega_0} = 45°$$

➔ $\omega_{osc} = \omega_0 (A_0 = \sqrt{2})$

Details of Delay Cell

✓ Differential type delay cell



► PMOS
  – Length : 1u
  – Width : 40u (finger : 4)

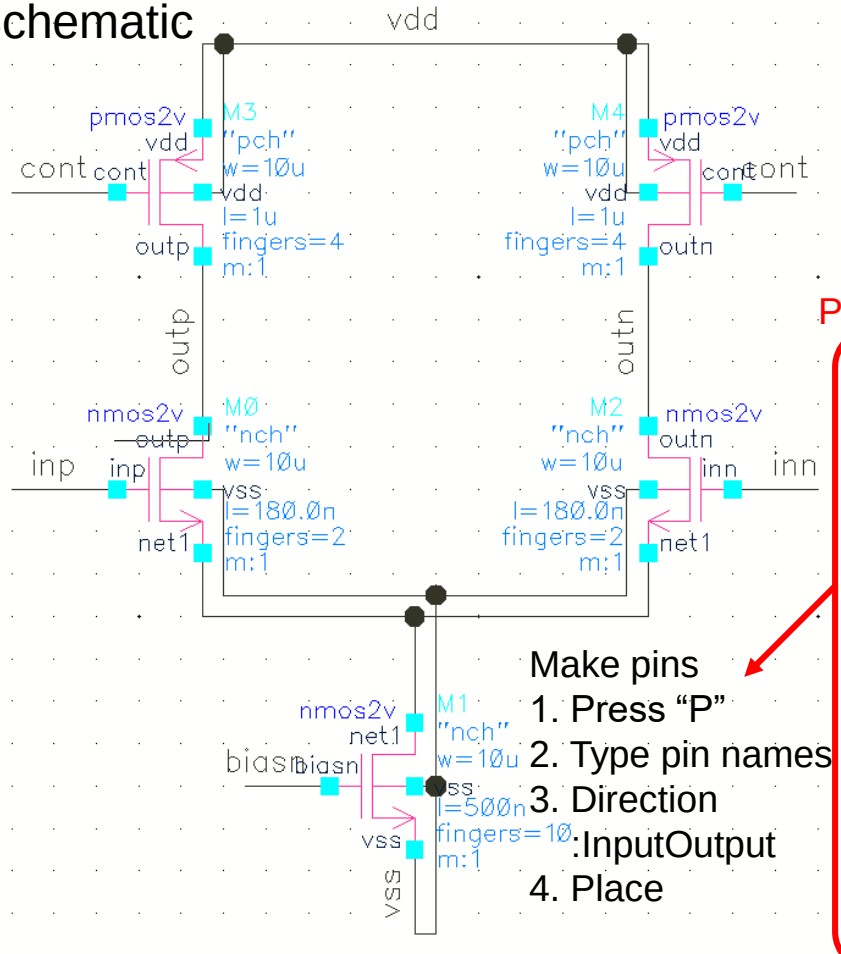
► INPUT NMOS
  – Length : 0.180u
  – Width : 20u (finger : 2)

► Source NMOS
  – Length : 0.500u
  – Width : 100u (finger : 10)

► V_{biasn} = 600 mV

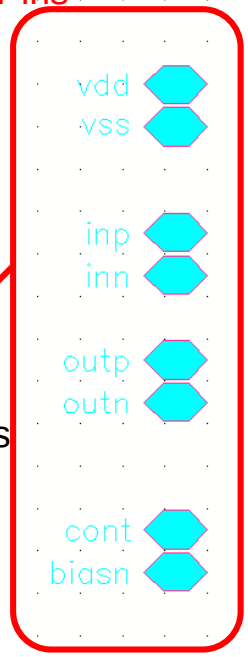
Schematic & Symbol of Delay Cell

① Schematic

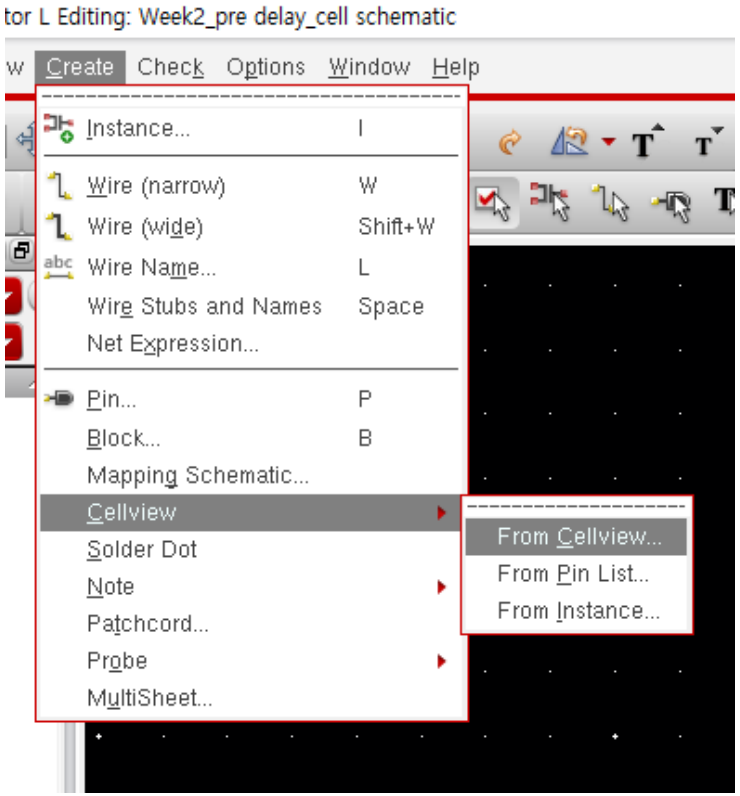


Make pins
1. Press “P”
2. Type pin names
3. Direction
:InputOutput
4. Place

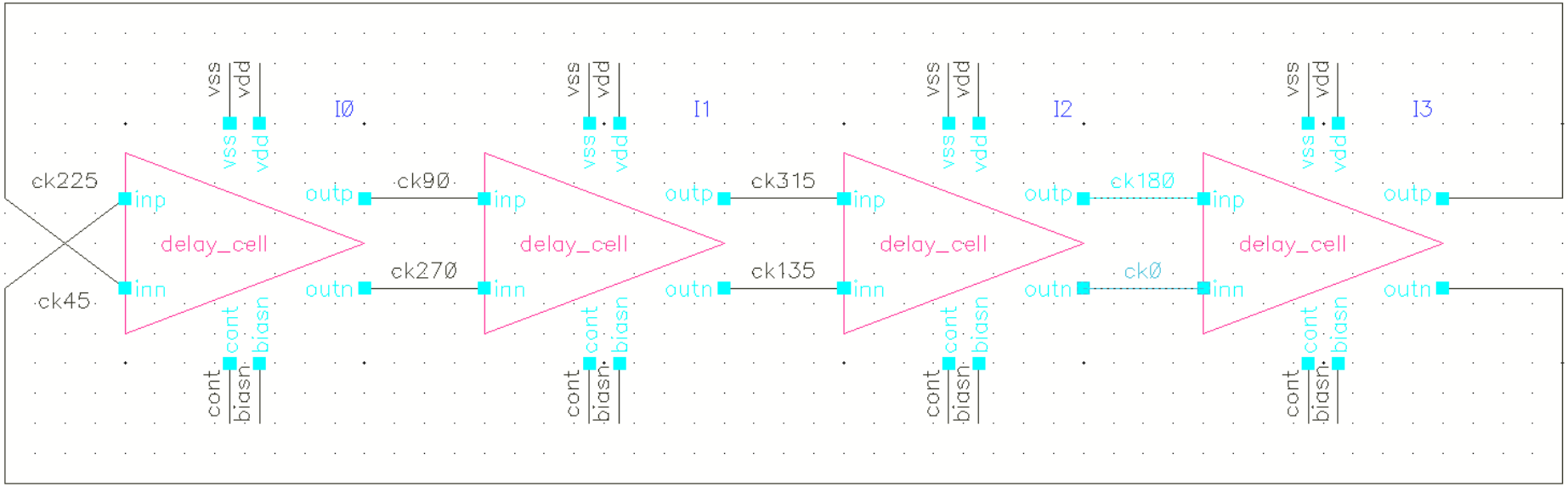
Pins



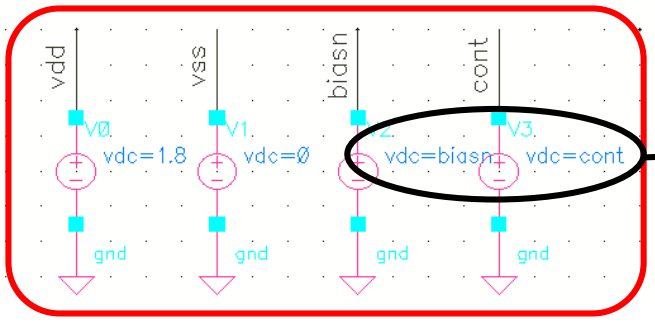
② Make symbol of schematic



Simulation Testbench Schematic



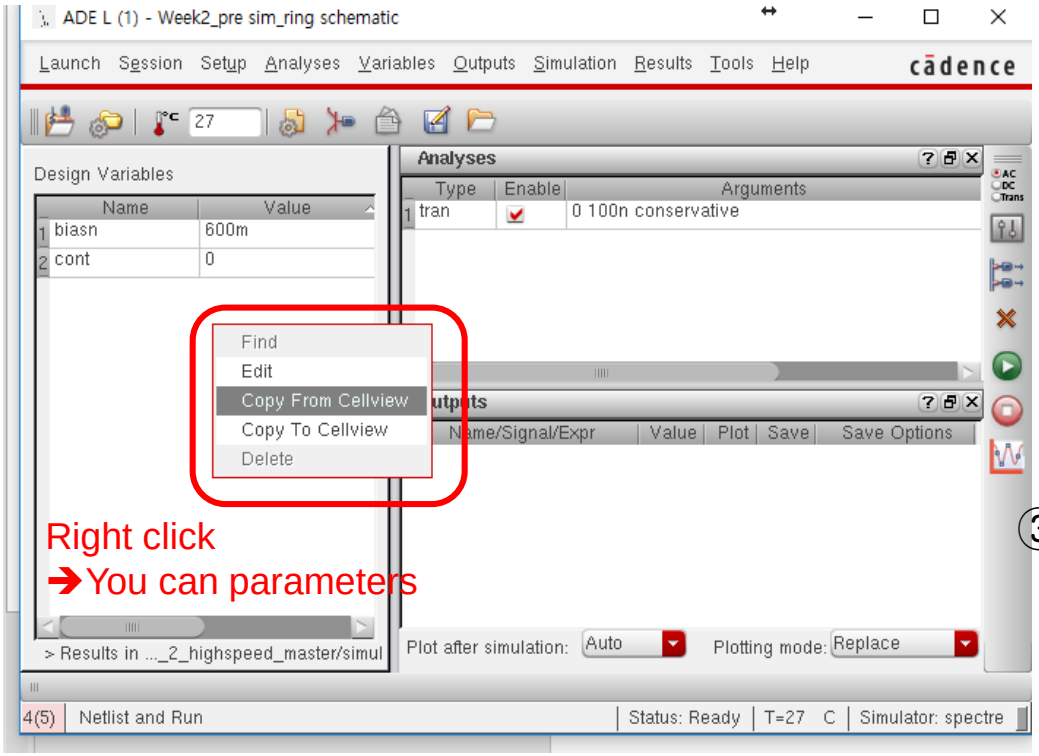
Sources



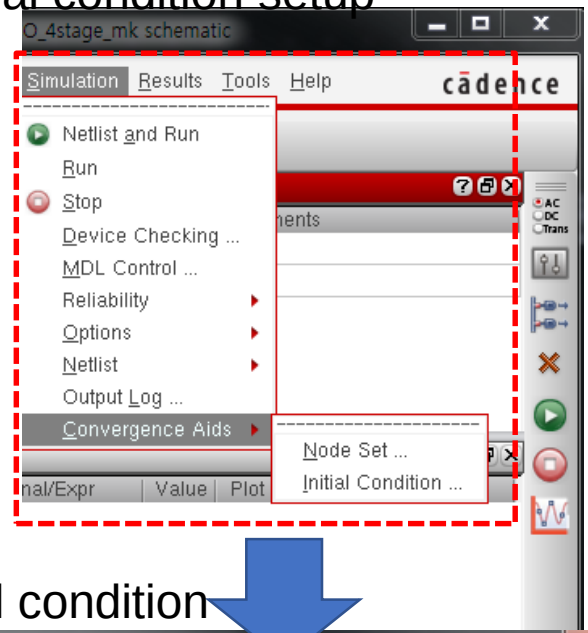
You can parameterize values using text for your convenience

Transient Simulation

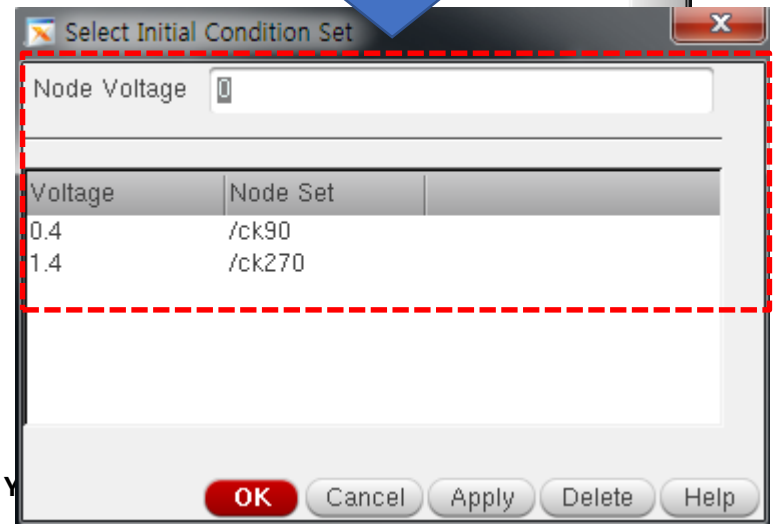
① Simulation setup



② Initial condition setup

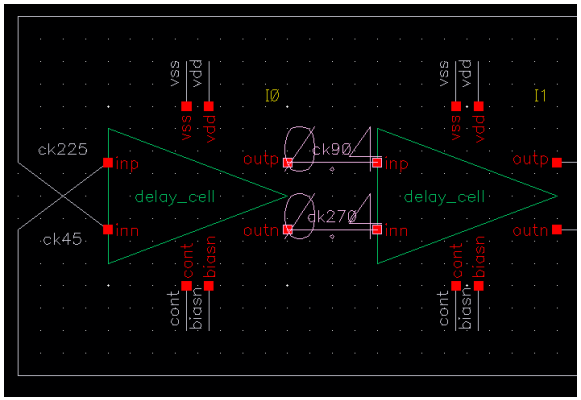


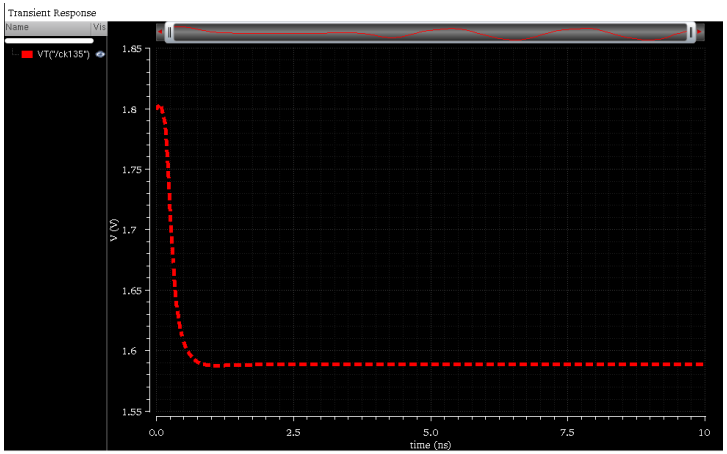
③ Initial condition



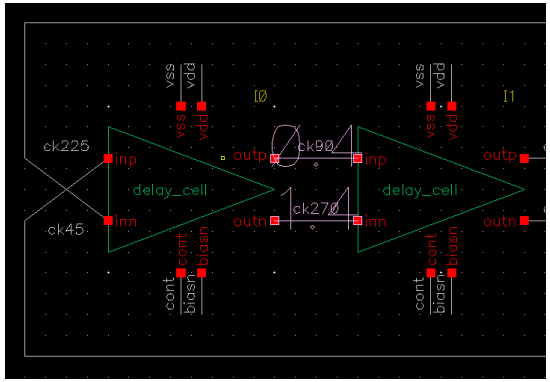
Initial Condition Value Examples

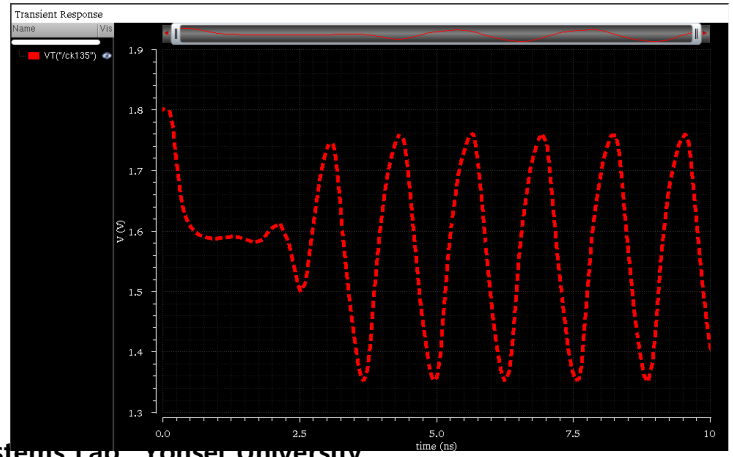
- ✓ Initial condition change
  - CK90 : 0.1V & CK270 0.1V



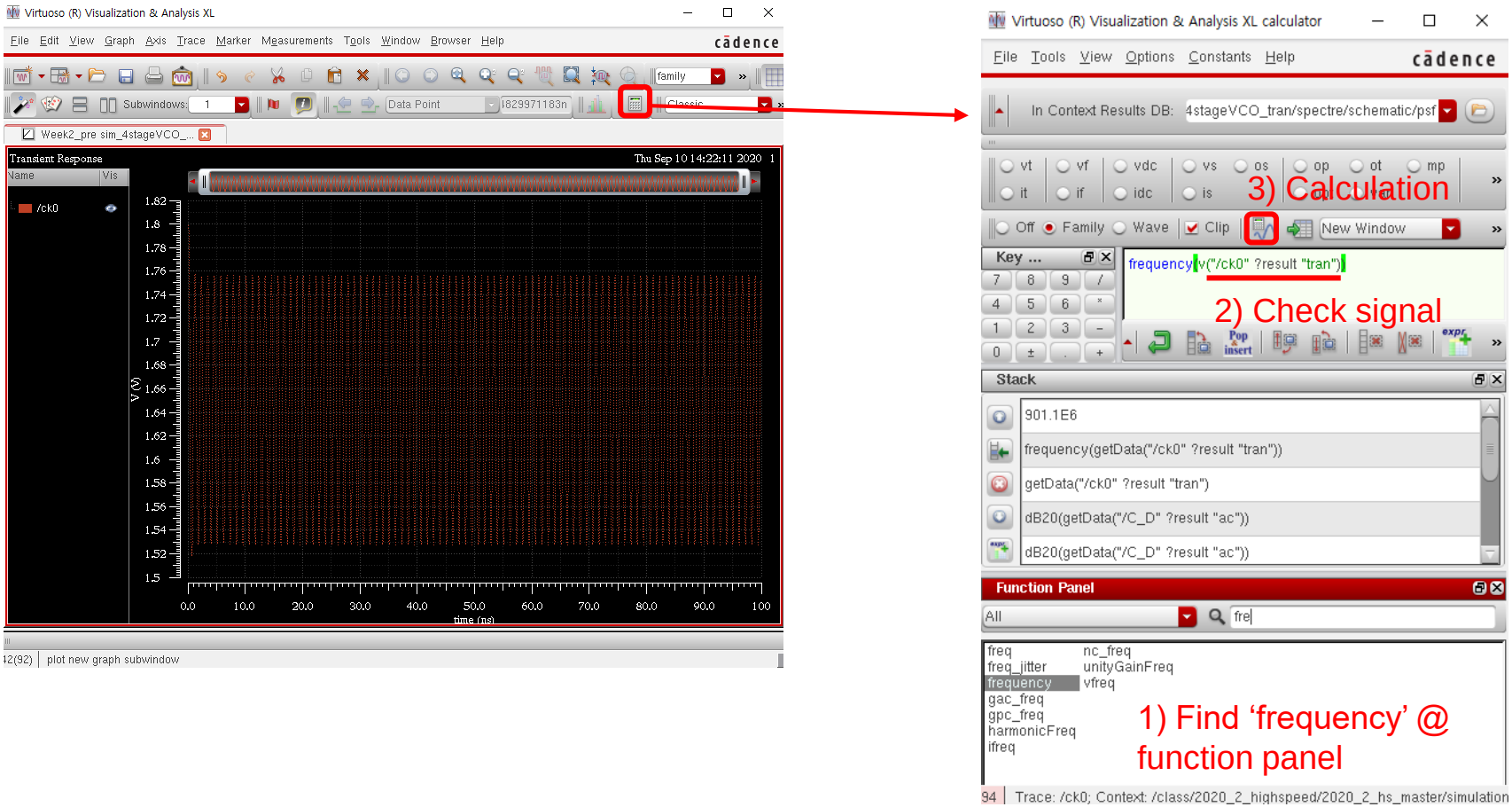


  - CK90 : 0.4V & CK270 1.4V

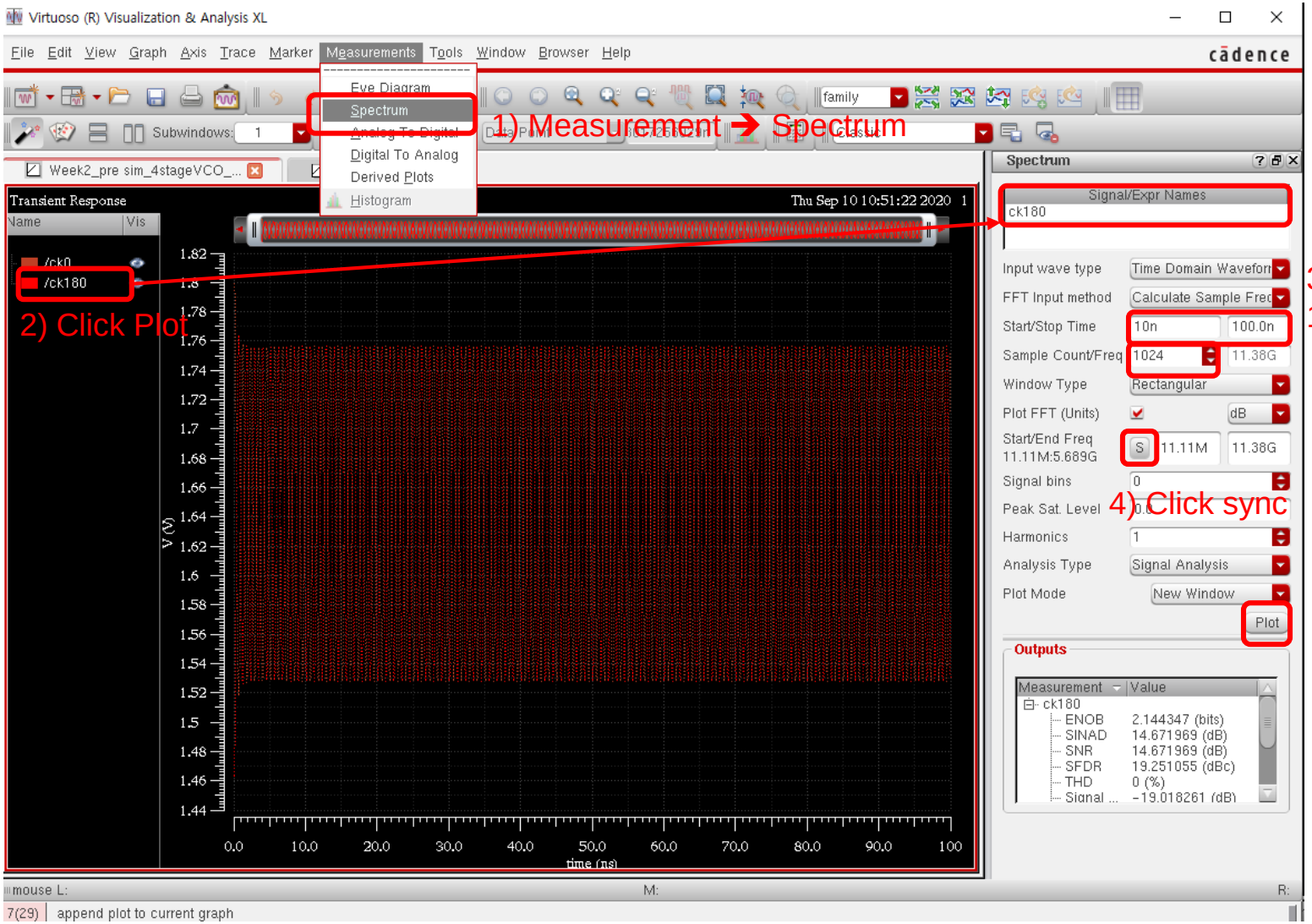




Frequency calculation

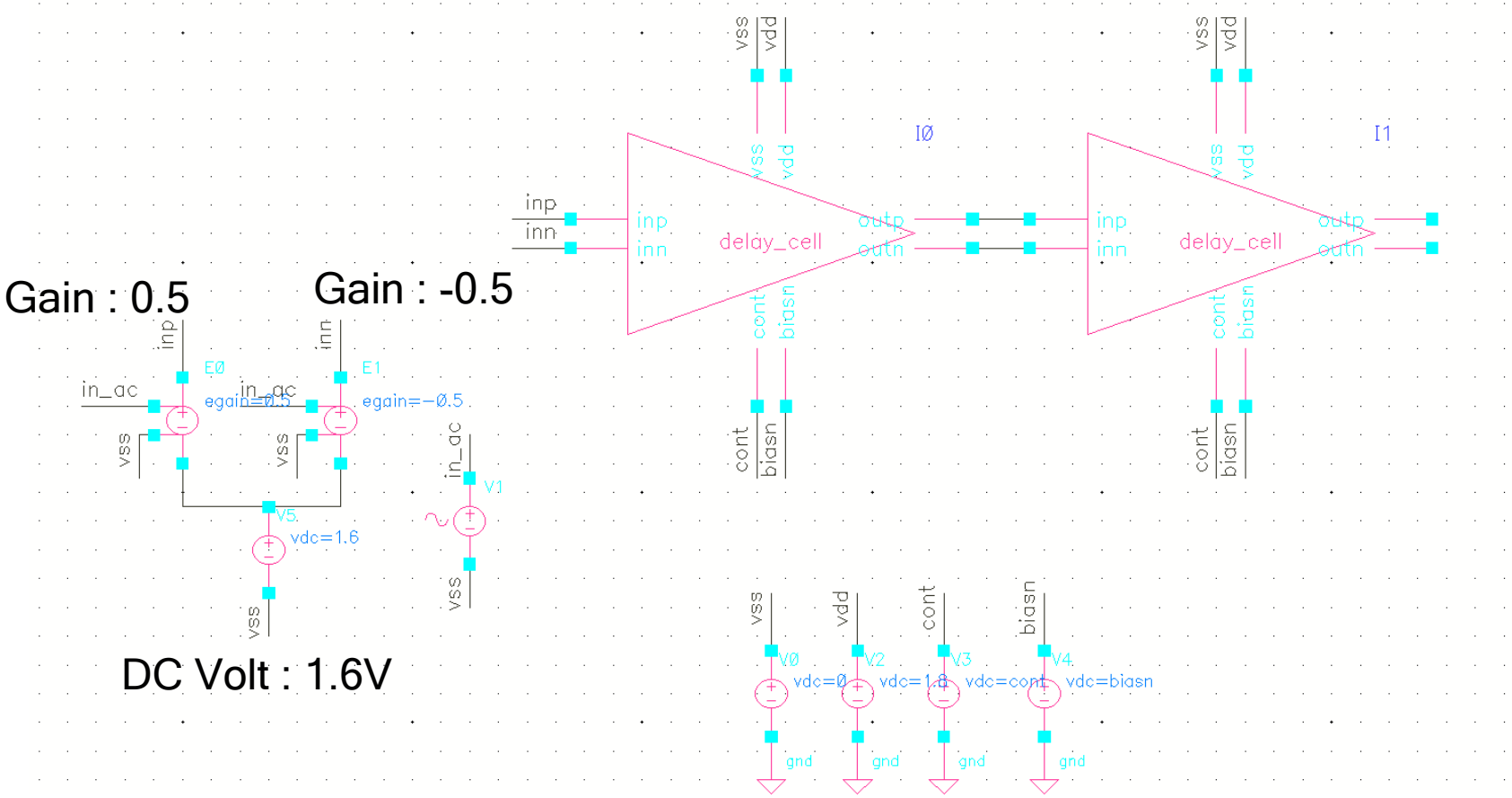


Spectrum Analysis

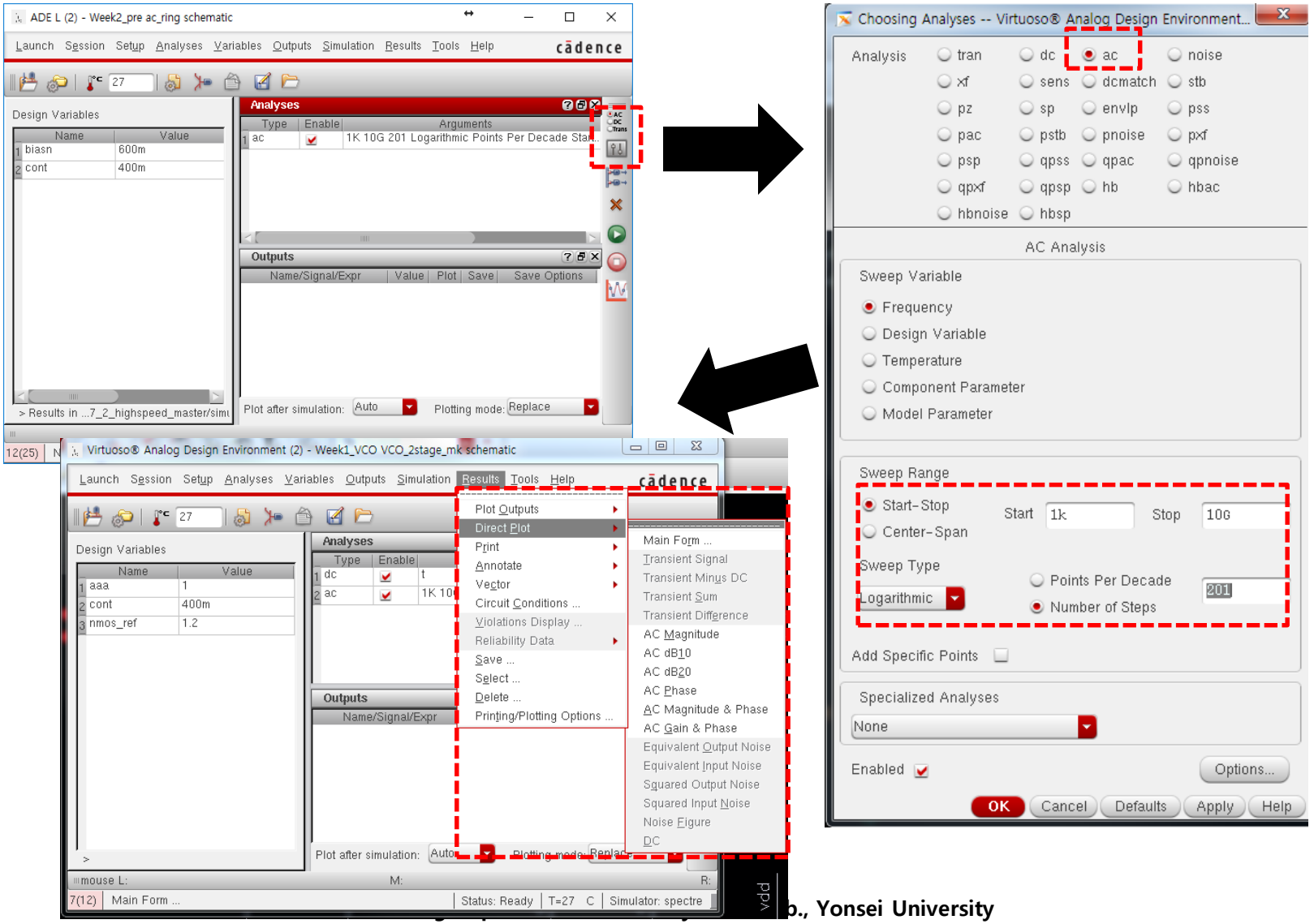


Small-Signal Simulation (AC)

- ✓ Schematic design
  - 2-stage delay cell 구성
  - Vsin source 이용 (AC magnitude 1)

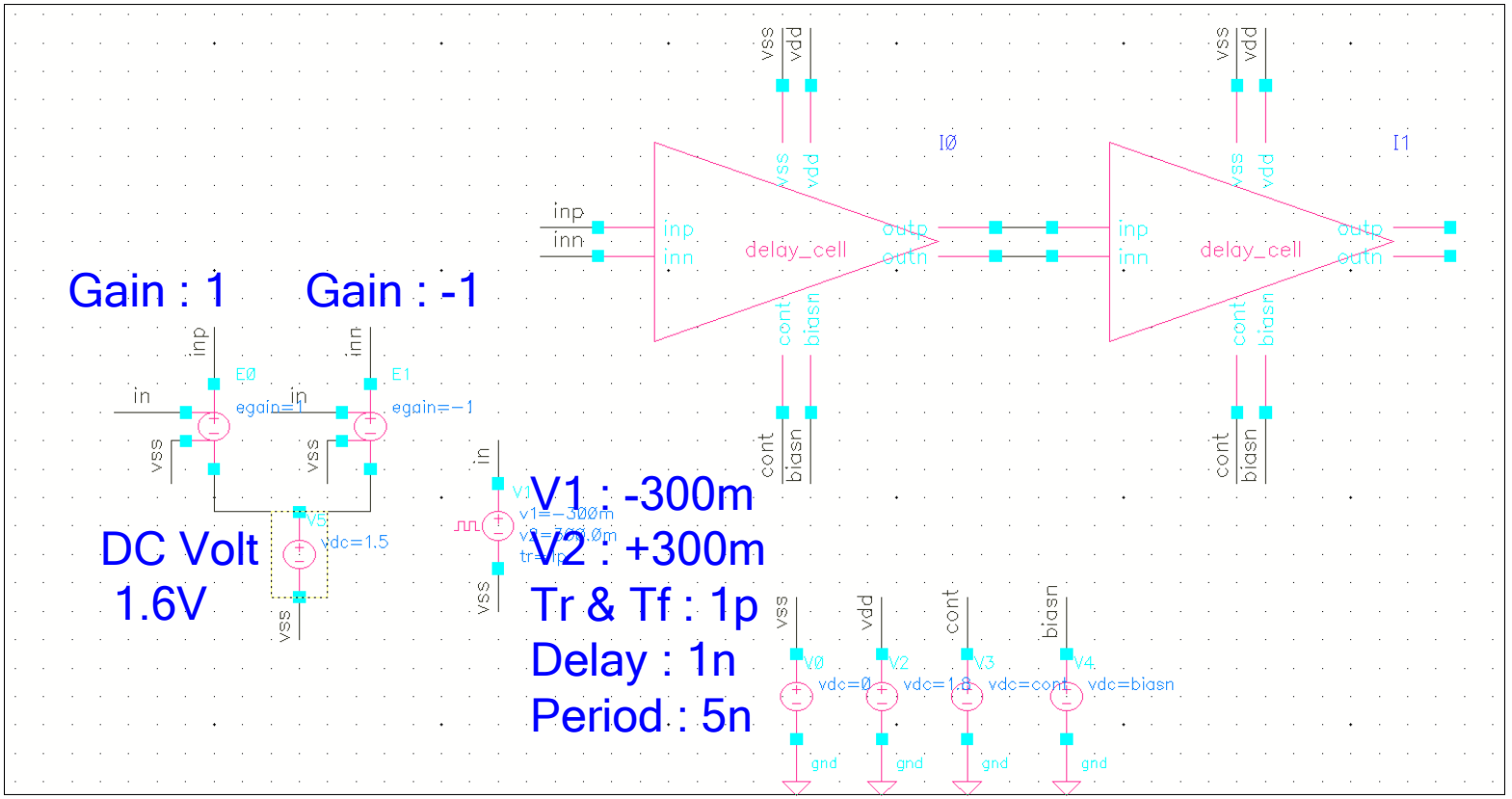


AC Simulation

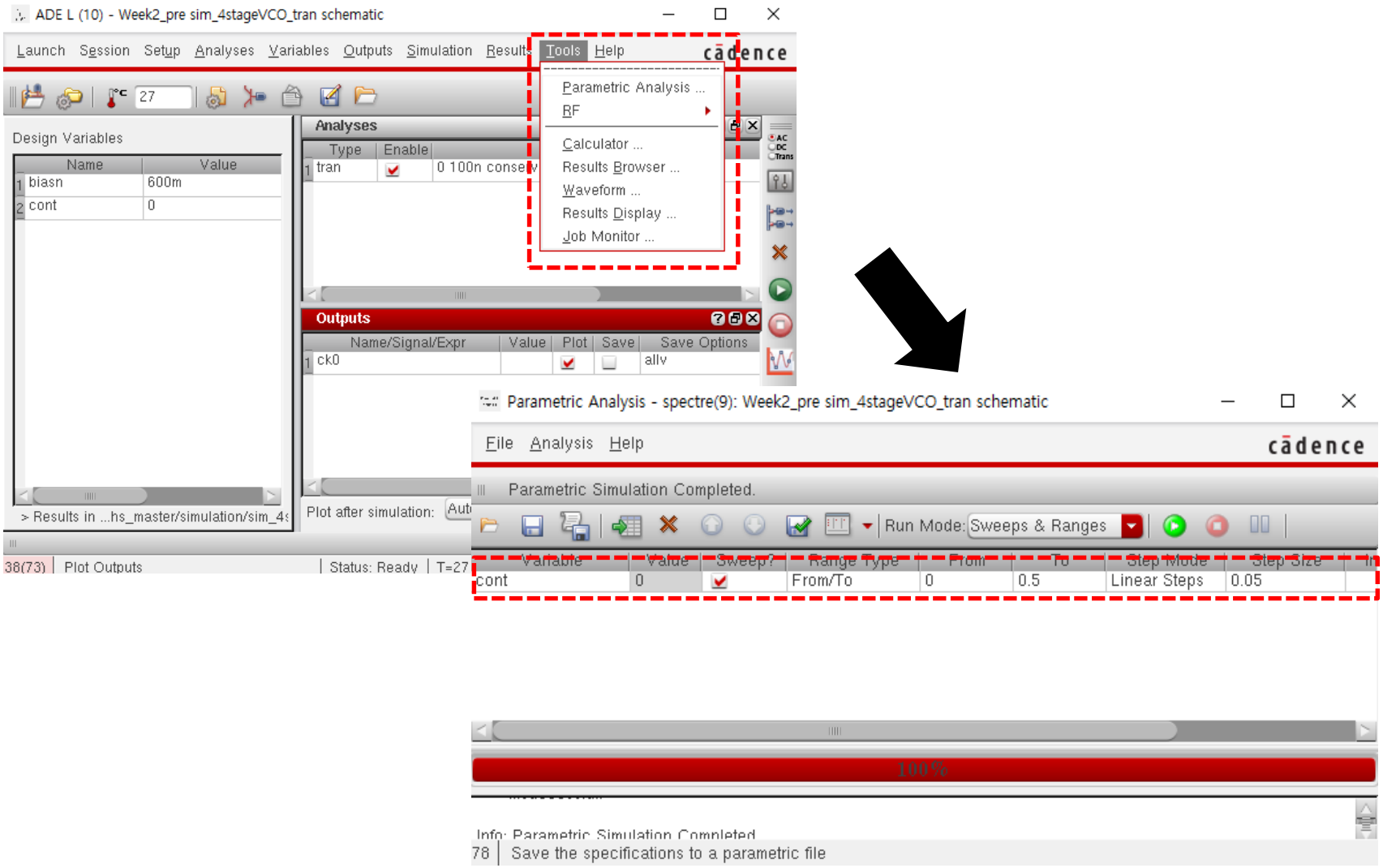


Pulse Response Simulation

- ✓ Schematic design
  - 2-stage delay cell 구성
  - Vpulse source 이용



Parameter Sweep



Homework

- ✓ Verify and plot 8-phase output of VCO, and derive K_{VCO} by changing V_{cont} from 0V to 0.5V

- ✓ Compare and analyze frequency of oscillator with small-signal analysis (pole, phase response) and large-signal analysis (pulse response) and transient simulation result. (And why K_{VCO} is negative?)

- ✓ Deadline : 09/17(Thu) 19:00
  - ➢ Upload pdf file to YSCEC