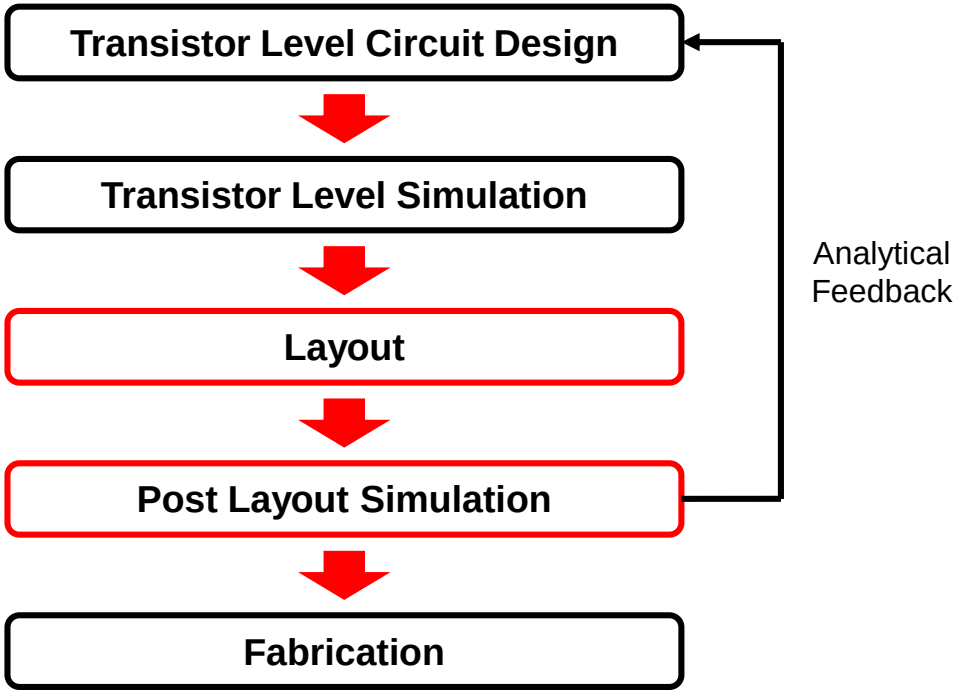
IC-CAD Labs.

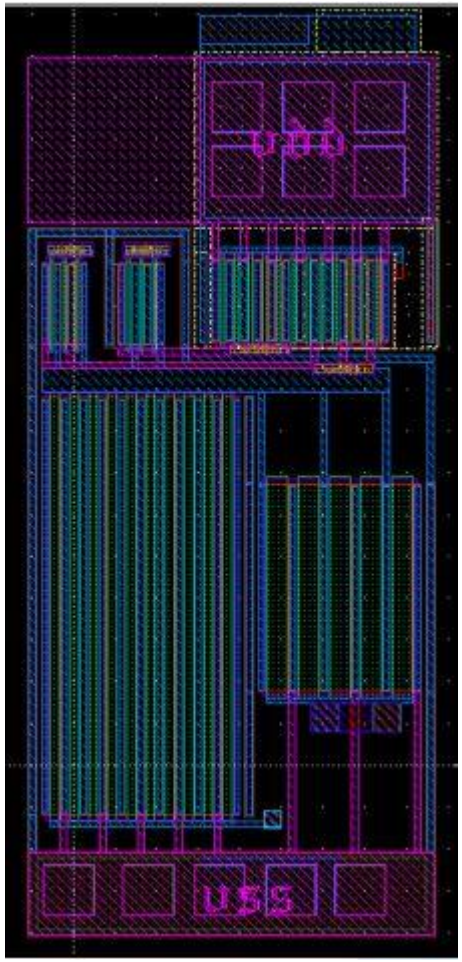
Analog Part

Lect. 3 Cadence Layout Editor

Analog Circuit Design

- **Basic Flow**





Cadence Schematic Editor

- **/office1/class/2022_1_ICCAD/2022_1_ICCADxx 폴더에서 다음 명령어를 입력합니다.**

  → source .chsrc

- **그 다음 Cadence Schematic Editor를 작업할 폴더로 이동합니다.**

  → cd /office1/class/2022_1_ICCAD/2022_1_ICCADxx/PDK/FreePDK45/cds_ncsu

- **그 다음 해당 폴더에 있는 setup.csh를 import 합니다.**

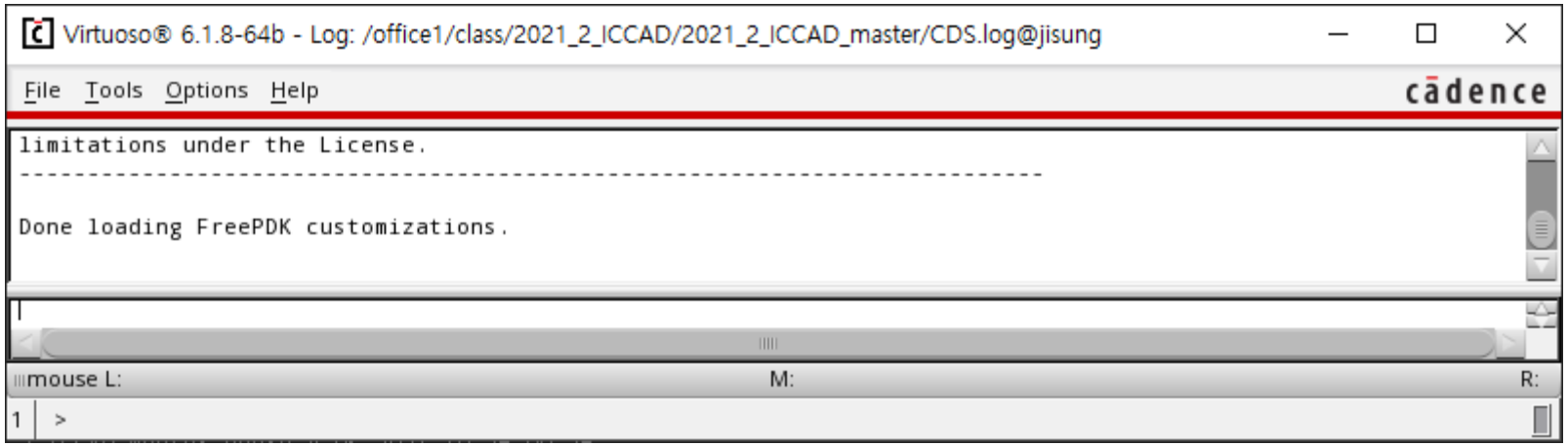
  → source setup.csh

- **virtuoso & 혹은 vir 를 커맨드창에 입력합니다.**

*위의 모든 과정이 커맨드 창에 iccad를 입력하면 진행되도록 셋업이 되어있습니다.

Cadence Schematic Editor

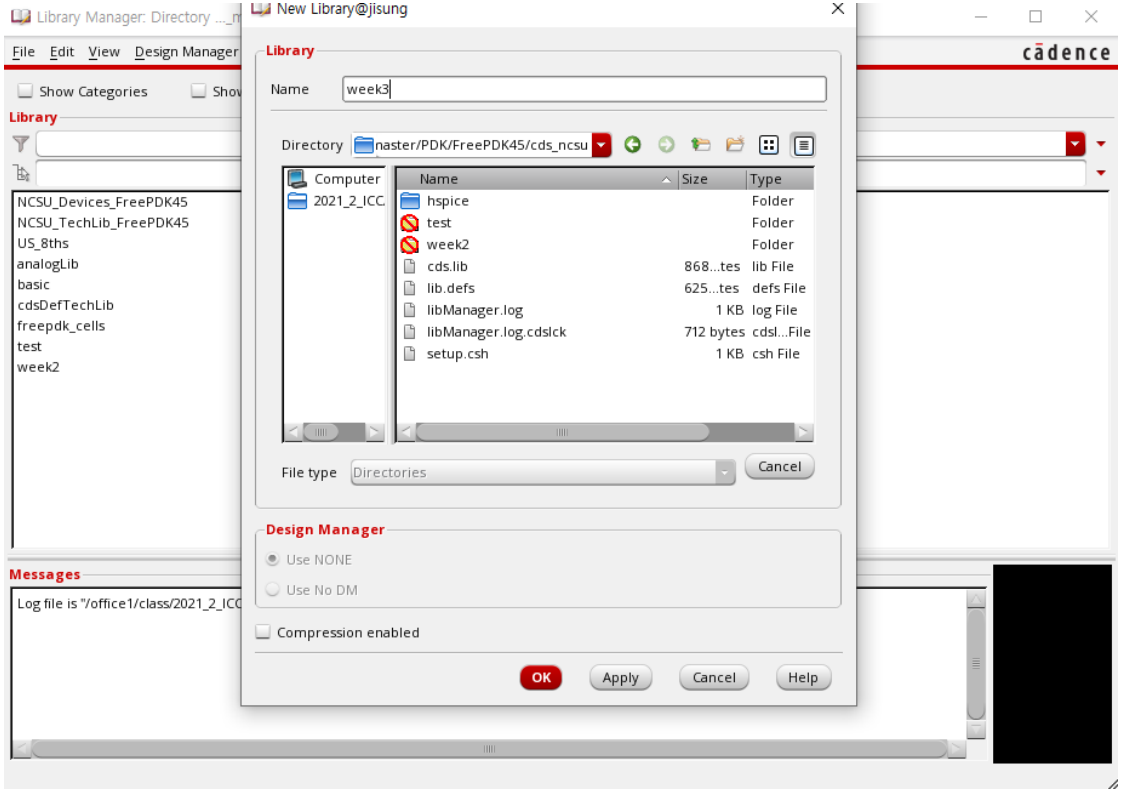
- **Tools → Library Manager**



위와 같은 창이 생성되는지 확인해보세요.

Cadence Schematic Editor

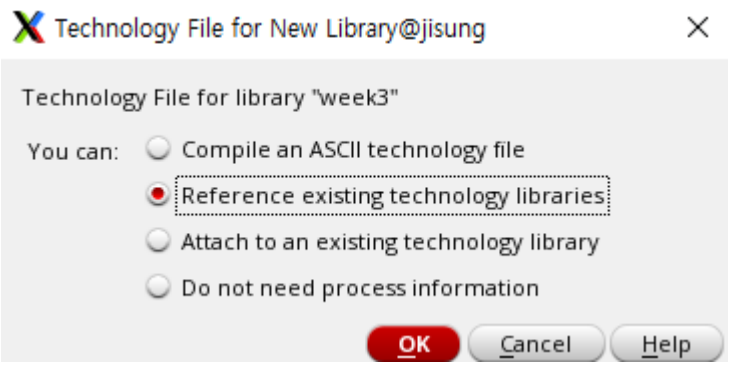
- **Library Manager → New → Library**

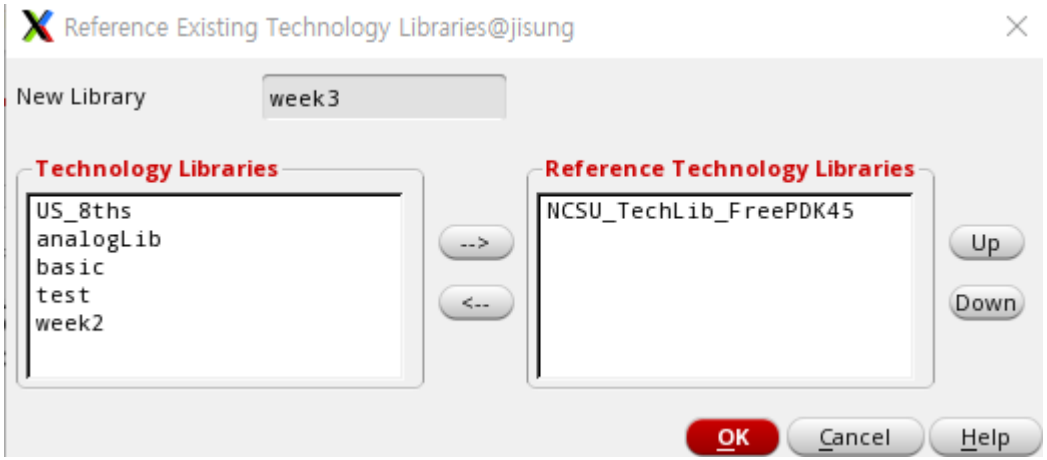


Name에는 week3 라고 씁니다

Cadence Schematic Editor

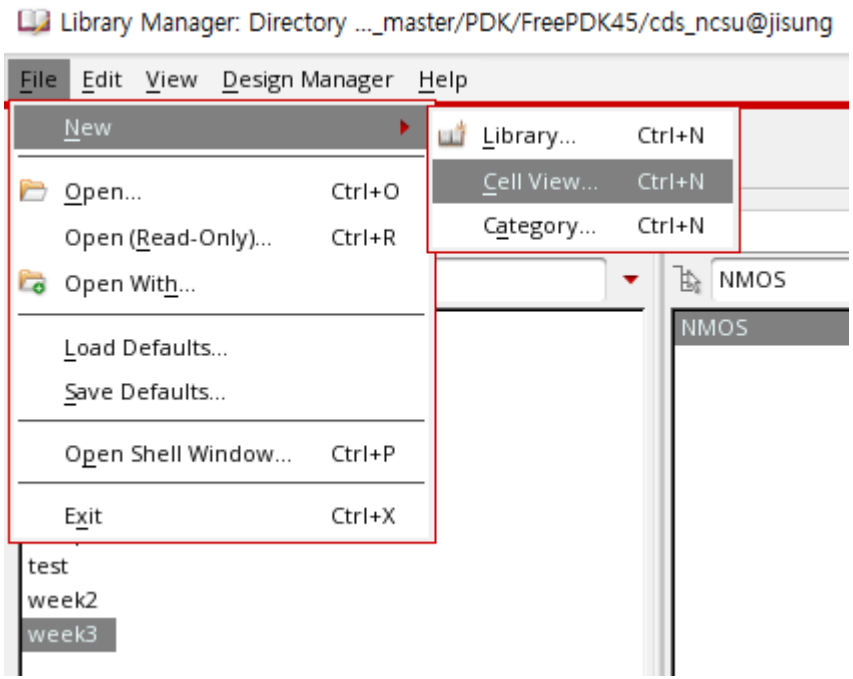
- **Technology File 불러오기 → MOSFET의 Model이 정의되어 있는 파일**



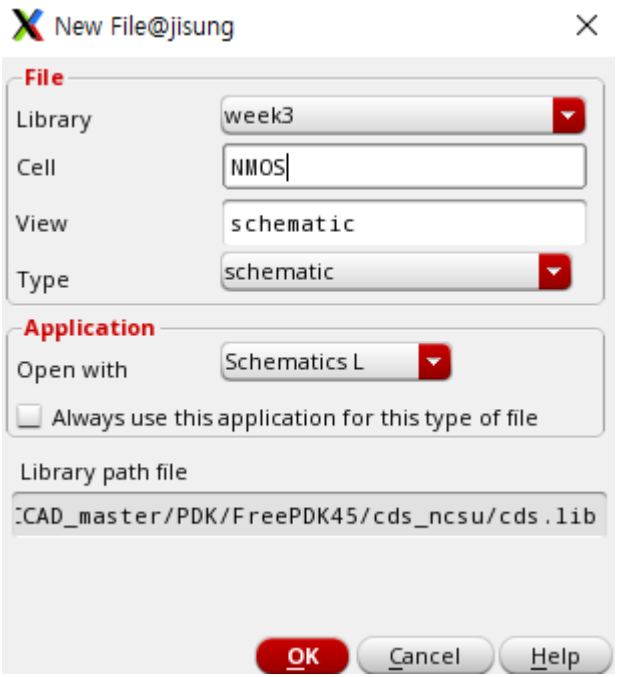


Cadence Layout Editor

- **Library manager File → New → Cell View**

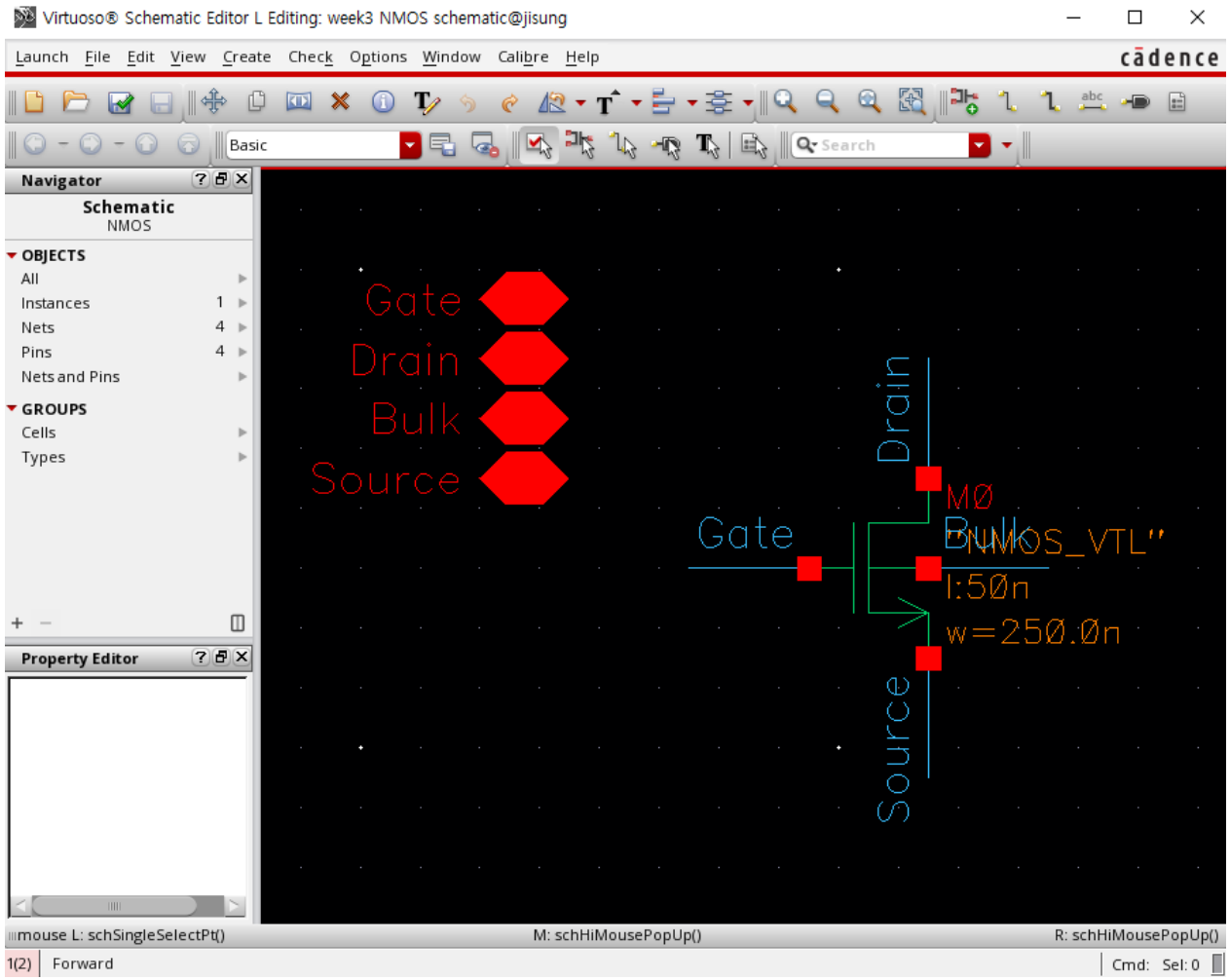


- ✓ **Library Name → week3**
- ✓ **Cell Name → NMOS**
- ✓ **Tool → Composer-Schematic**



Cadence Layout Editor

- **Schematic 그리기**

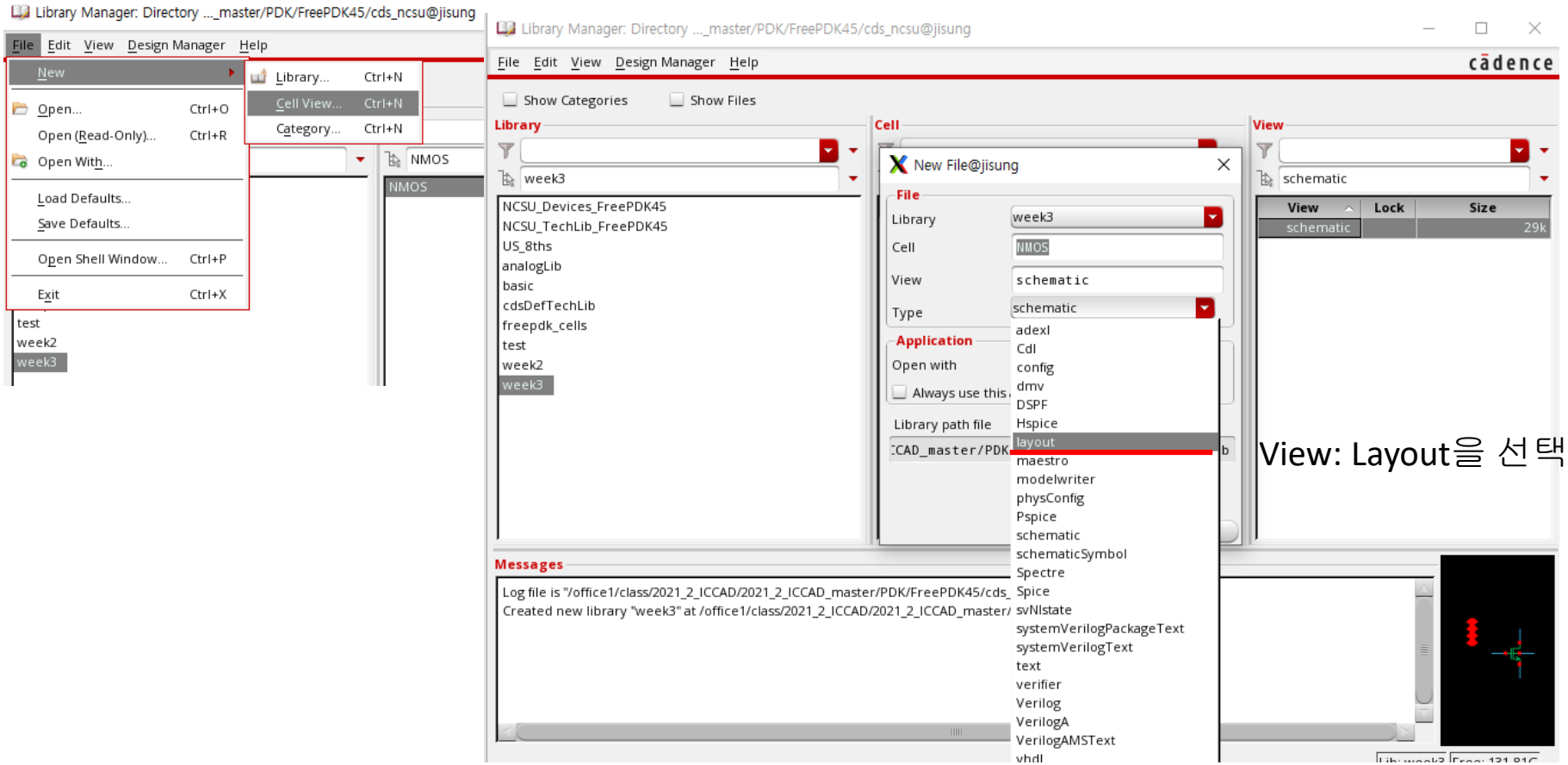


TR:NMOS_VTL
Width: 0.25um
Length: 0.05um

Cadence Layout Editor

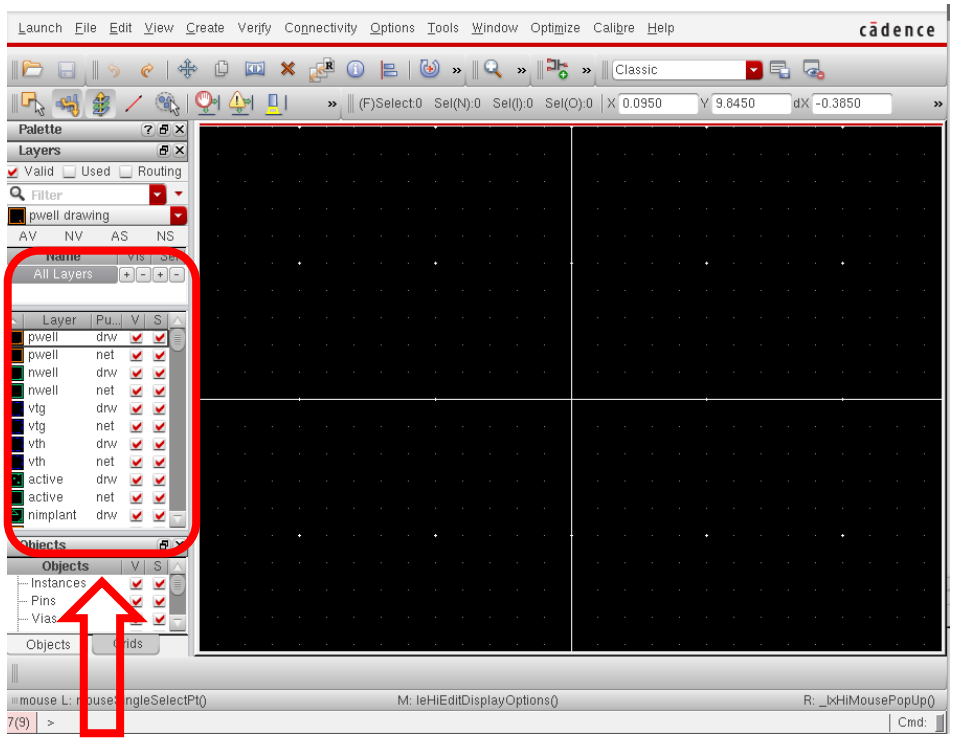
- **Library manager File → New → Cell View**

✓ **Library Name → week3**
✓ **Cell Name → NMOS**
✓ **Tool → Virtuoso**



Cadence Layout Editor

- **Layout Editor Basics**



Layout Select Window (LSW)

<Shortcut>

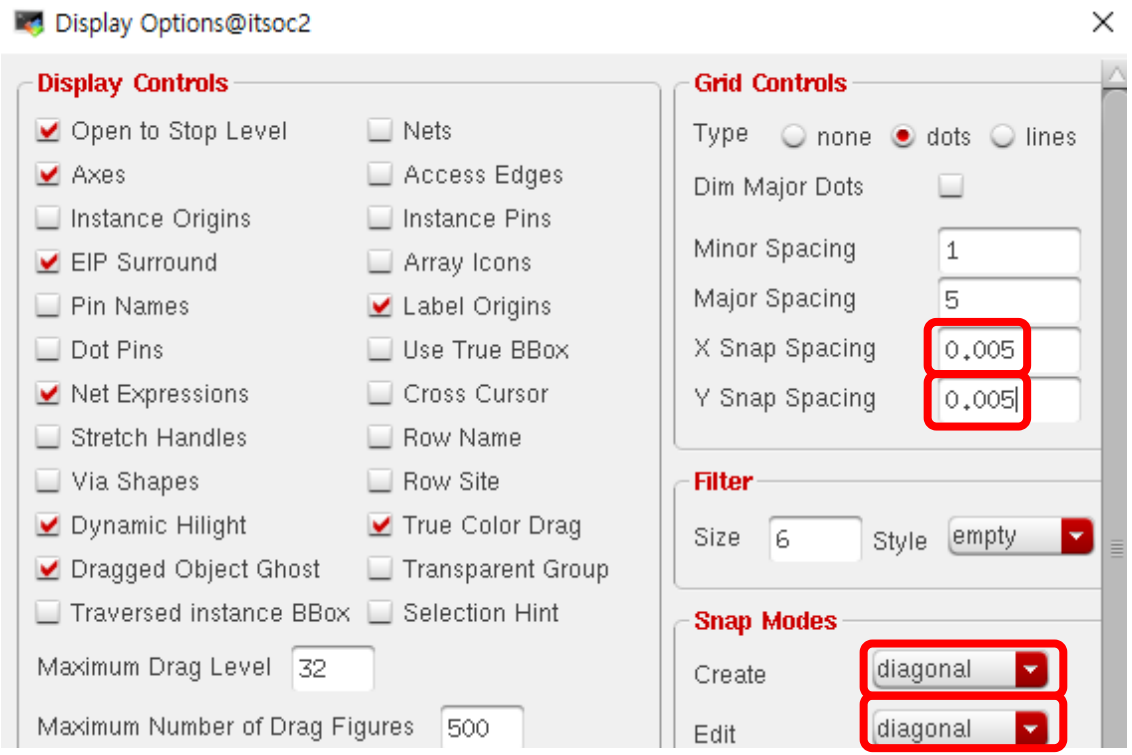
E	: Display option
I	: Instance 불러오기
C	: Copy
M	: Move
Shift + M	: Merge
Ctrl + D	: Deselect
Q	: Instance의 상태 확인
F	: 화면 크기 자동 조정
R	: 사각형 그리기
S	: Layer 늘이기
K	: Ruler 생성
Shift + K	: 모든 Ruler 없애기
Del	: 삭제

<알아두면 좋은 점!>

Layout Editor를 사용할 때엔 드래그 보다는 클릭 투 클릭을 사용하는 것이 좋습니다.

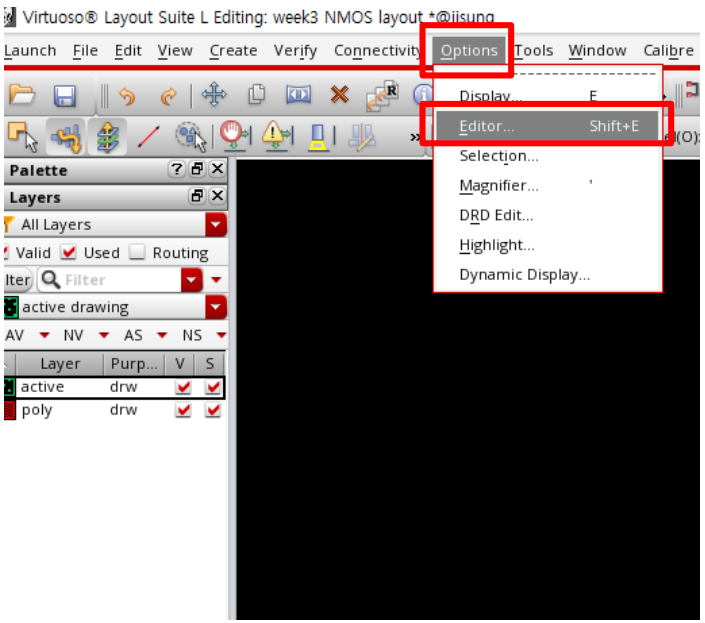
Cadence Layout Editor

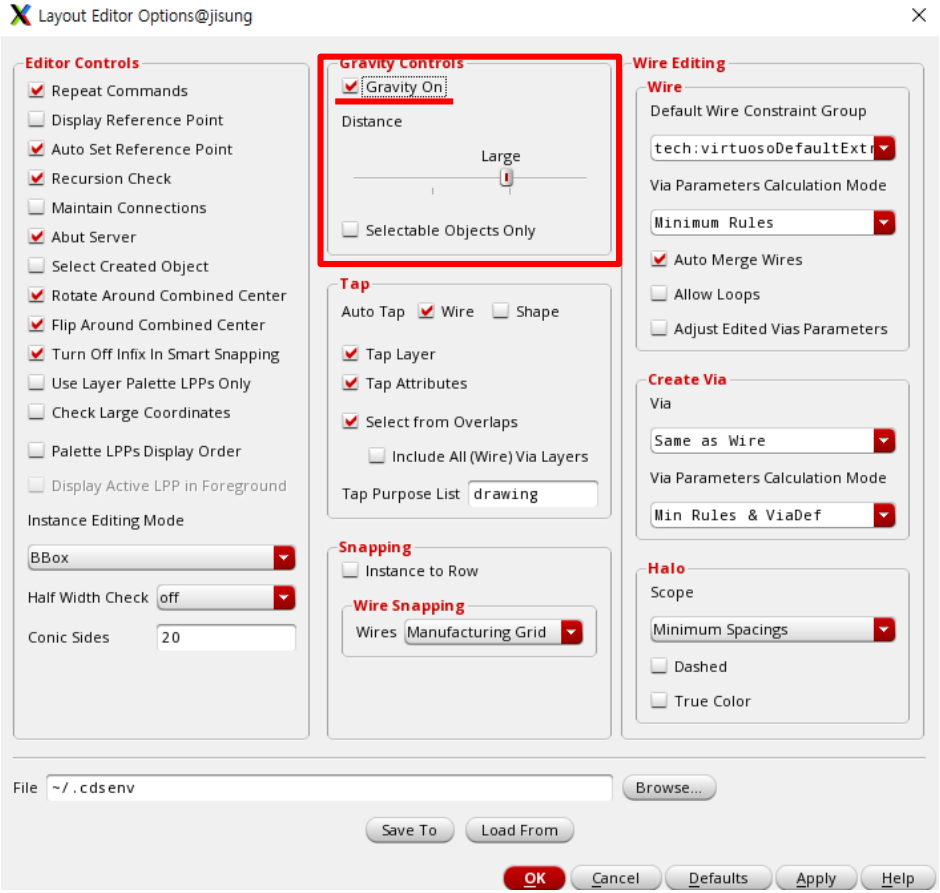
- E → Display Options
  - ✓ Grid Controls : X snap Spacing : 0.005, Y snap Spacing : 0.005
  - ✓ Snap Modes : Create : diagonal, Edit : diagonal



Cadence Layout Editor

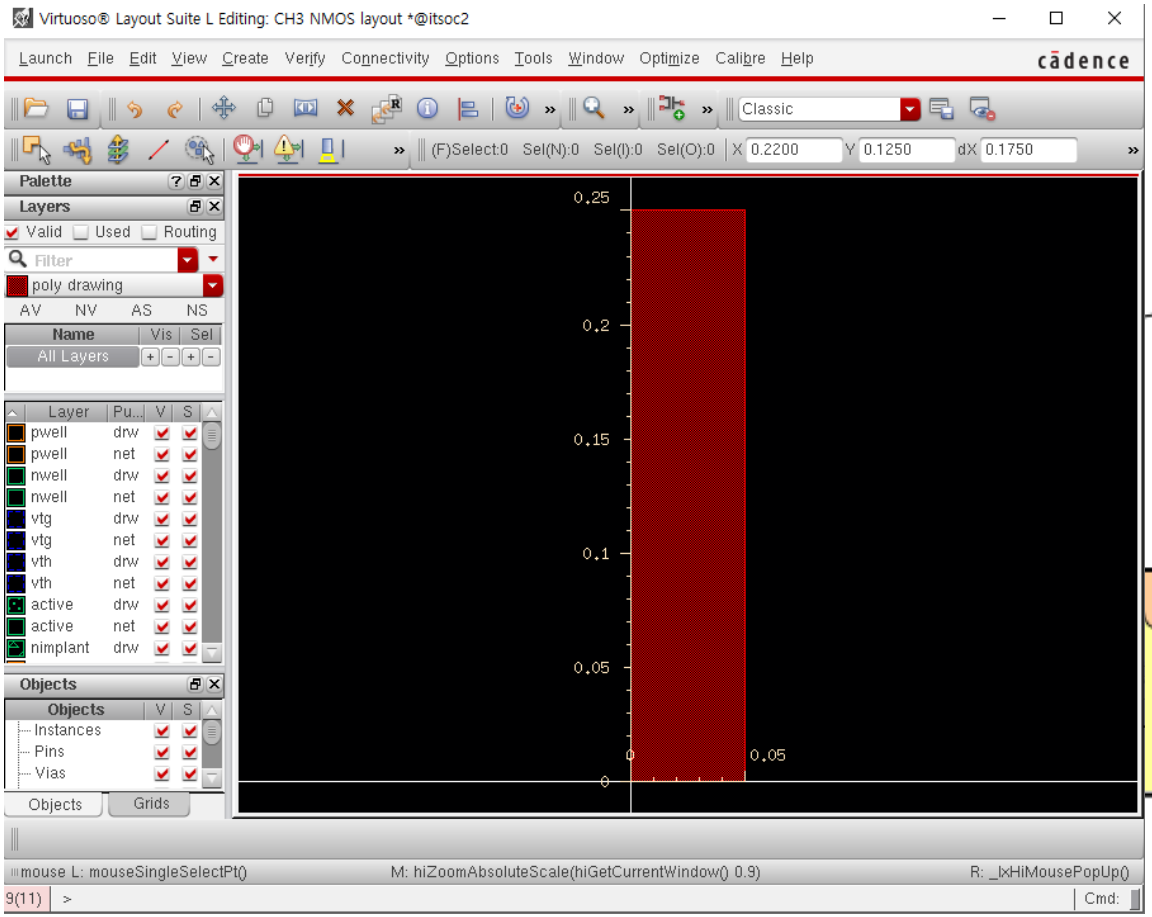
- **Options → Editor**
  - ✓ **Gravity Controls: Gravity On, Distance Large**

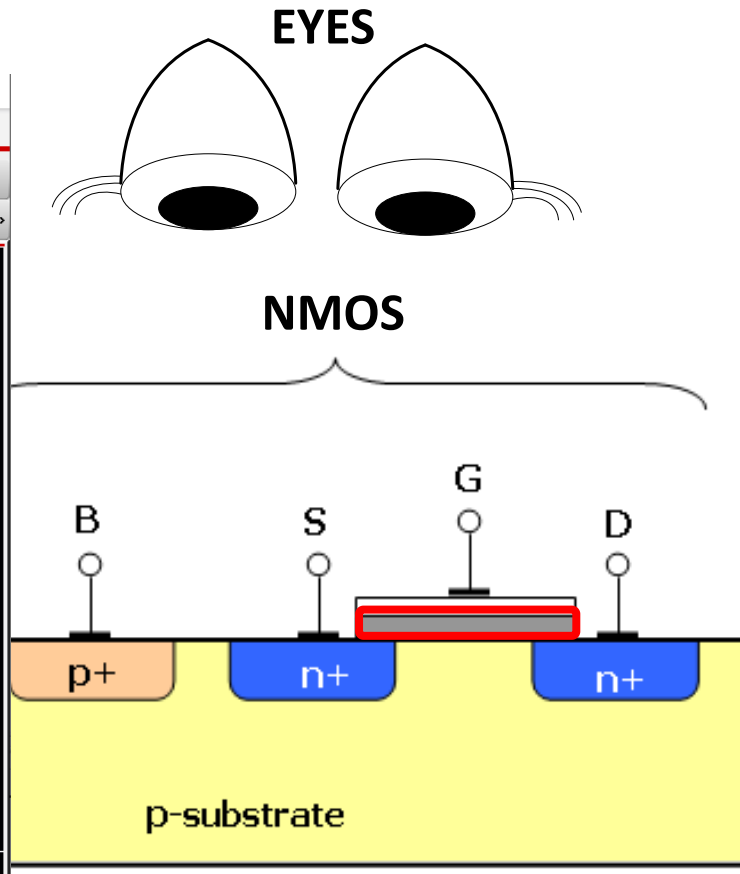




Cadence Layout Editor

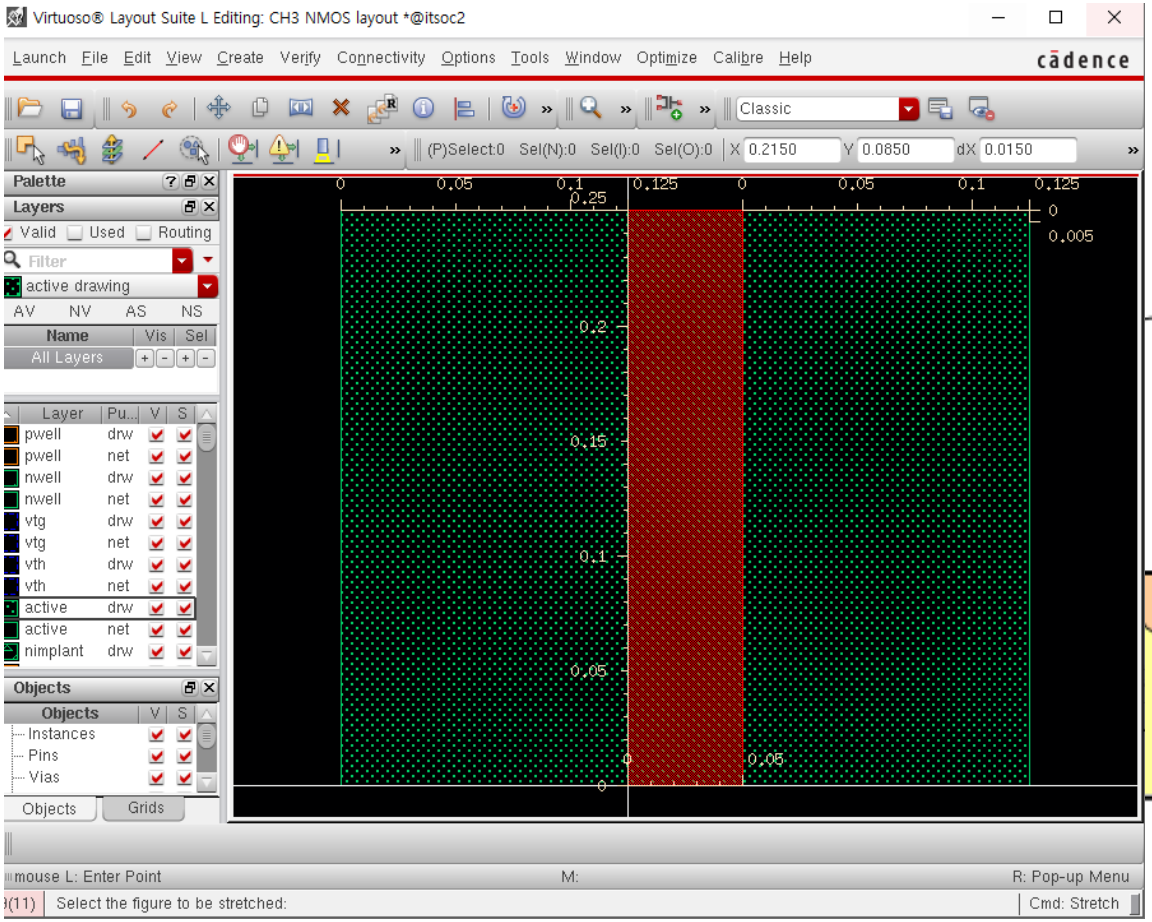
- **Gate-Poly 생성 (0.05 * 0.25)**

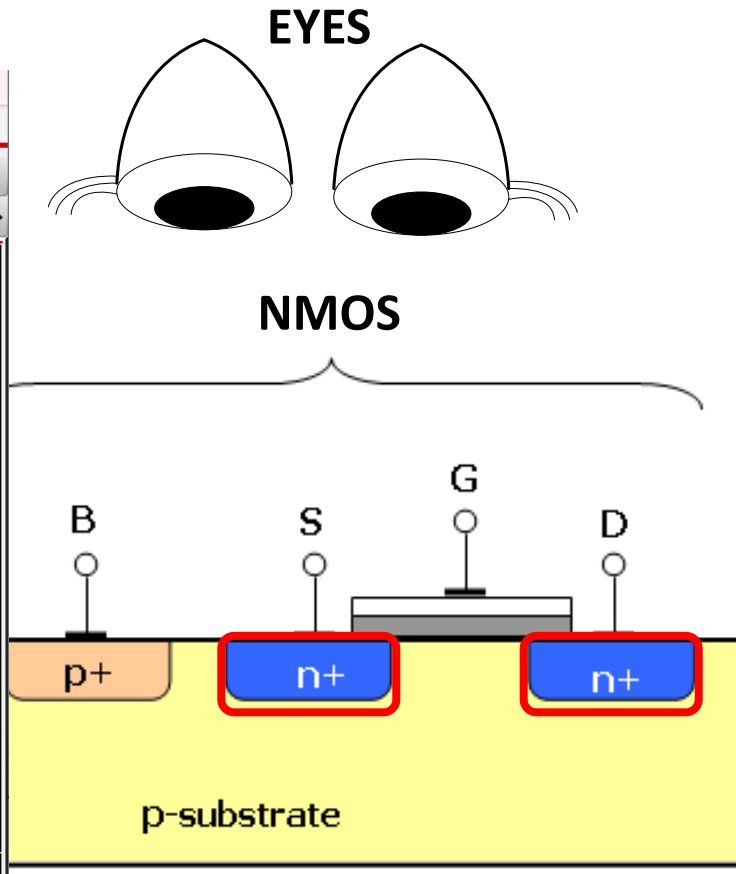




Cadence Layout Editor

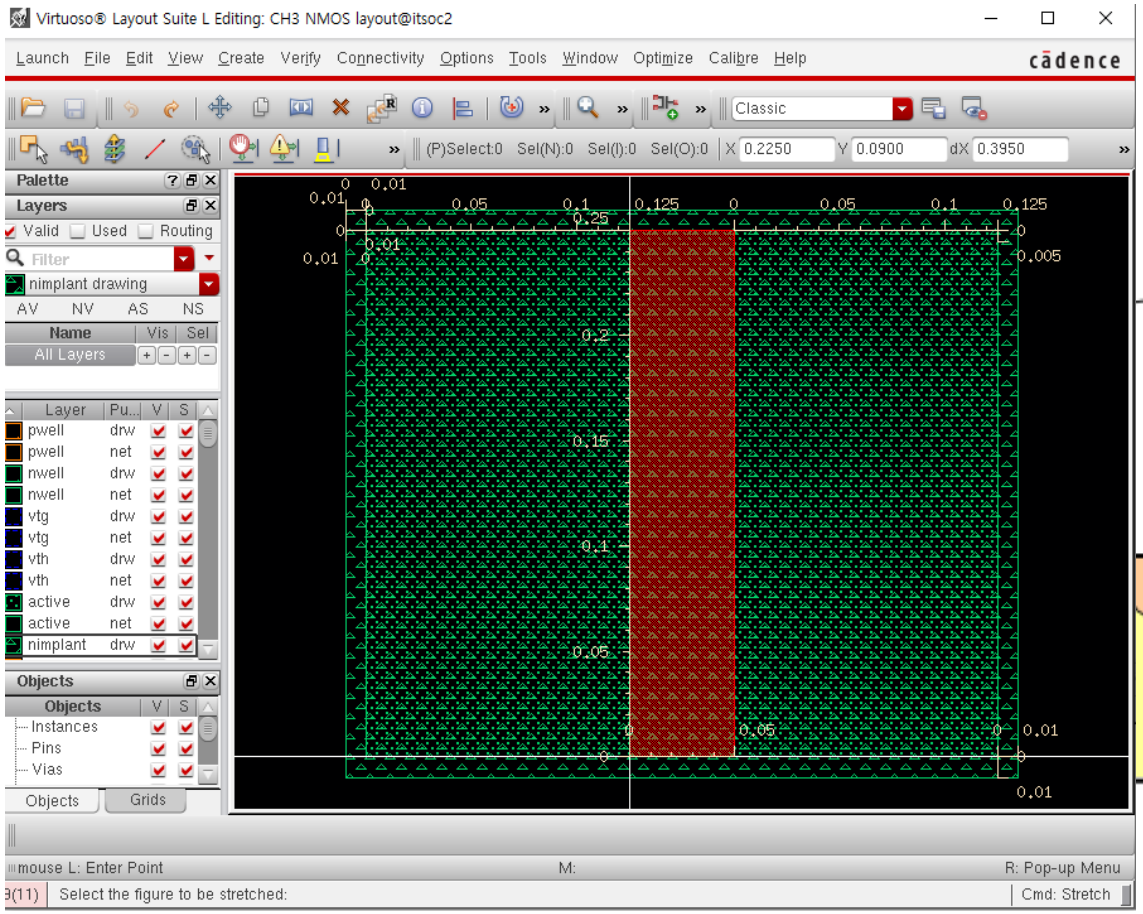
- **Active 생성 (0.3 * 0.25)**

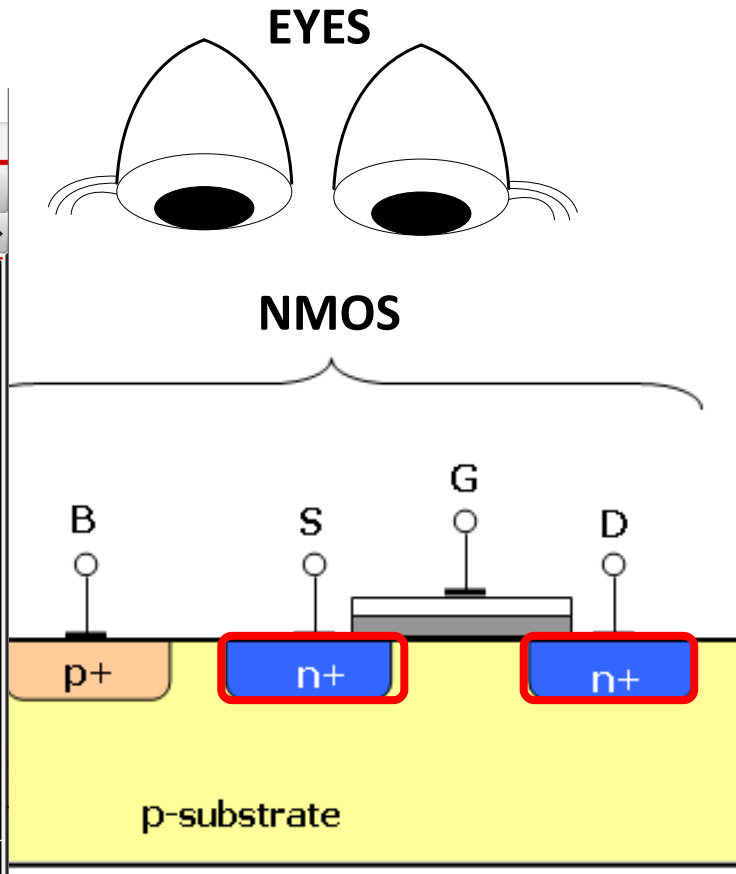




Cadence Layout Editor

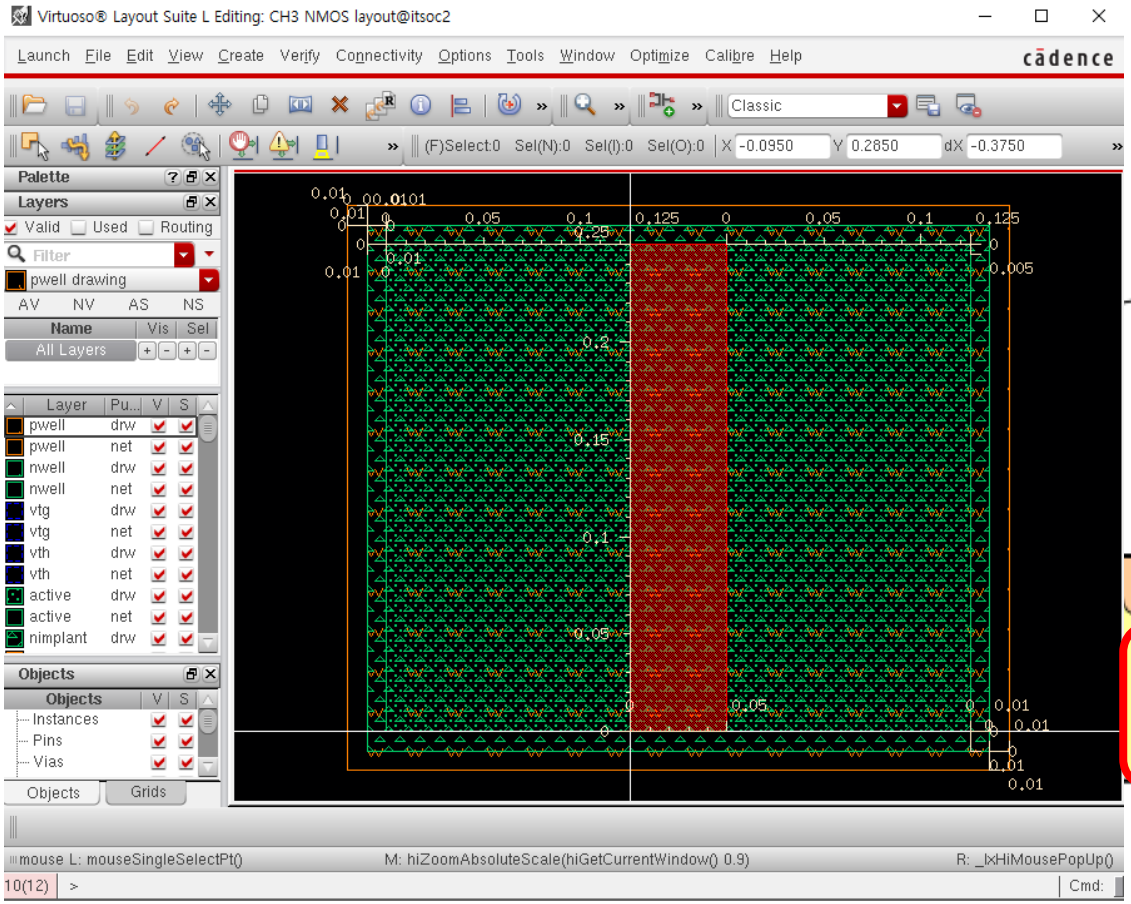
- **Nimplant 생성 (0.32 * 0.27)**

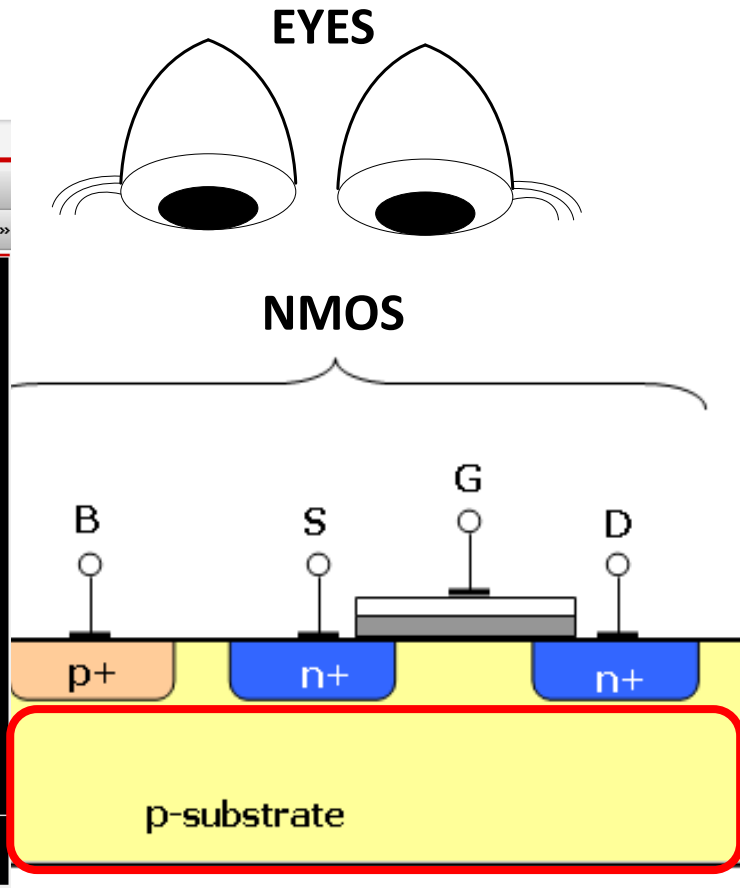




Cadence Layout Editor

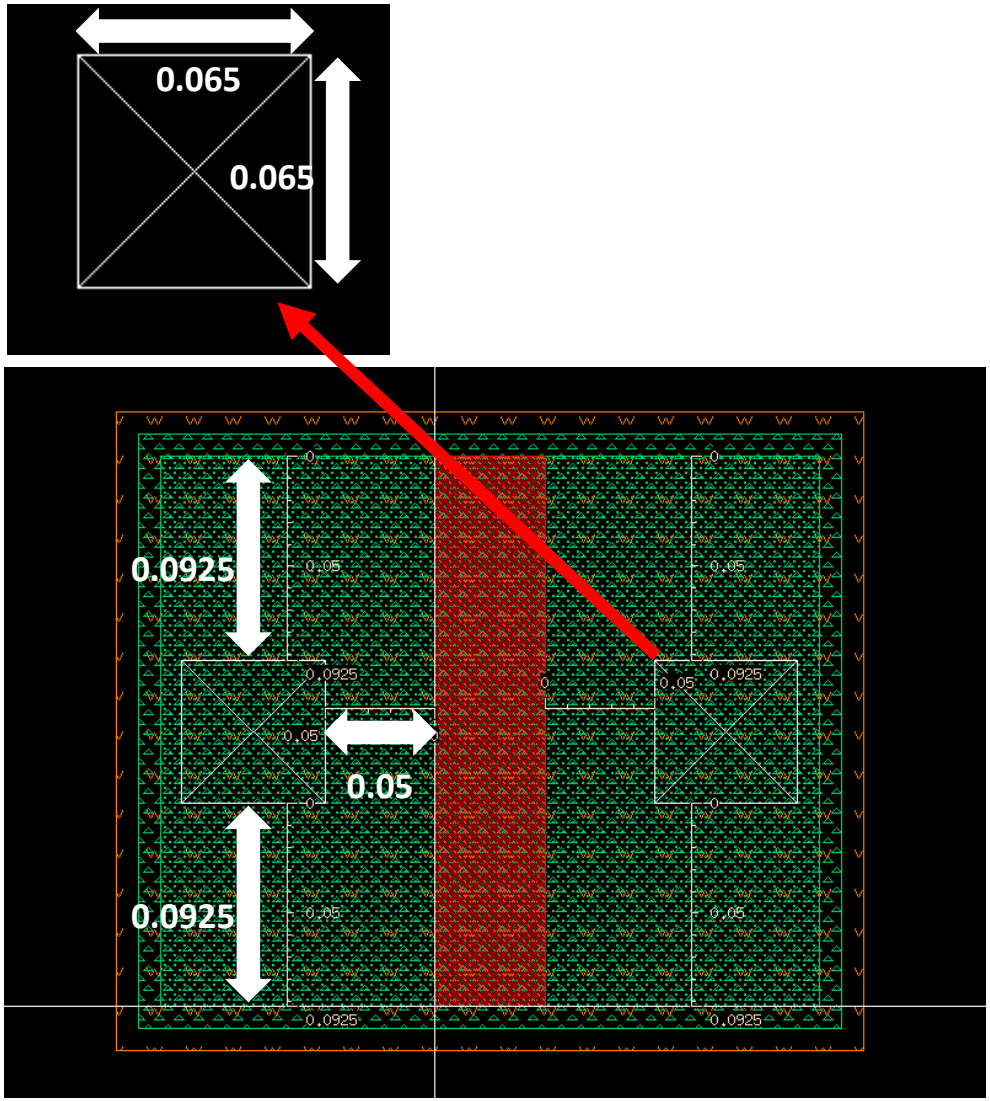
- **P-Well 생성 (0.34 * 0.29)**

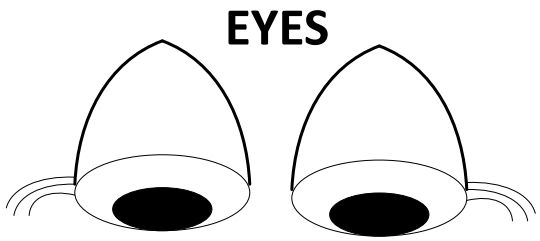


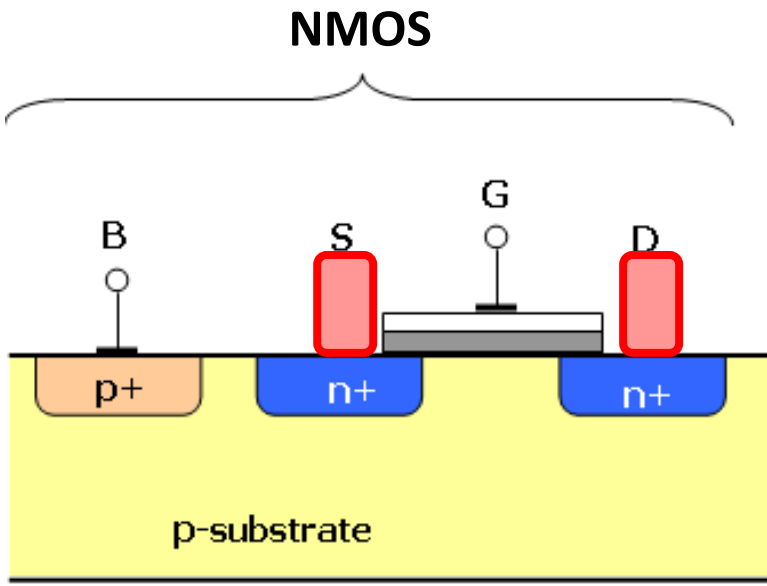


Cadence Layout Editor

- Contact 생성 (0.065 * 0.065)

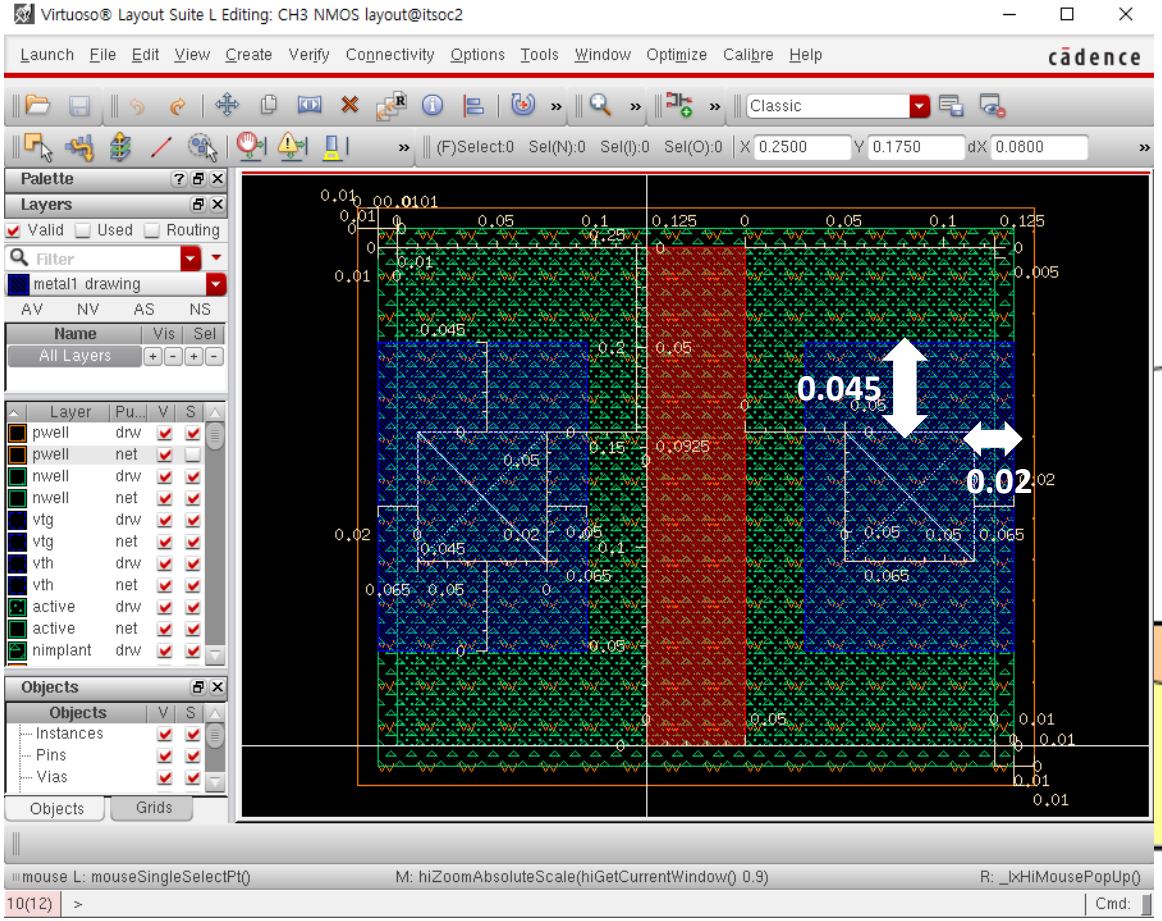


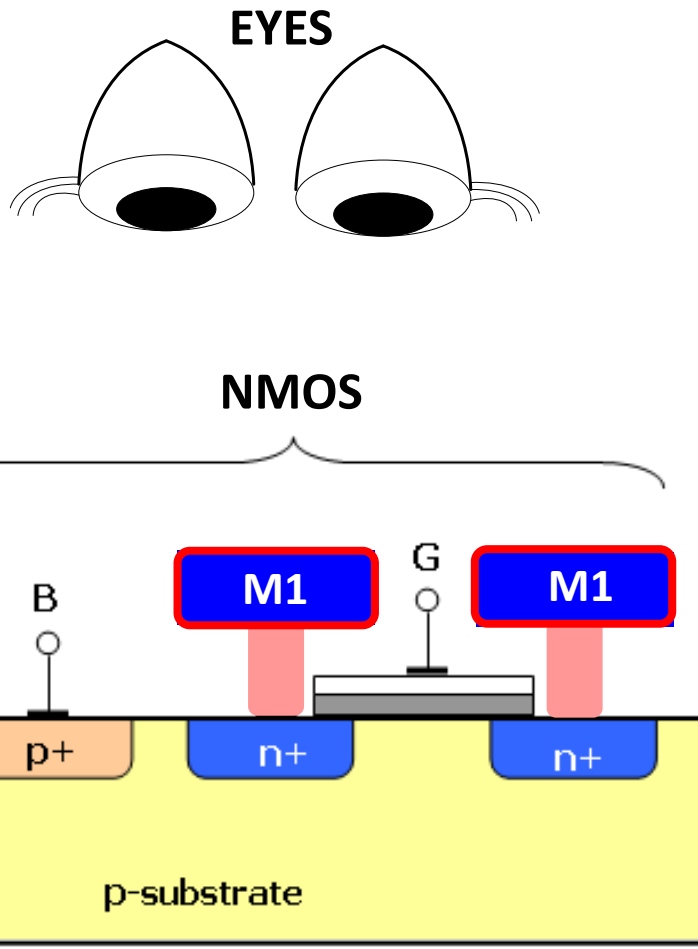




Cadence Layout Editor

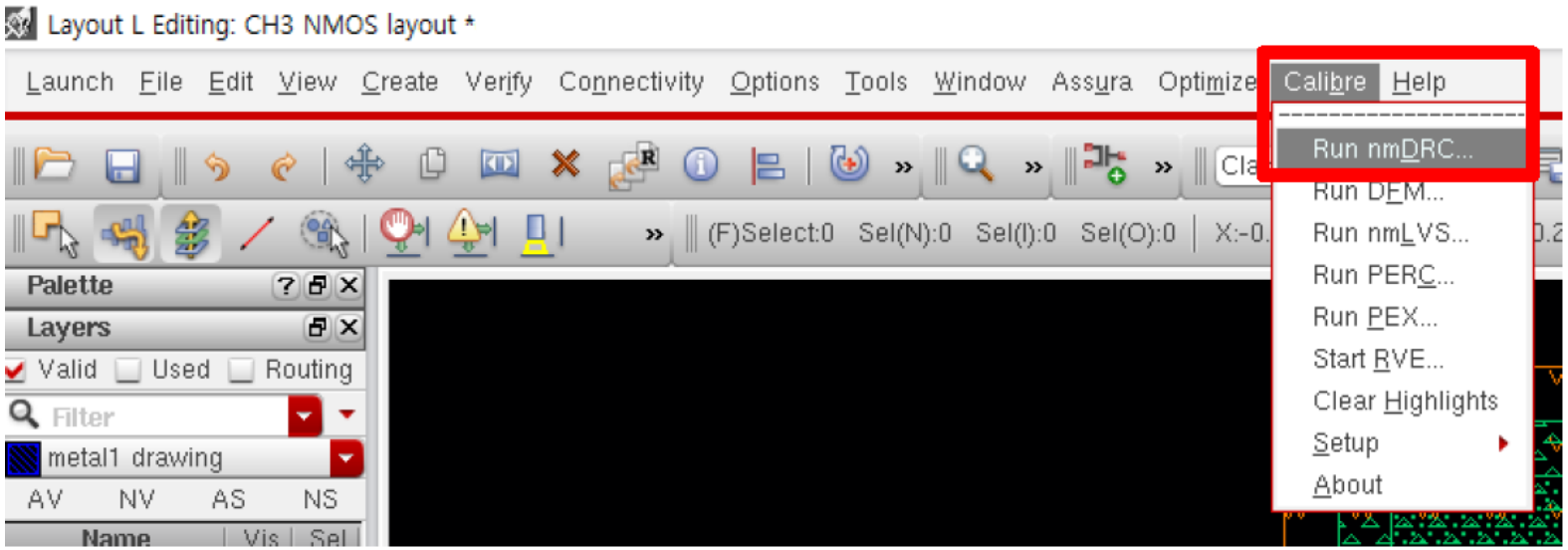
- **Metal1 생성**





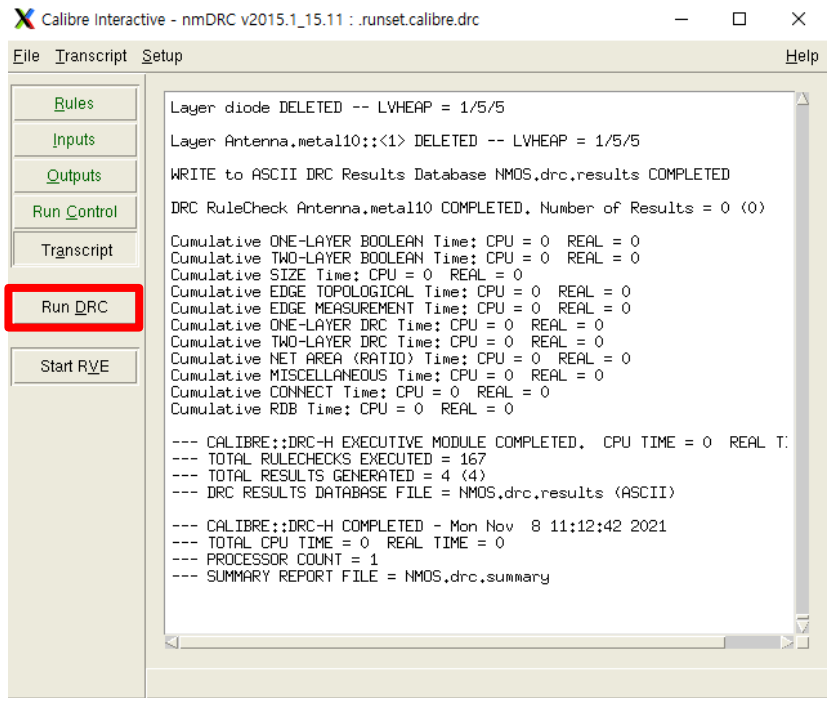
Cadence Layout Editor

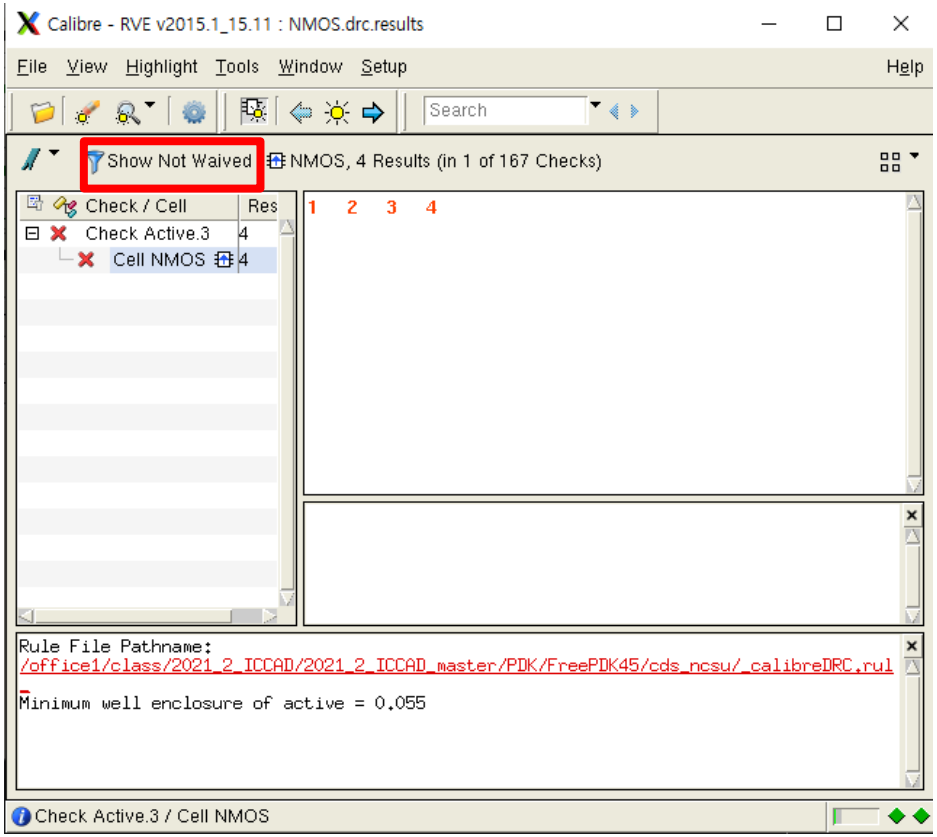
- **Design Rule Check (DRC)**
  - ✓ **Calibre → Run nmDRC**



Cadence Layout Editor

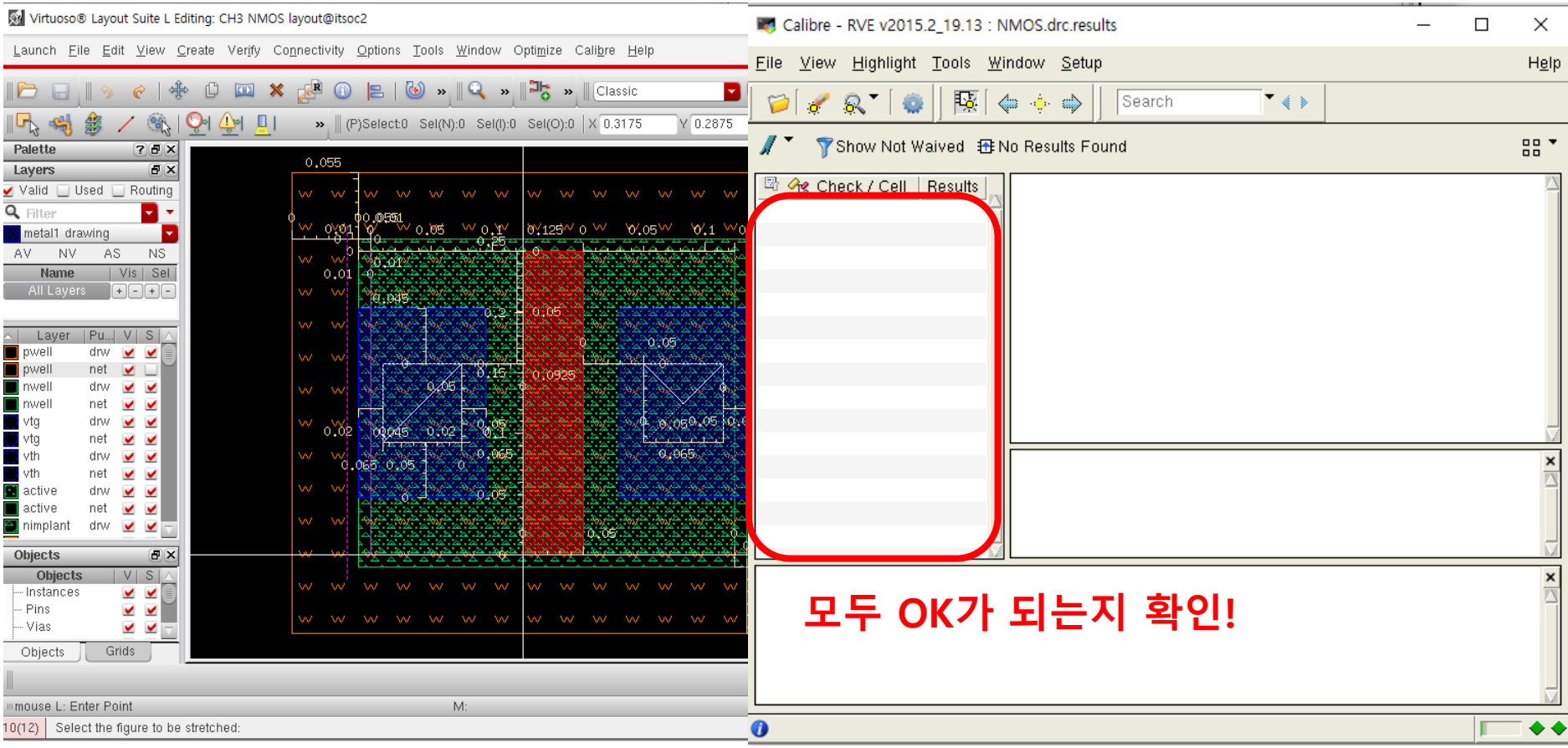
- **Design Rule Check (DRC)**
  - ✓ **Calibre → Run DRC**





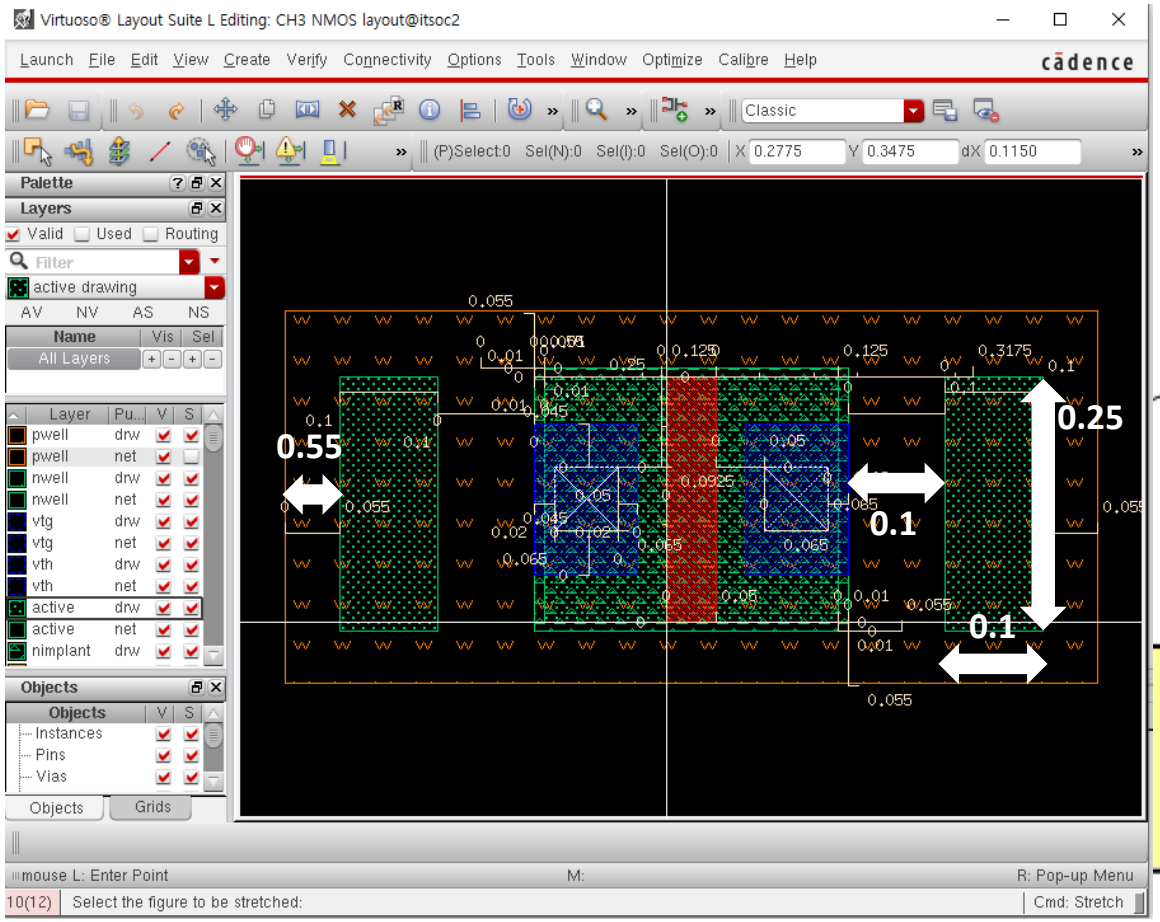
Cadence Layout Editor

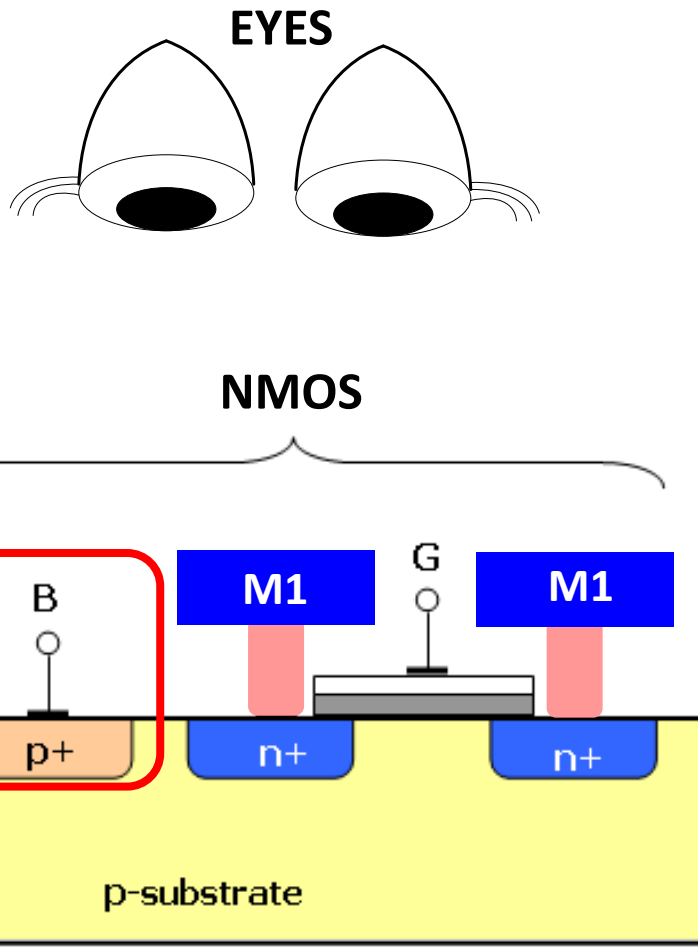
- **Layout을 고친 후 다시 DRC를 수행하자!**



Cadence Layout Editor

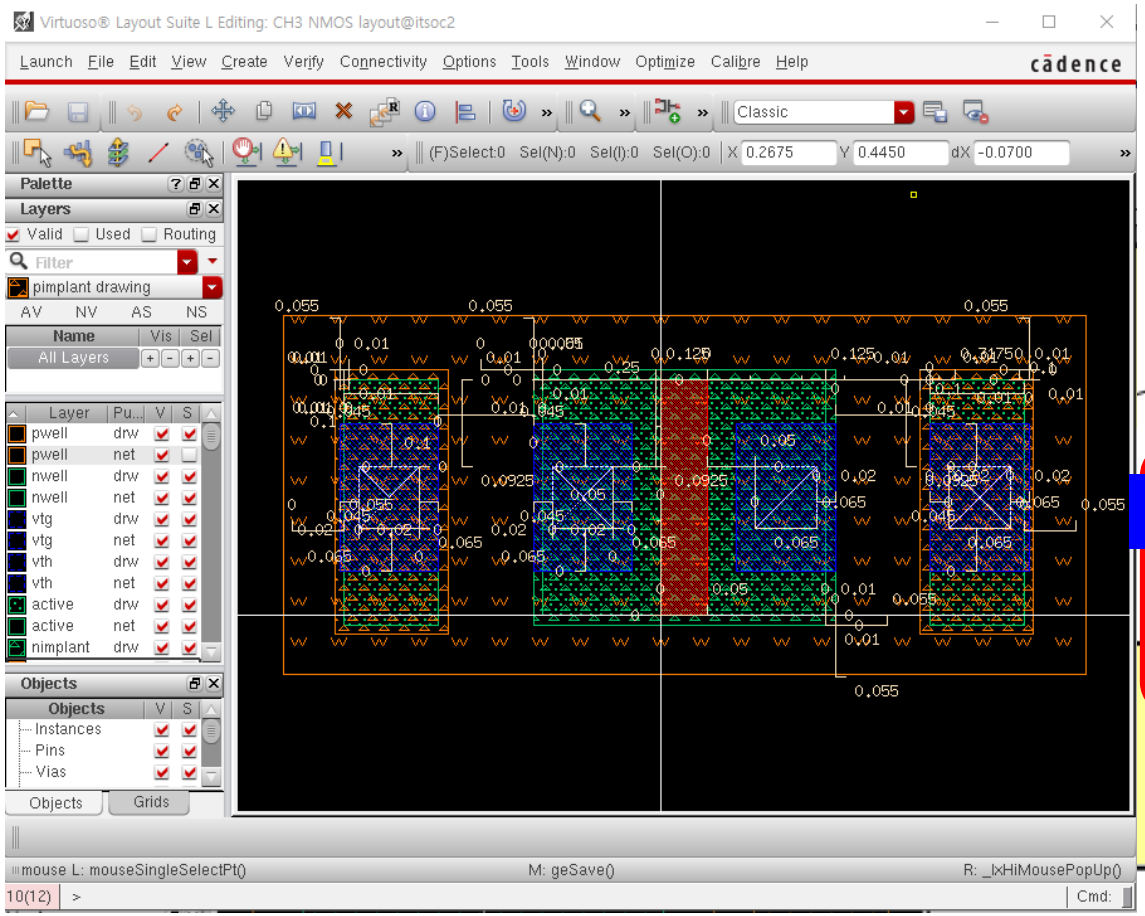
- **Bulk 생성 (Pimplant, contact, metal1)**

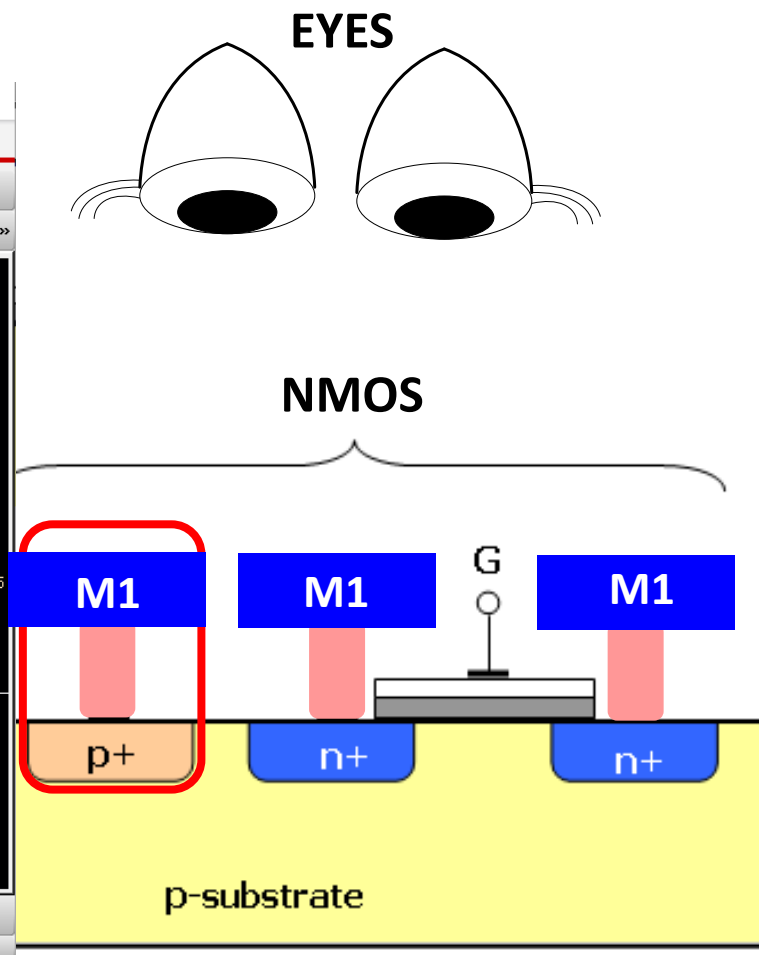




Cadence Layout Editor

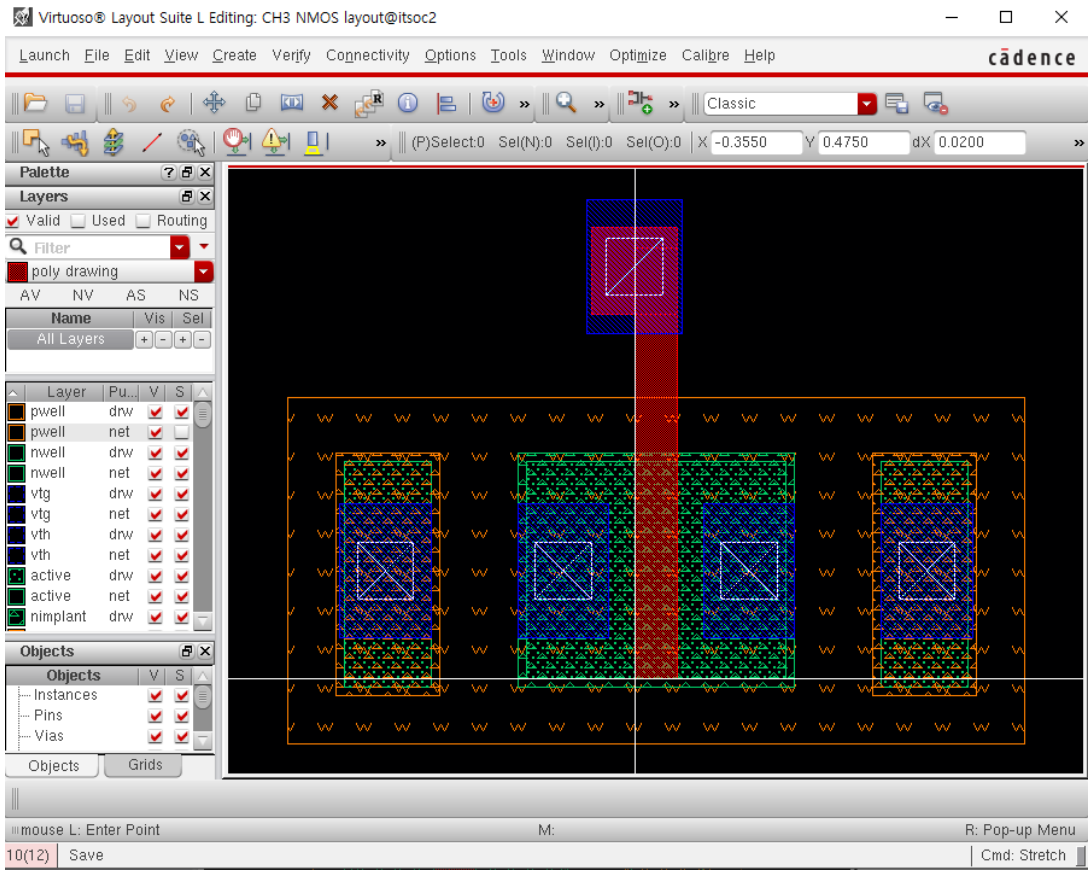
- **Bulk 생성 (Pimplant, contact, metal1)**

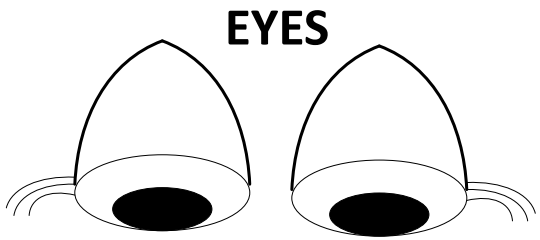


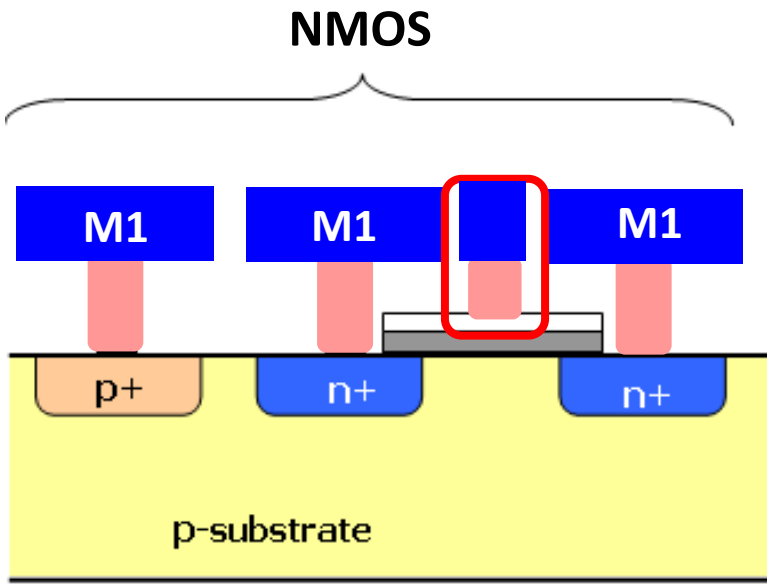


Cadence Layout Editor

- **Gate에 Metal 연결**

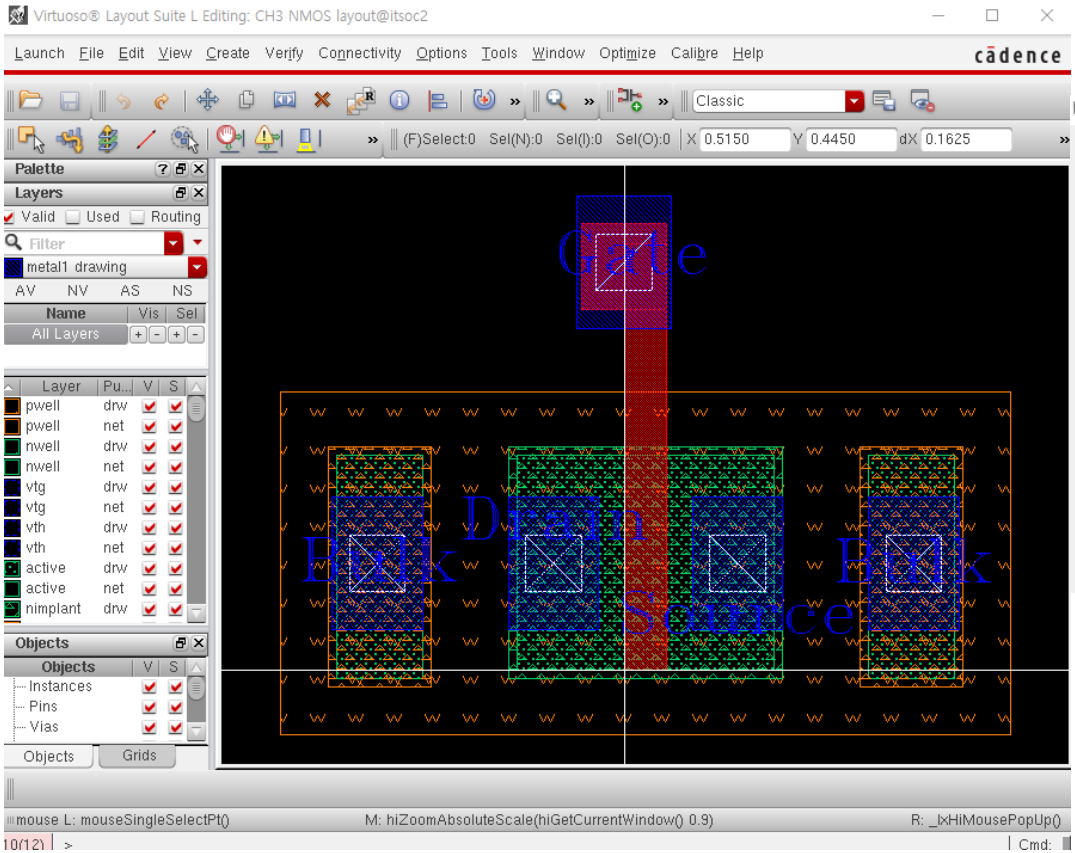




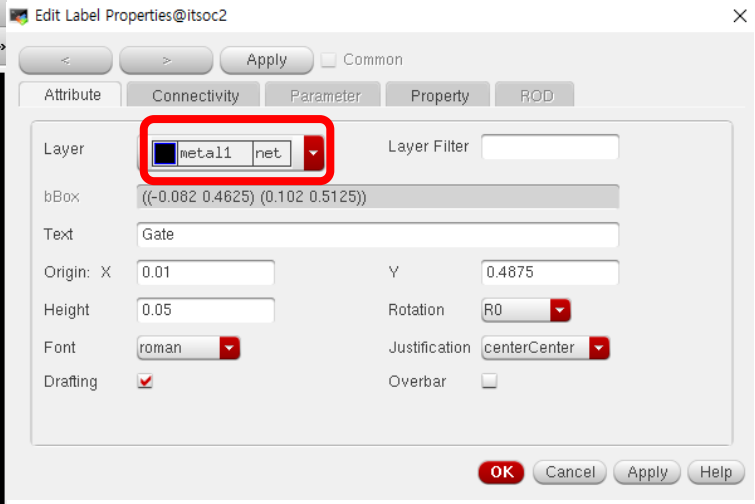


Cadence Layout Editor

- **Label 붙이기**
  - ✓ **Create → Label**

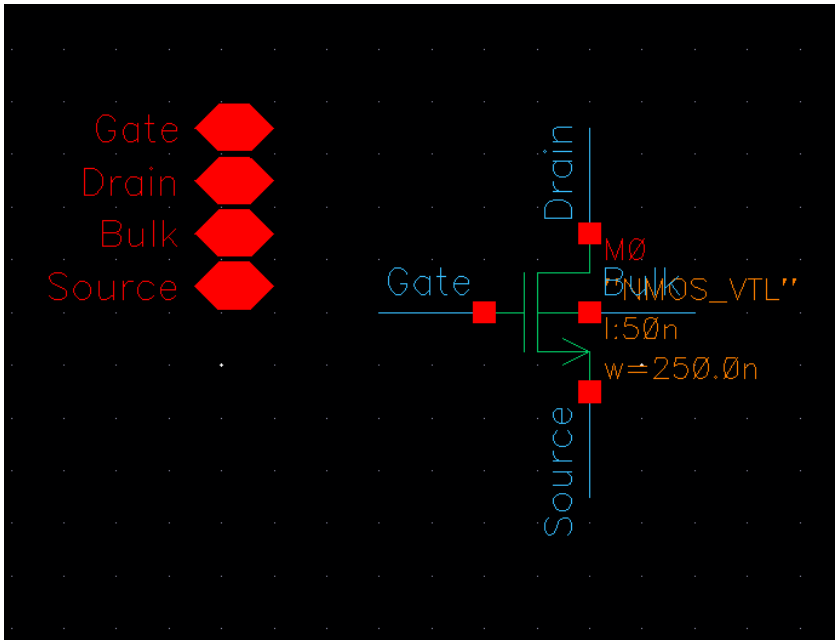


이 때, Layer는 반드시 NET으로 선택



Cadence Layout Editor

- **Layout vs Schematic (LVS) 수행**



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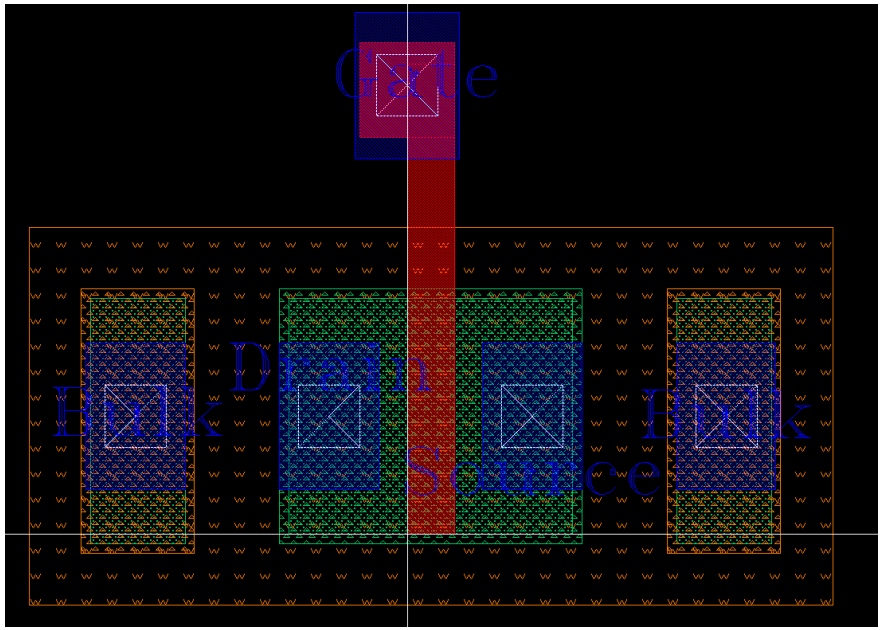
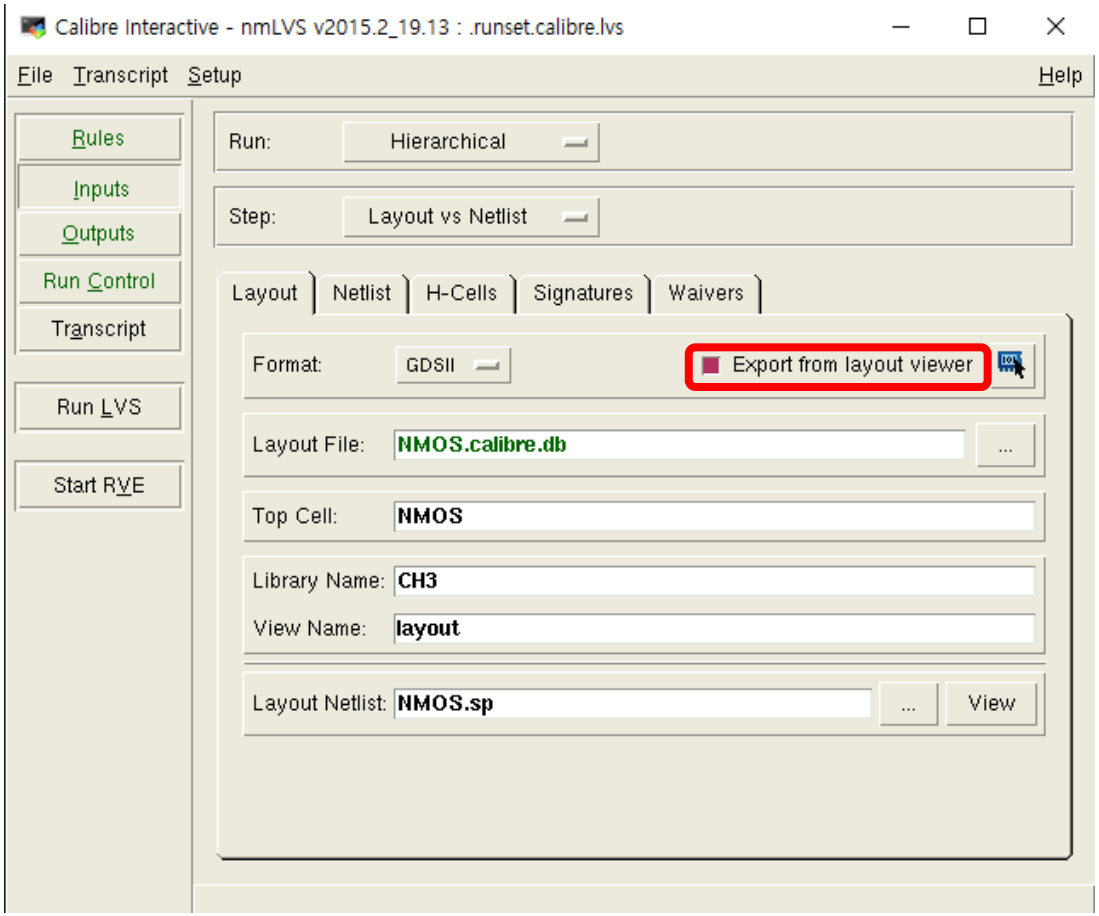


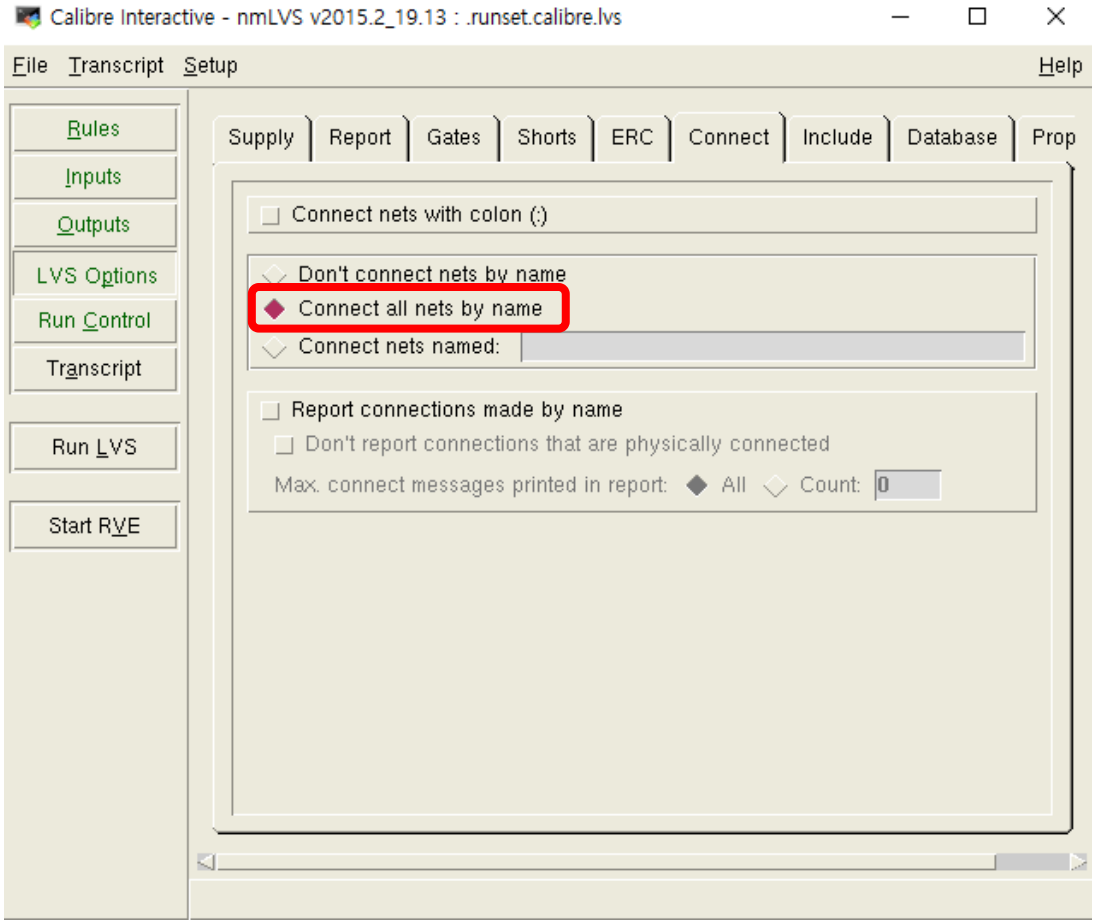
Cadence Layout Editor

- **Layout vs Schematic (LVS) 수행**
  - ✓ **Calibre → Run LVS**



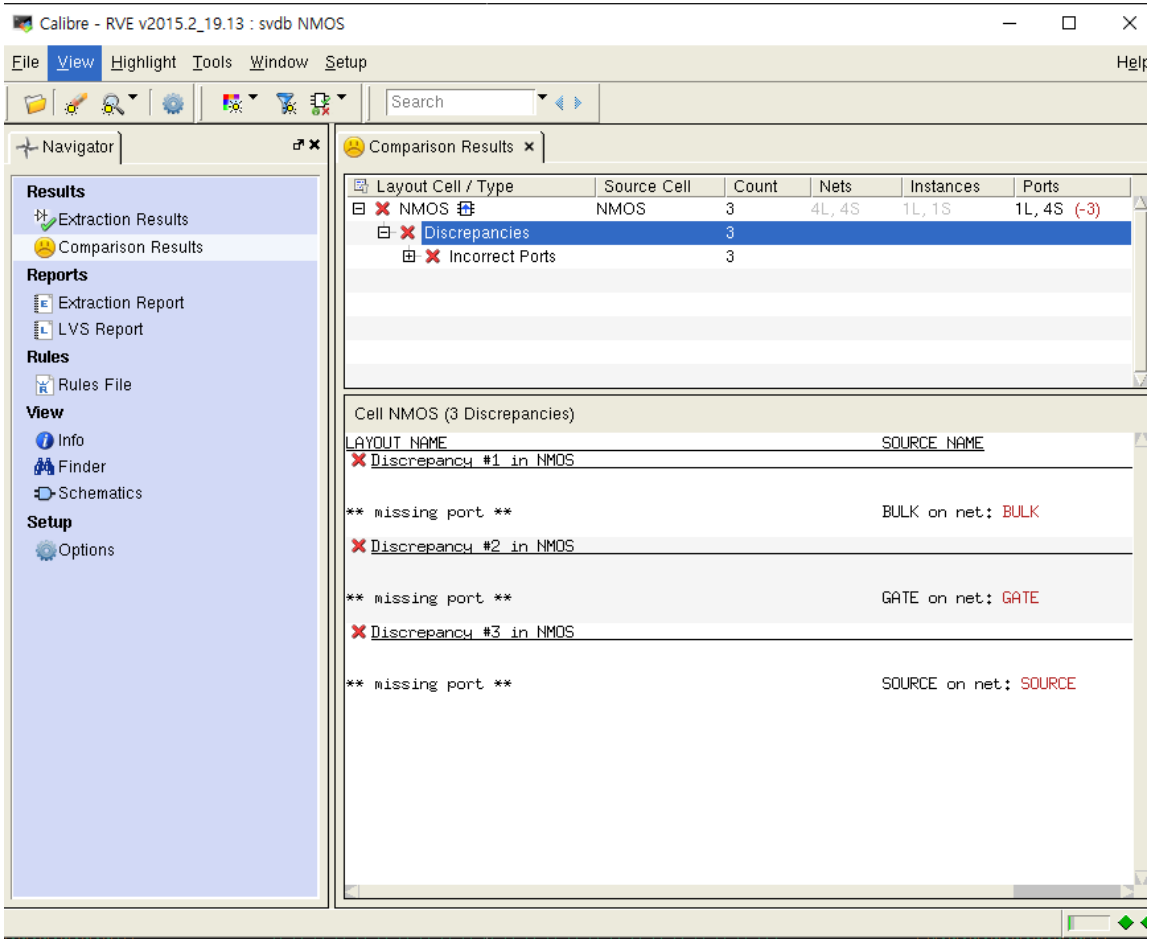
Cadence Layout Editor

- **Layout vs Schematic (LVS) 수행**
  - ✓ **Setup → LVS Options → Connect tap → Connect all nets by name**



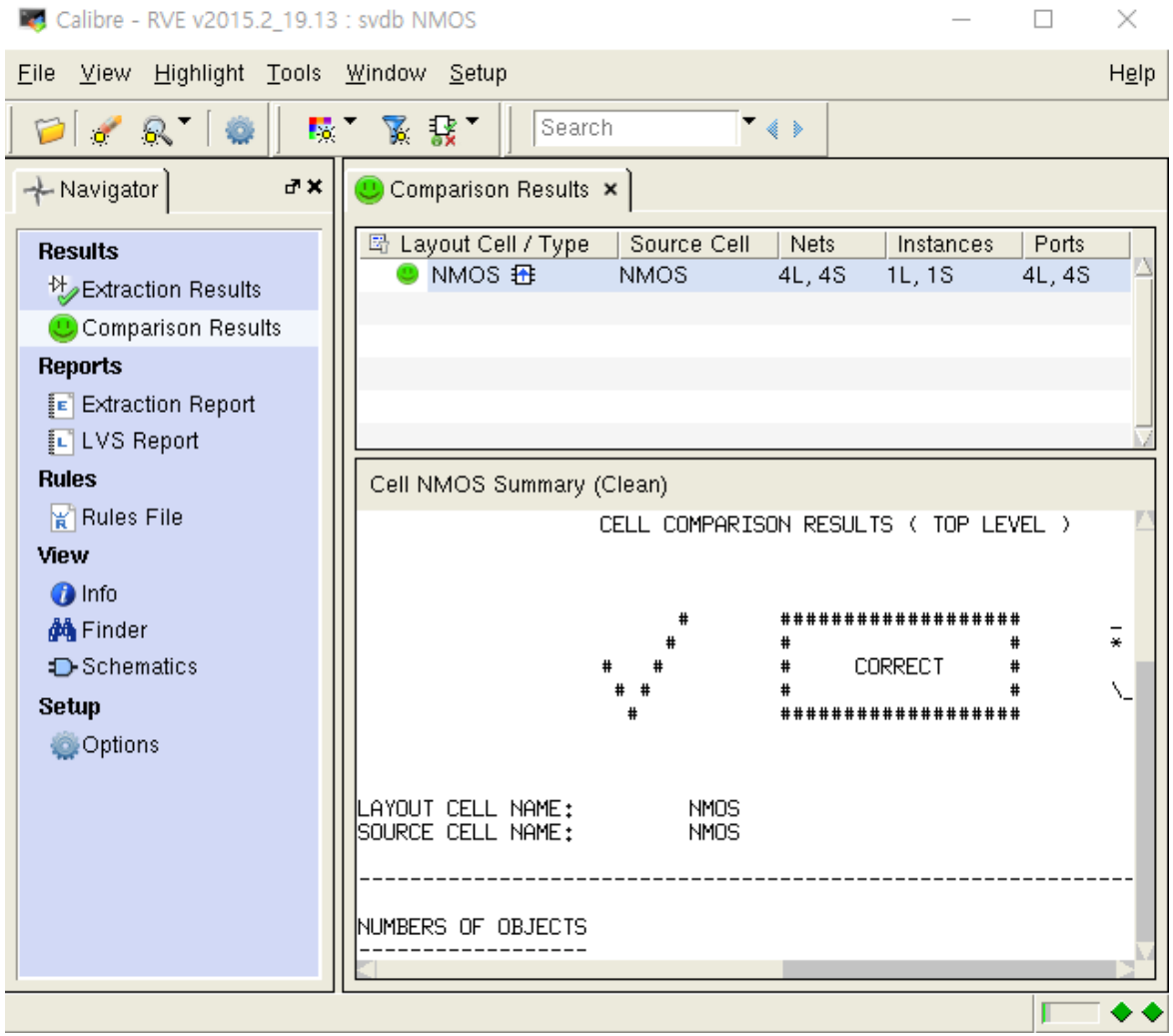
Cadence Layout Editor

- **Layout vs Schematic (LVS) 수행**



Cadence Layout Editor

- **Layout vs Schematic (LVS) 수행**



Homework

- **PMOS/NMOS layout & DRC & LVS**

✓ PMOS W=5u, L=0.3u
✓ NMOS W=2u, L=0.5u

	NMOS	PMOS
Well	PWELL	NWELL
Implant (Transistor)	Nimplant	Pimplant
Implant (Bulk Contact)	Pimplant	Nimplant

1) 레이아웃 캡쳐
2) DRC 에러없는 화면 캡쳐
3) LVS CORRECT 화면 캡쳐