Si Photonics

Lecture 9 : Si Waveguides

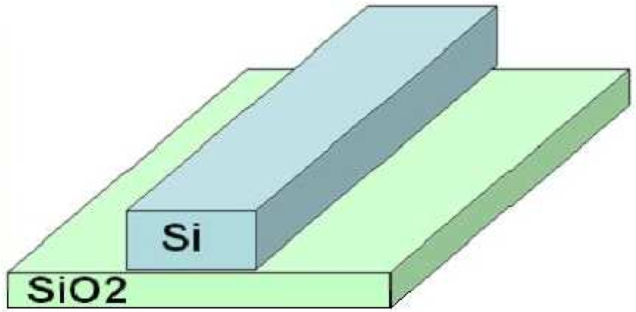
(Ref.: Silicon Photonics Design by Chrostowski and Hochberg)

Woo-Young Choi

Dept. of Electrical and Electronic Engineering
Yonsei University

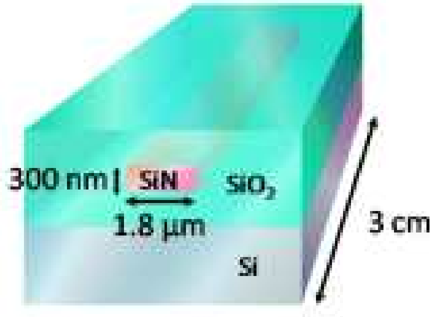
Lecture 9: Si Waveguides

Dielectric waveguides for Si photonics



Core: Si
Cladding: SiO_2

(~1dB/cm)



Core: SiN
Cladding: SiO_2

Smaller loss but larger size (~ 0.01dB/cm)

➔ Passive devices only

How to analyze 3-dimensional dielectric waveguides ?

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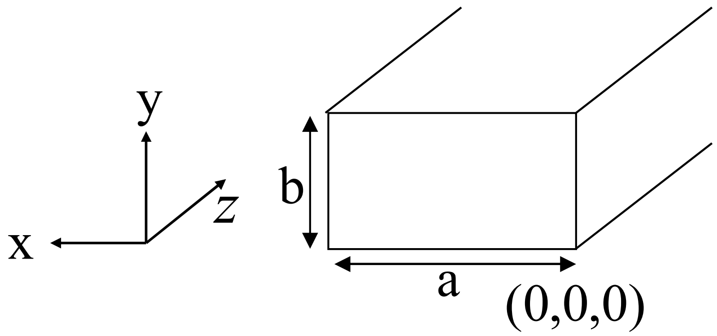
3-D Metallic Waveguide



$$\overline{E}(x,y,z,t) = \overline{E}(x,y) \cdot e^{-jkz} \cdot e^{j\omega t}$$

$$\nabla^2{}_{xy}\overline{E} + (-k^2 + \mu\varepsilon\omega^2)\overline{E} = 0$$

➔ 2-D Wave Equation

1) Transverse Electro-Magnetic (TEM) solution: $E_z=H_z=0$

➔ Cables, Transmission lines (But not for dielectric waveguides)

2) Transverse Electric waves (TE_{mn})
$E_z=0$ but H_z nonzero

3) Transverse Magnetic waves (TM_{mn})
$H_z=0$ but E_z nonzero

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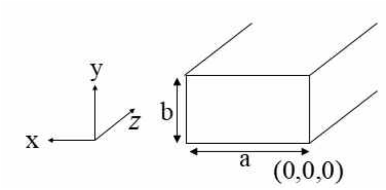


TE_{11}

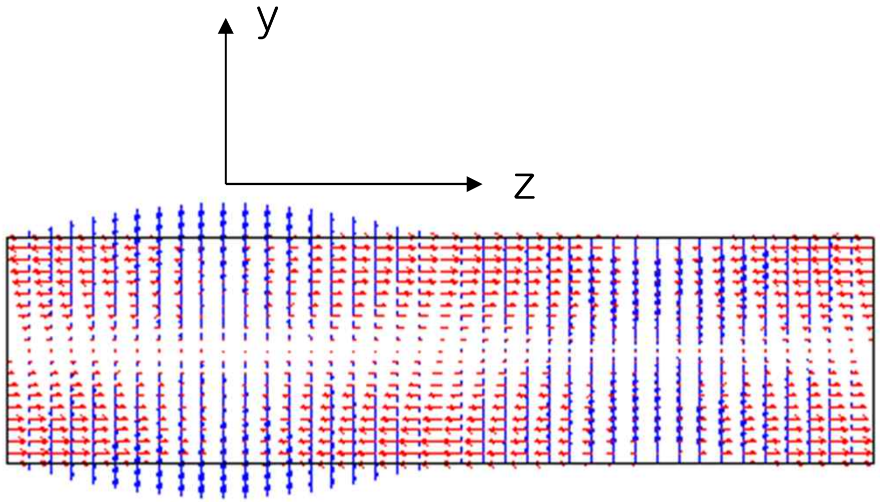
$$E_x(x,y,z,t) \sim \cos(\frac{\pi}{a}x)\sin(\frac{\pi}{b}y)\sin(\omega t-\beta z)$$

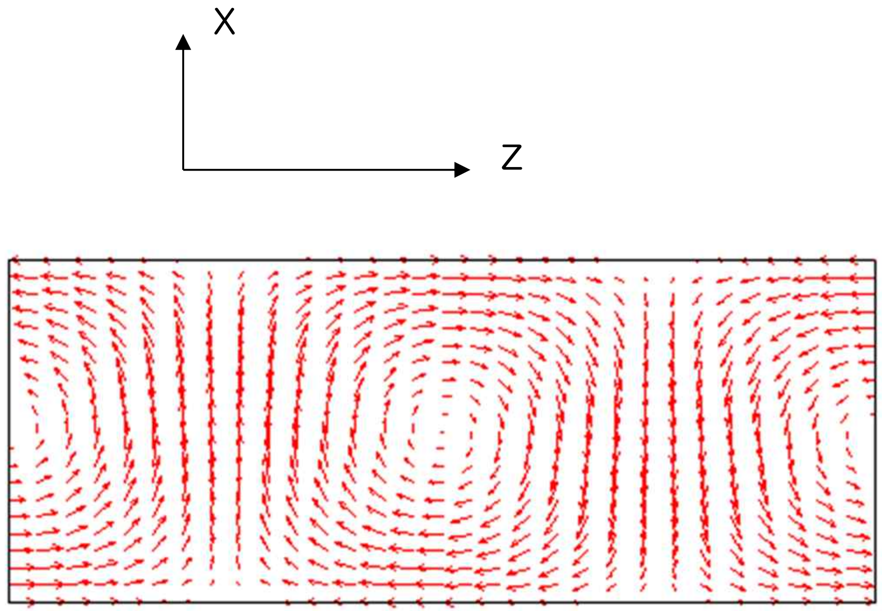
$$E_y(x,y,z,t) \sim \sin(\frac{\pi}{a}x)\cos(\frac{\pi}{b}y)\sin(\omega t-\beta z)$$

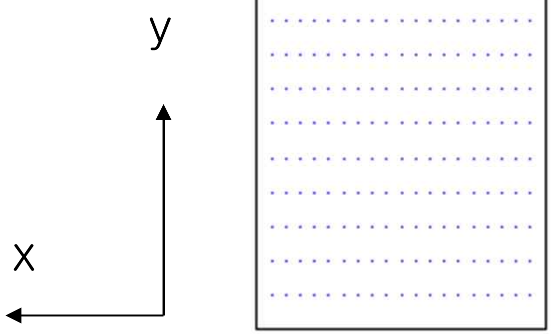
$$H_x(x,y,z,t) \sim \sin(\frac{\pi}{a}x)\cos(\frac{\pi}{b}y)\sin(\omega t-\beta z)$$

$$H_y(x,y,z,t) \sim \cos(\frac{\pi}{a}x)\sin(\frac{\pi}{b}y)\sin(\omega t-\beta z)$$

$$H_z(x,y,z,t) \sim \cos(\frac{\pi}{a}x)\cos(\frac{\pi}{b}y)\cos(\omega t-\beta z)$$







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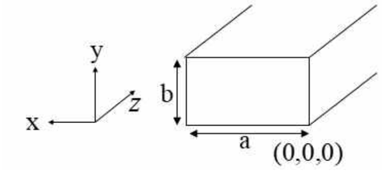
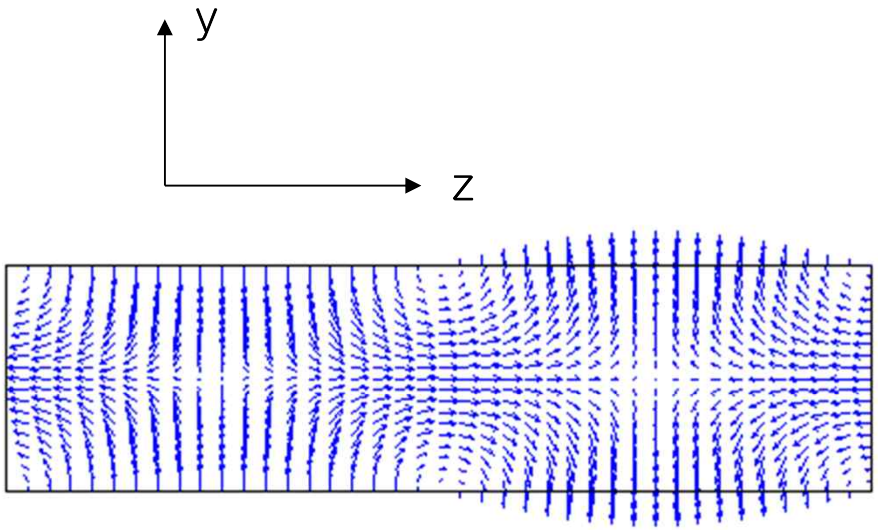




TM_{11}

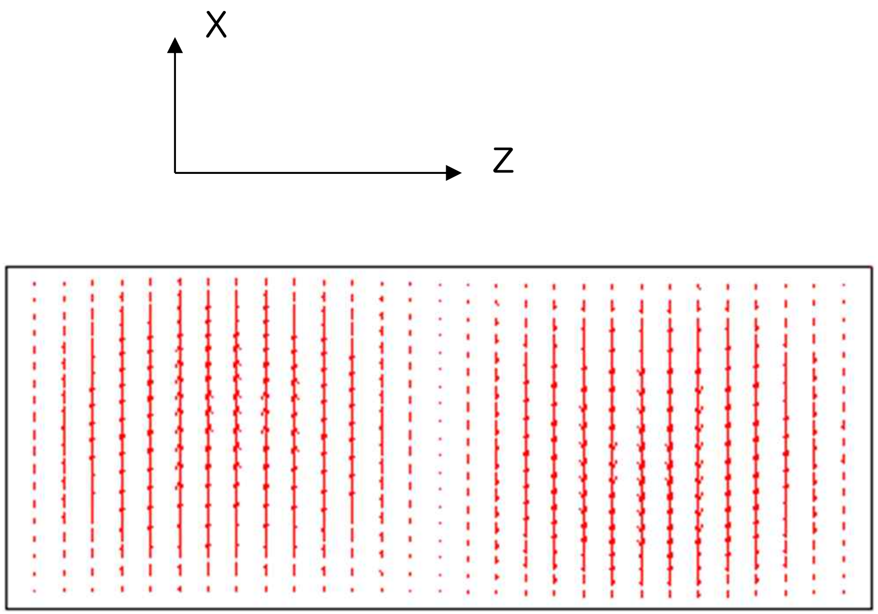
$$E_x(x,y,z,t) \sim \cos(\frac{\pi}{a}x)\sin(\frac{\pi}{b}y)\sin(\omega t - \beta z)$$

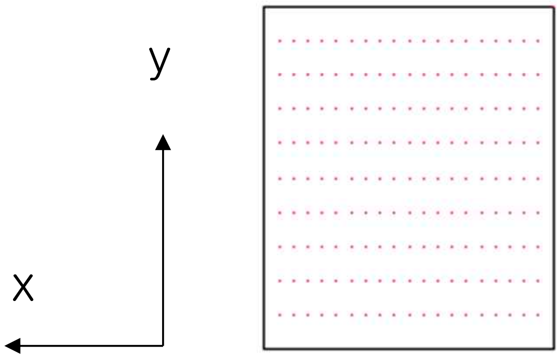
$$E_y(x,y,z,t) \sim \sin(\frac{\pi}{a}x)\cos(\frac{\pi}{b}y)\sin(\omega t - \beta z)$$

$$E_z(x,y,z,t) \sim \sin(\frac{\pi}{a}x)\sin(\frac{\pi}{b}y)\cos(\omega t - \beta z)$$

$$H_x(x,y,z,t) \sim \sin(\frac{\pi}{a}x)\cos(\frac{\pi}{b}y)\sin(\omega t - \beta z)$$

$$H_y(x,y,z,t) \sim \cos(\frac{\pi}{a}x)\sin(\frac{\pi}{b}y)\sin(\omega t - \beta z)$$





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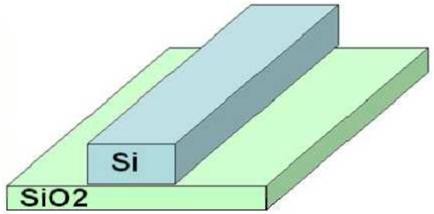
Metallic waveguides used
for very high-frequency electric signals

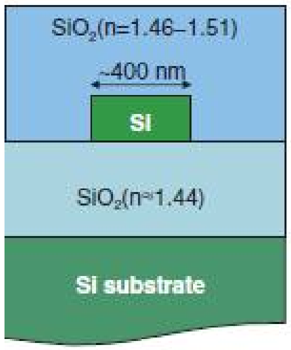
But too lossy for light propagation



No pure TE_{mn}, TM_{mn} mode solutions

➔ Mixture of TE_{mn} and TM_{mn} ➔ Hybrid modes

For lowest-order modes in planar waveguides,
very good approximation with



HE_{mn}: Hybrid with TE dominant ➔ TE_{mn} (TE-like)

E-field pointing (approximately) **horizontally**

EH_{mn}: Hybrid with TM dominant ➔ TM_{mn} (TM-like)

E-field pointing (approximately) **vertically**

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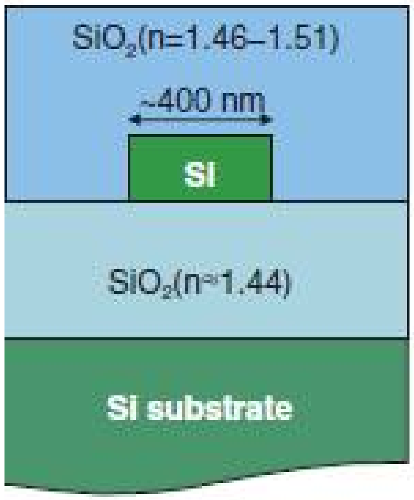
3-D Dielectric Waveguide for Si photonics



Analytical solution still very complicated

Analytical approximation techniques

Effective Index Method

Coupled Mode Theory

Numerical techniques

Finite Difference Time Domain (TDTD) Method

(Numerical solution of wave equation)

Beam Propagation Method

Eigenmode Expansion Method

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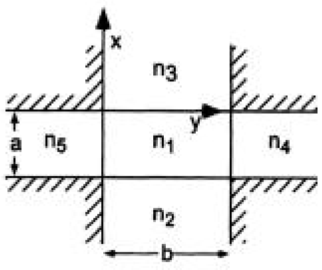
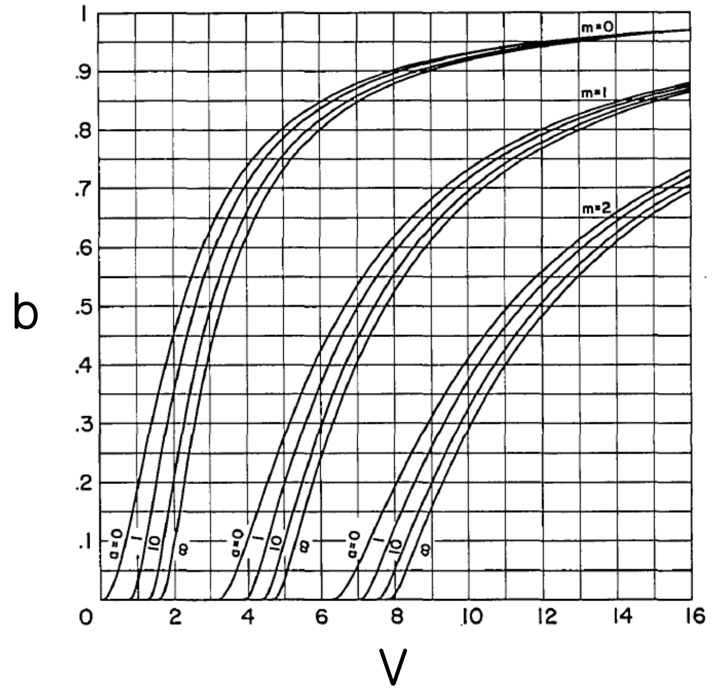
Effective Index Method

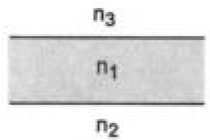
2D problem ➔ Two 1-D problems



n_{eff} for the first TE-like mode?

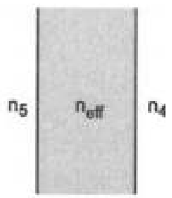


Determine TE n_{eff} for the three-layer problem using the b-V diagram



$$V = k_0 d (n_1^2 - n_2^2)^{1/2} \qquad b = \frac{\left(\beta / k_0\right)^2 - n_2^2}{n_1^2 - n_2^2}$$

Determine TM n_{eff} for the three-layer problem



$$a = \frac{n_2^2 - n_3^2}{n_1^2 - n_2^2} \text{ for TE, } a = \frac{n_1^4}{n_3^4}\frac{n_2^2 - n_3^2}{n_1^2 - n_2^2} \text{ for TM}$$

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Homework #1

Core: Si with n = 3.47

Cladding: SiO_2 with n = 1.44

W = 500nm, H=220nm

Estimate n_{eff} for the fundamental mode (TE-like) at 1550 nm
using the effective index method. Assume the cladding layer extends infinitely.

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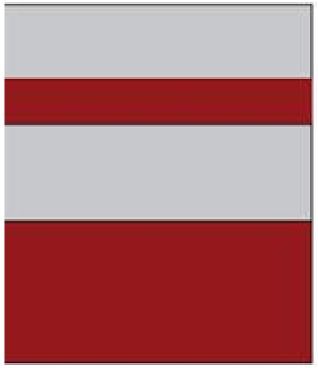
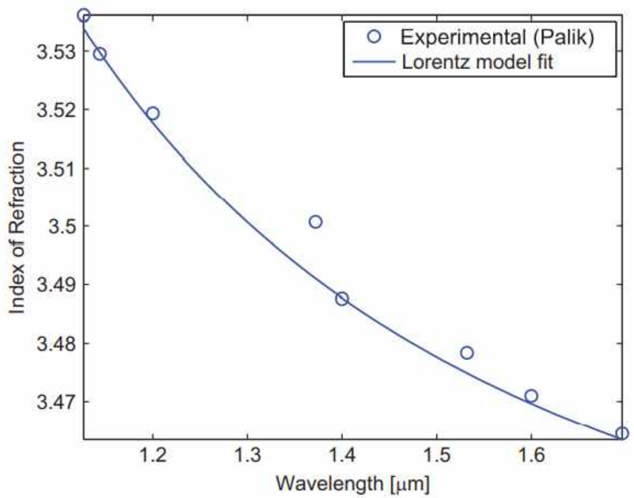


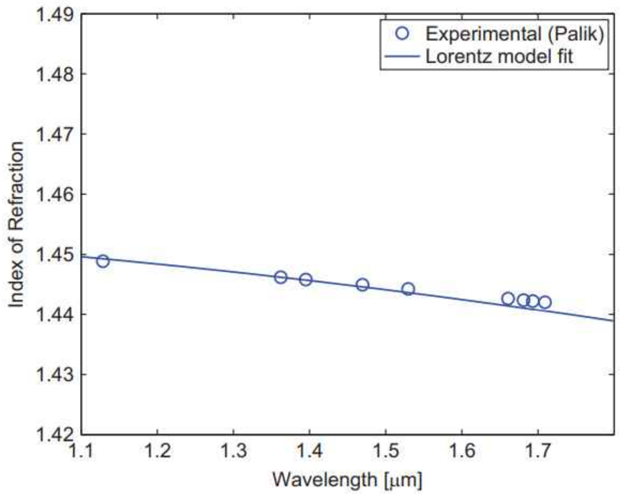
➔ SOI thickness for single mode?

Refractive Index

Si



SiO_2



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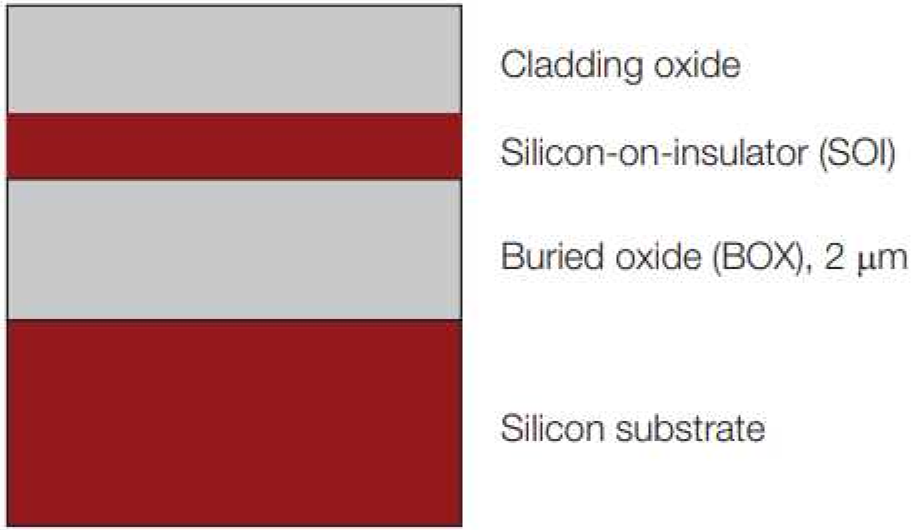
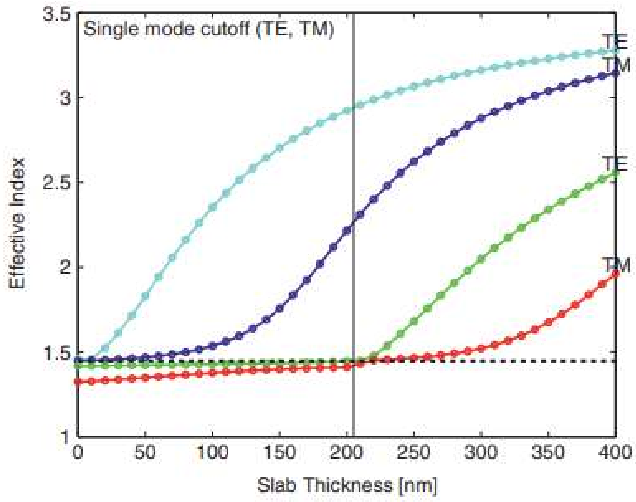
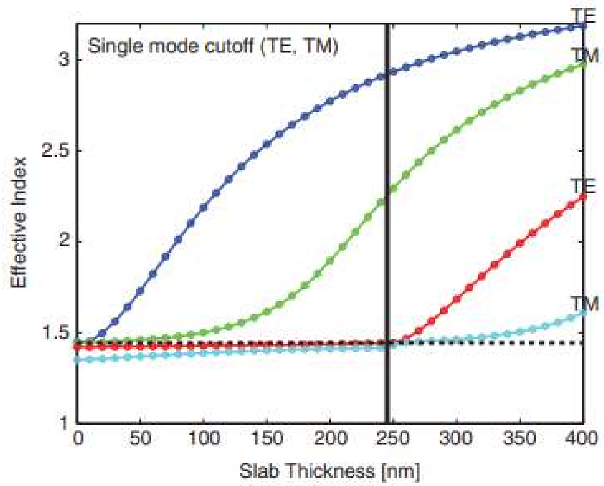
SOI Thickness for single mode?





Wavelength of 1310 nm.



Wavelength of 1550 nm.

(If cladding oxide and buried oxide sufficiently thick, can be approximated with three-layer waveguide)

➔ SOI thickness: 220nm

At 1550nm, TE: n_{eff}=2.845 TM: n_{eff}=2.054

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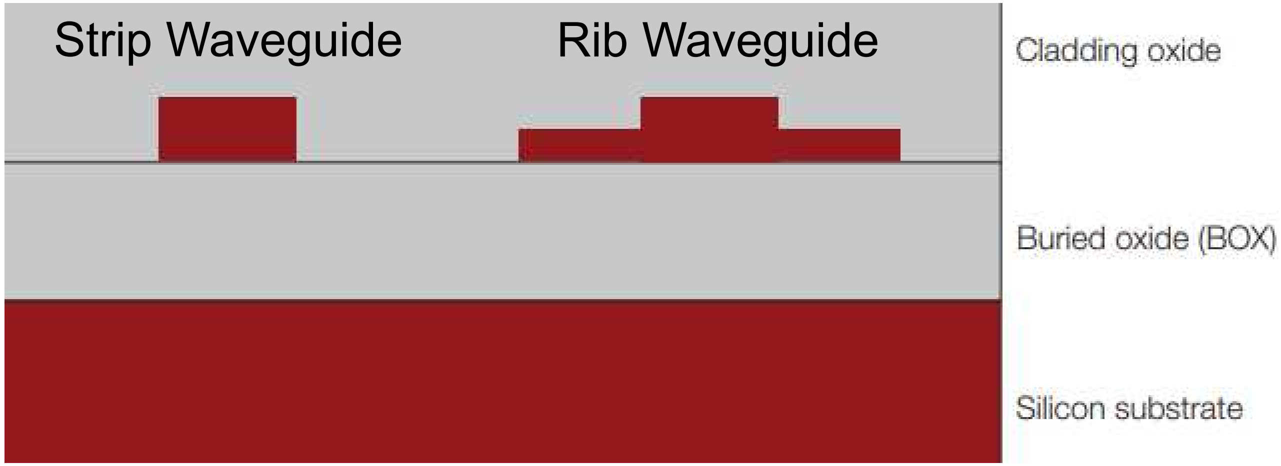
Lateral guidance



Difference?

More tightly guided in strip than in rib waveguide

Larger loss in strip than in rip waveguide

Smaller bending radius for strip waveguide

Waveguide width for single mode?

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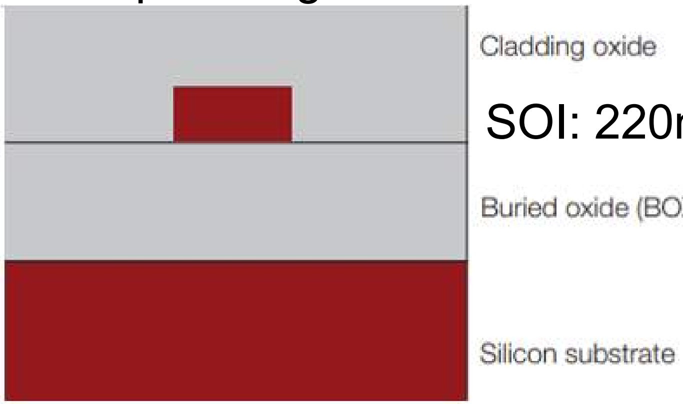
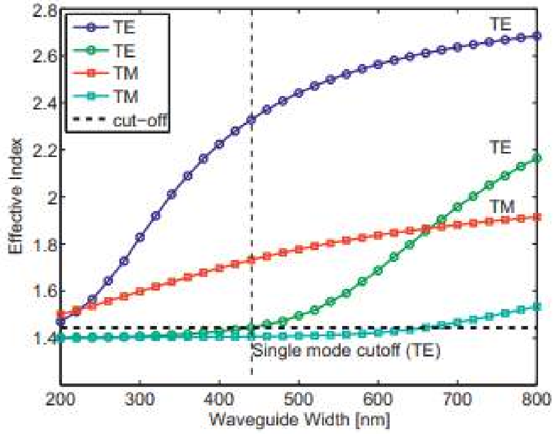
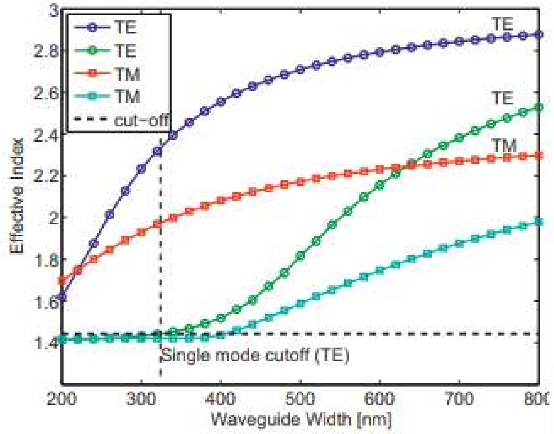
Strip Waveguide



SOI: 220nm



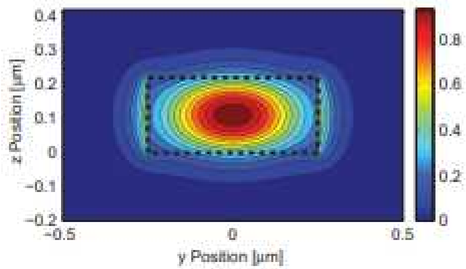
Wavelength of 1550 nm



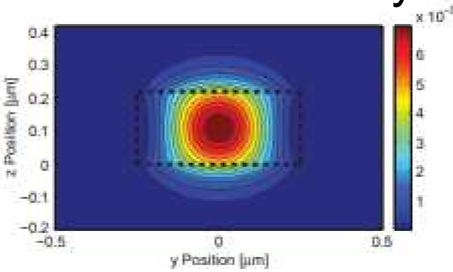
Wavelength of 1310 nm

500 x 220 nm

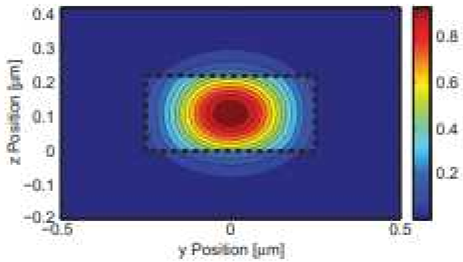
E-field intensity



H-field intensity



Energy



Strip width for single mode operation?

< ~ 440 nm at 1550nm

< ~ 320 nm at 1310nm

TE/TM filtering is required at the input

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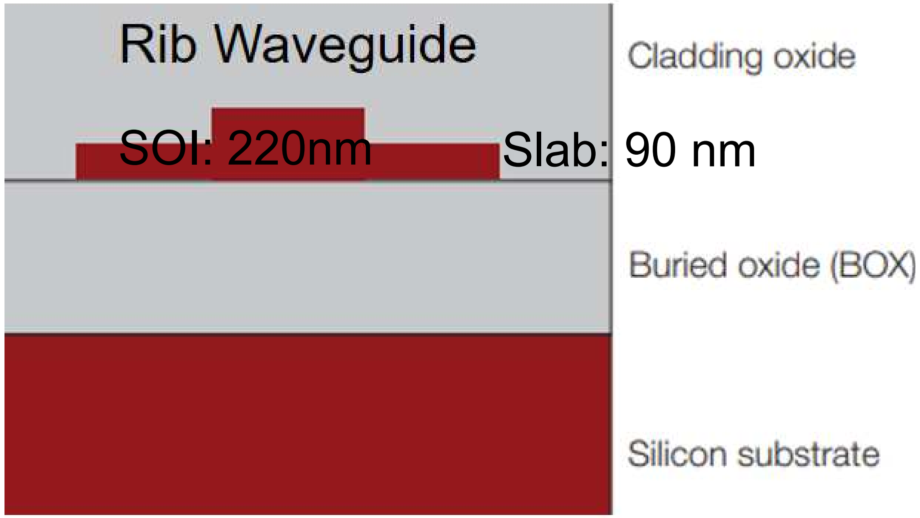

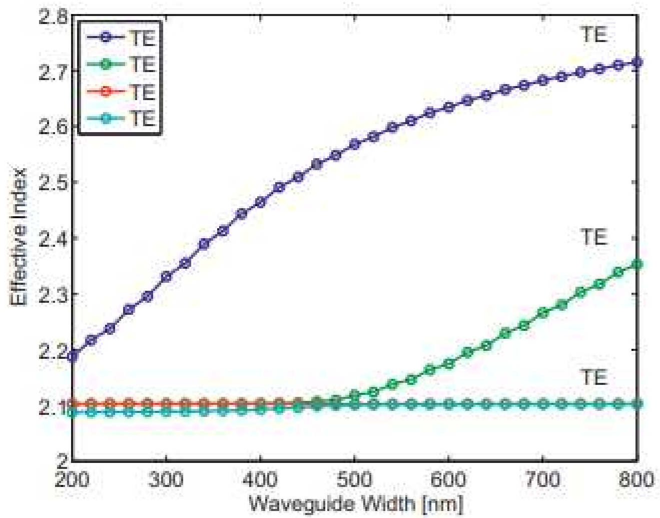

Strip width for single mode operation?

< 500 nm

No TM-like guided modes

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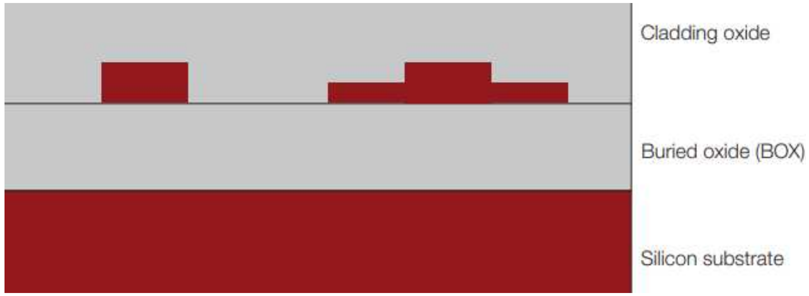
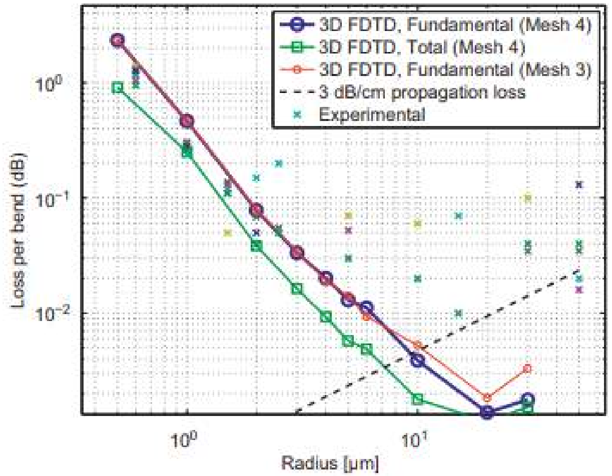
Loss



500 x 220 strip

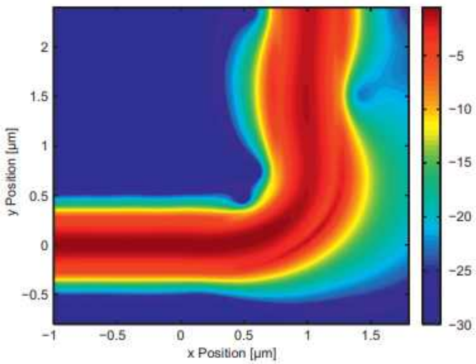


- Propagation loss: sidewall scattering loss of a few dB/cm

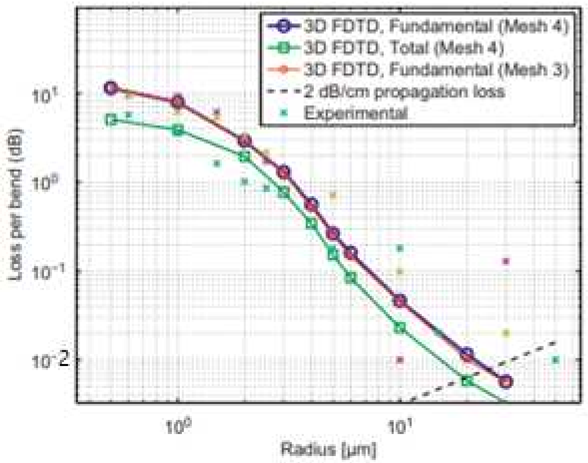
strip > rib

- Bending loss: mode mismatch, larger for smaller radius

rib > strip



500 x 220 rib



➔ Strip waveguide for routing, rib waveguide for device

Lecture 9: Si Waveguides

How to fabricate Si waveguides ➔ Si (CMOS) fabrication technology

300 mm Si wafer

Unit processes on Si wafer

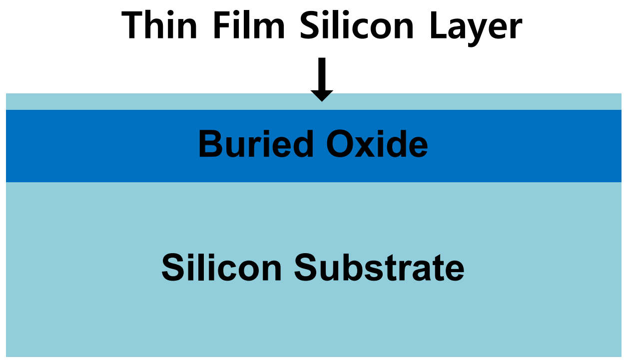
- Thin Film Deposition
- Etching
- Ion Implantation
- Photolithography
- Chemical Mechanical Polishing

Lecture 9: Si Waveguides

SOI (Silicon on Insulator):

A thin layer of silicon crystal on top of insulator on the top on insulator

< SOI Wafer >



- **Why SOI wafer?**

  MOS devices on SOI is more robust again many short channel effects, leading to faster operation with less power consumption

  Developed by IBM and Used by IBM and Motorola (Now Freescale) for high-performance microprocessors but lost to Intel's bulk Si technology

  ➔ Now used for Si Photonics and RF circuit applications

Lecture 9: Si Waveguides

➢ Smart-Cut Process

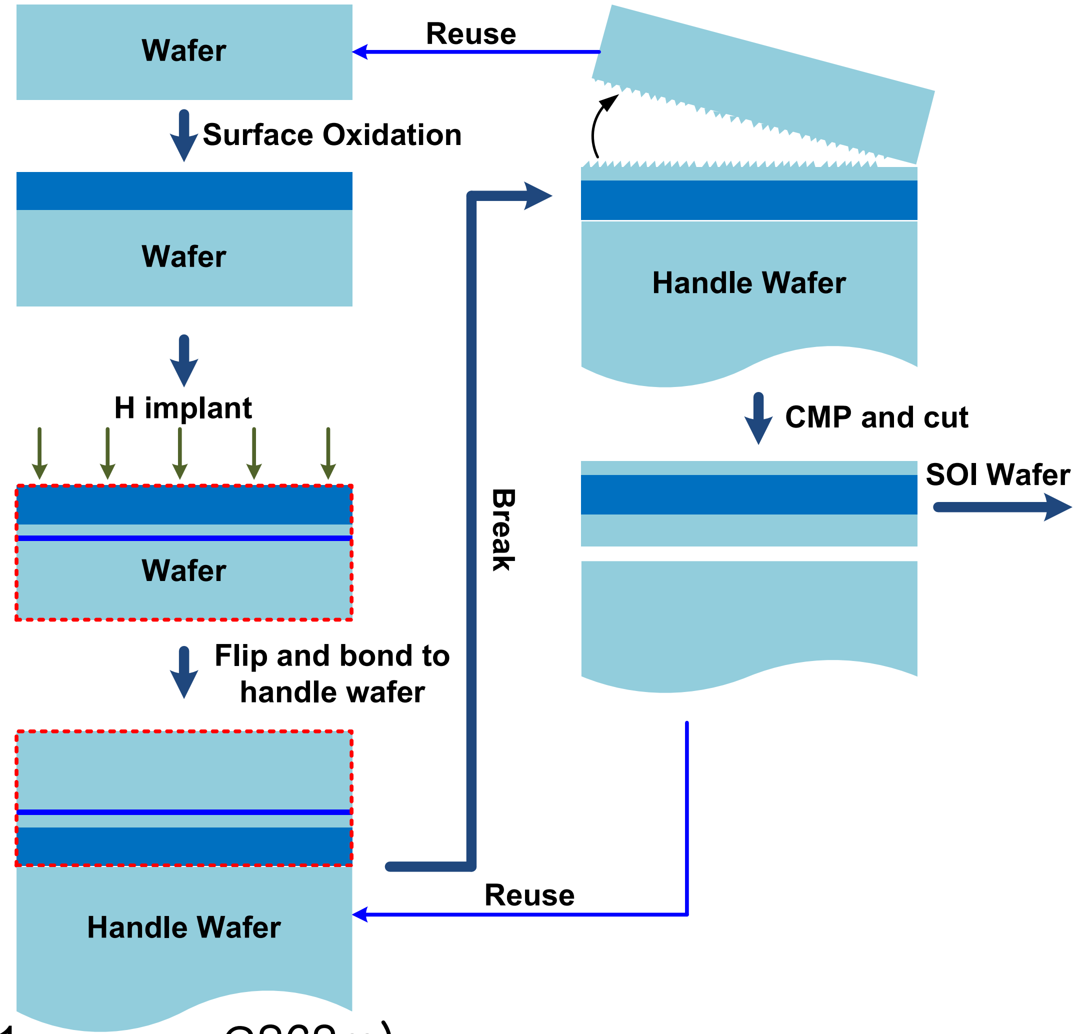
Surface Oxidation onto wafer

Implantation of hydrogen into wafer

Deposition of a thick layer or bonding wafer to another wafer

Heat treatment inducing splitting

Polishing and cutting

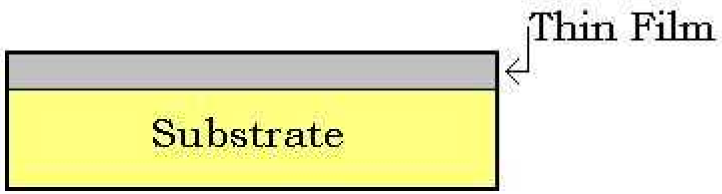


Developed and sold by Soitech (2021 revenue €863m)

Lecture 9: Si Waveguides

1. Thin Film Deposition

- Layer of materials ranging from fractions of nanometer to several micro-meters in thickness (oxide, nitride. metal, poly-silicon …)



- Types of Thin Film Deposition

- Physical Vapor Deposition (PVD)

  - Vaporized materials bombard onto substrate

- Chemical Vapor Deposition (CVD)

  - Gaseous materials react on substrate

- Oxidation

  - Oxidize Si into SiO_2 (consumes Si, 44%)

  - Wet or dry oxidation

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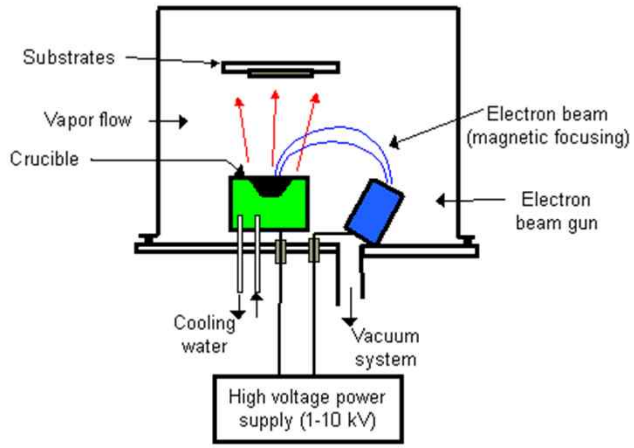
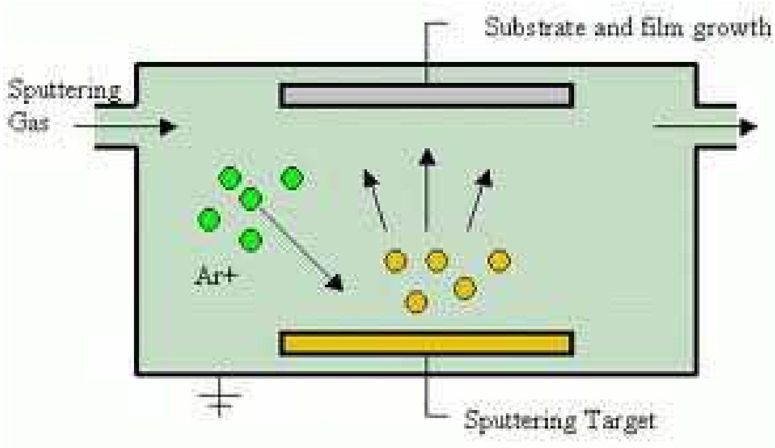
Physical Vapor Deposition (PVD)

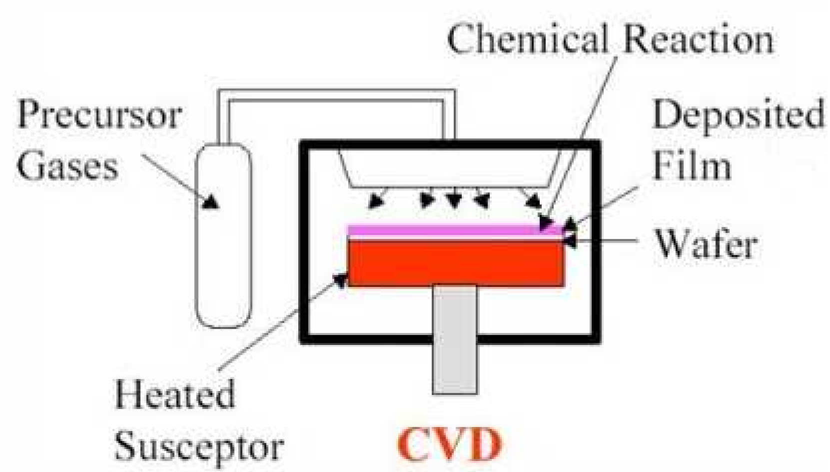
- Evaporation (Thermal, E-beam)
- Sputtering (DC, RF, Ion beam)
- Aluminum, Copper, Titanium, Tungsten silicide





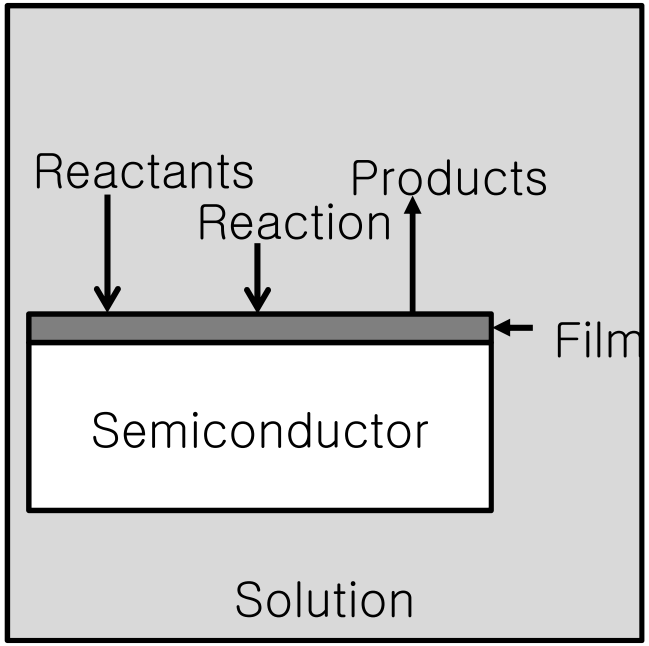
Chemical Vapor Deposition (CVD)

- Gases react on the substrate to form the desired thin films
- LPCVD (Low Pressure)
  PECVD (Plasma Enhanced)
  LACVD (Laser Assisted)
  MOCVD (Metal Organic) …



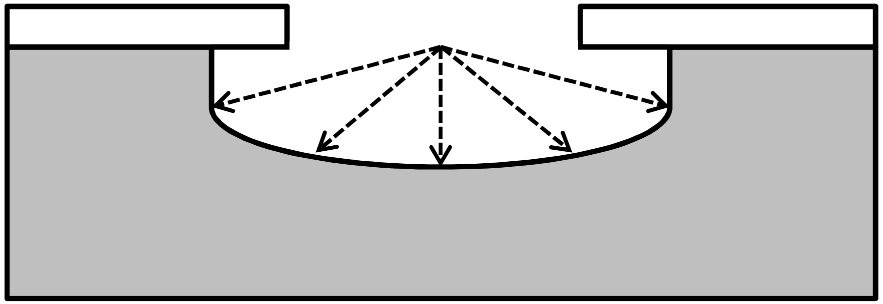
2. Etching

Wet Etching



- SiO_2 etching by HF
- Si_3N_4 etching by H_3PO_4
- Si etching by KOH

-Wet etching avoided if possible:
hazard materials, undercut



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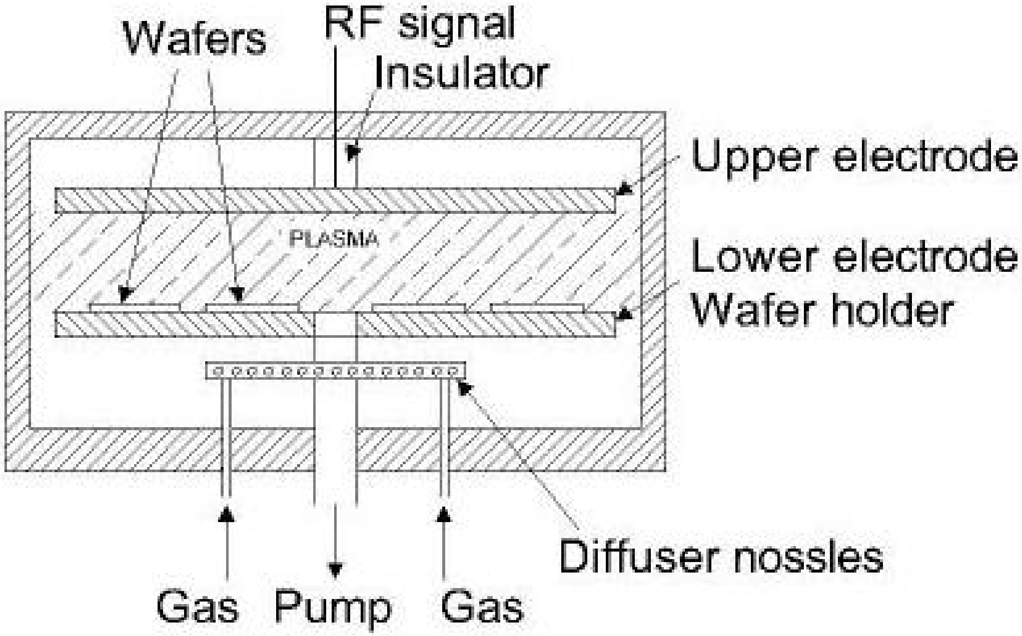
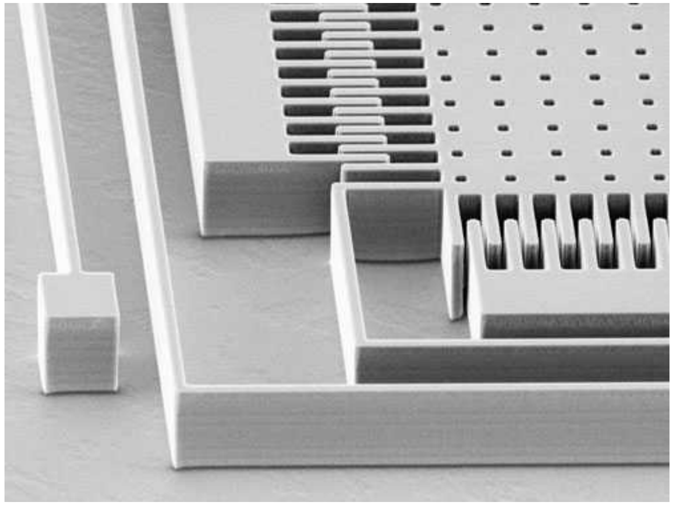
- Dry etching: chemical reaction with gases to eliminate desired material

RIE (Reactive Ion Etching), IBE (Ion Beam Etching) …

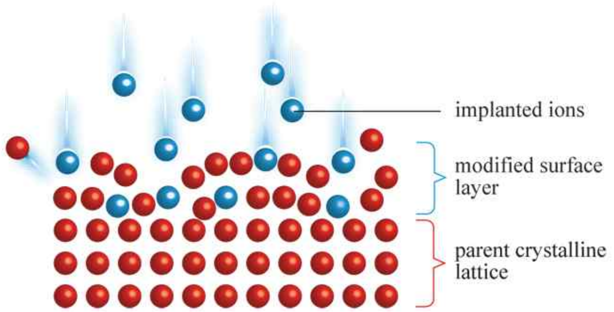


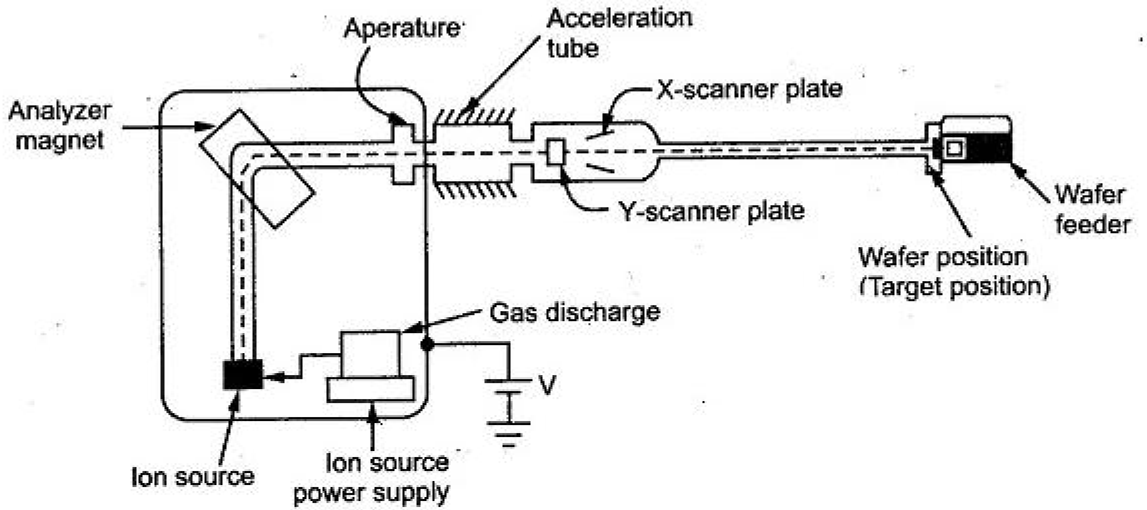
RIE system



3. Ion Implantation

Ions are accelerated by potential difference and implanted into the substrate





Ion flux and potential difference carefully controlled

for desired doping concentration profile

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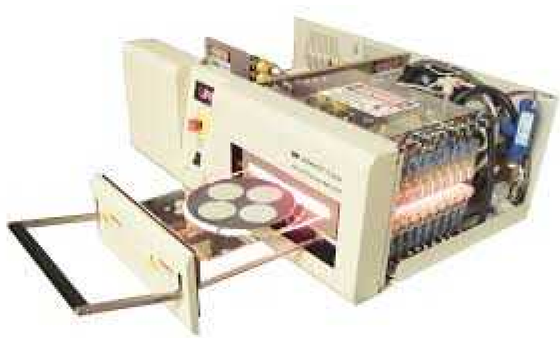
Dopants:

B for P-doping, As/P for N-doping

Rapid Thermal Annealing (RTA) is performed after implantation



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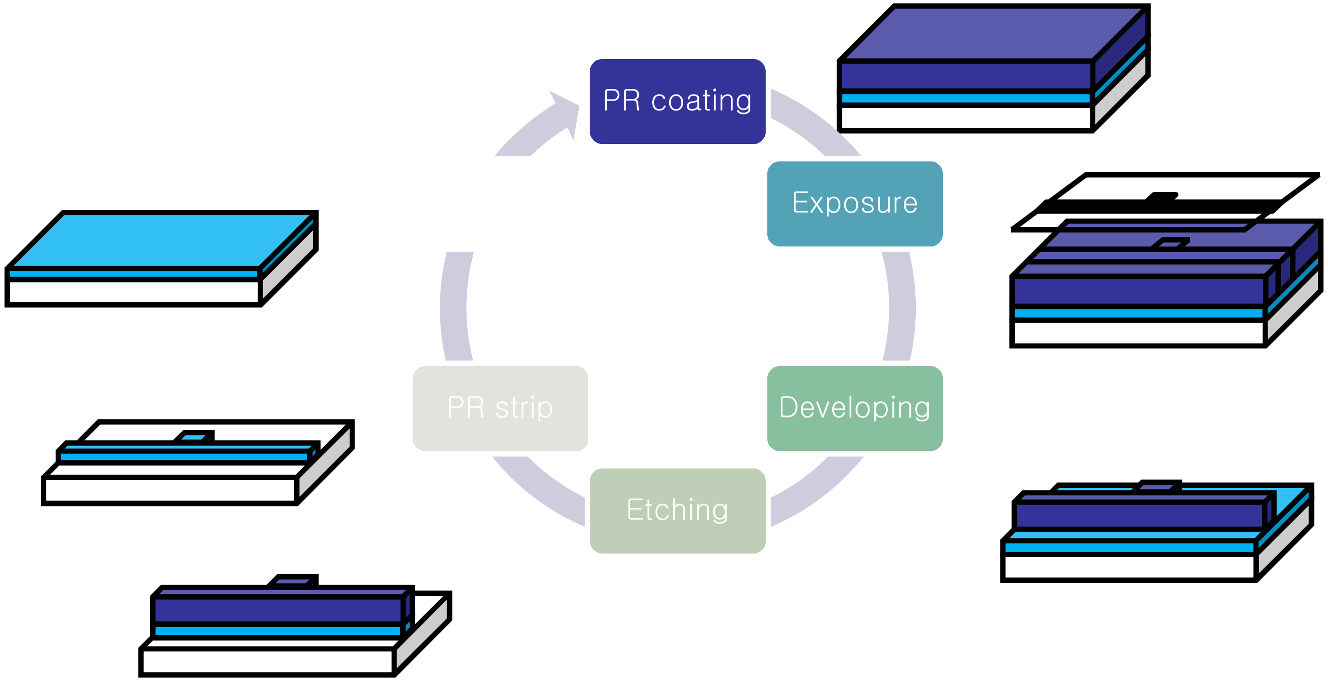
4. Photolithography

➢ Produces patterns on substrate by transferring mask patterns onto the substrate. Basically lithographic printing



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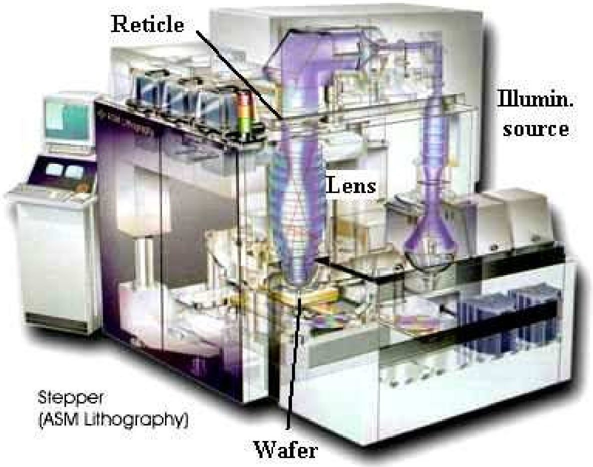
Stepper



g-line → i-line → KrF → ArF → F_2

436 nm → 365 nm → 248 nm → 193 nm → 157 nm

13.5 nm for

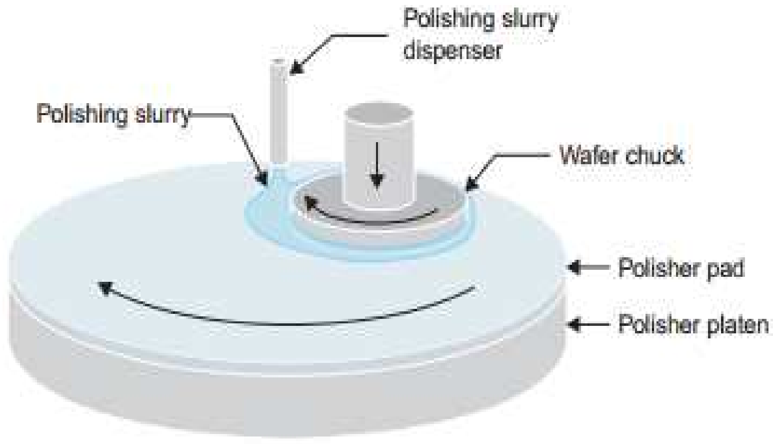
Extreme Ultraviolet Lithography

(EUV)

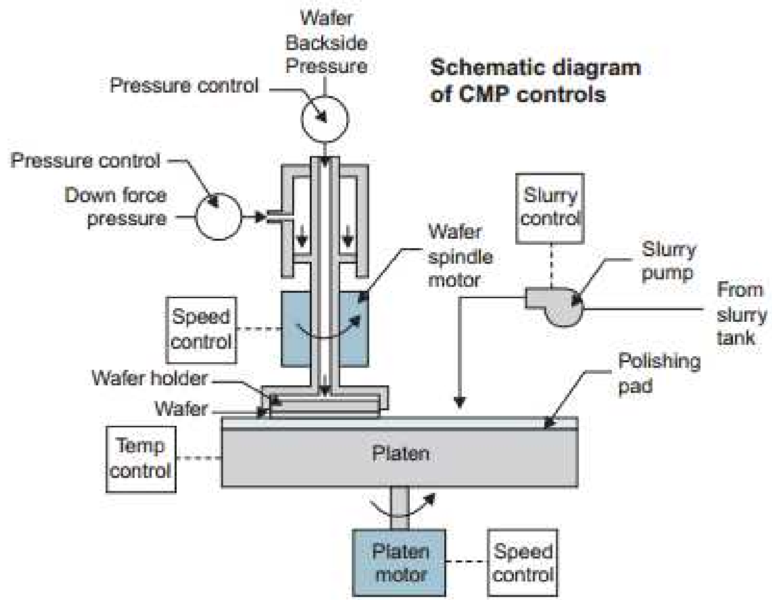
Lecture 9: Si Waveguides

5. Chemical Mechanical Polishing (CMP)

➢ Makes the wafer surface flat for better lithography

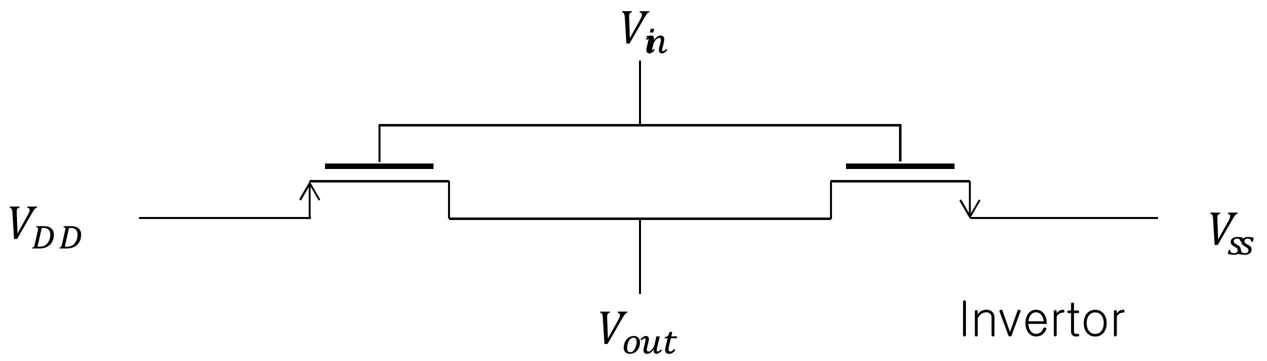


Rotary CMP tool

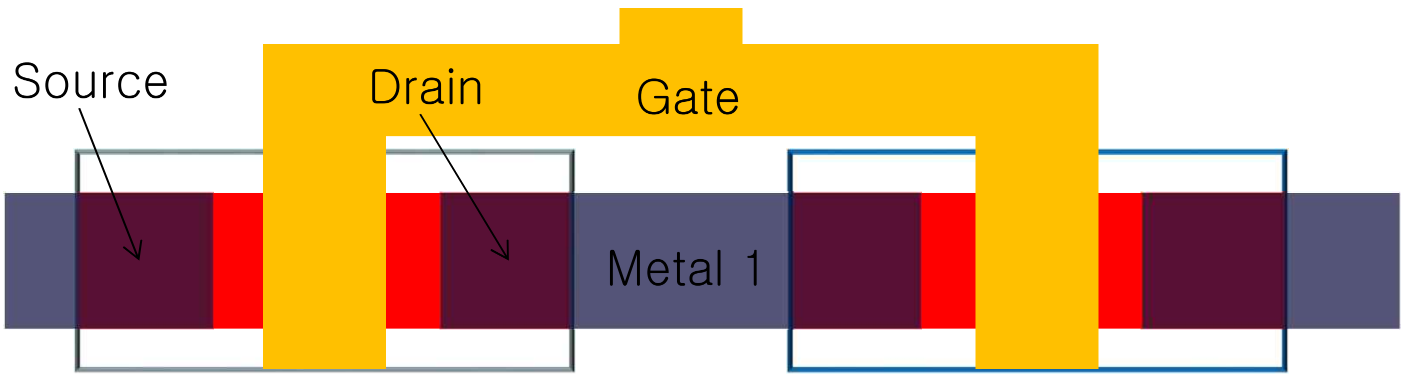


- Chemical Mechanical Planarization(CMP) combines chemical action with mechanical abrasion to achieve selective material removal through polishing

- **CMOS inverter**

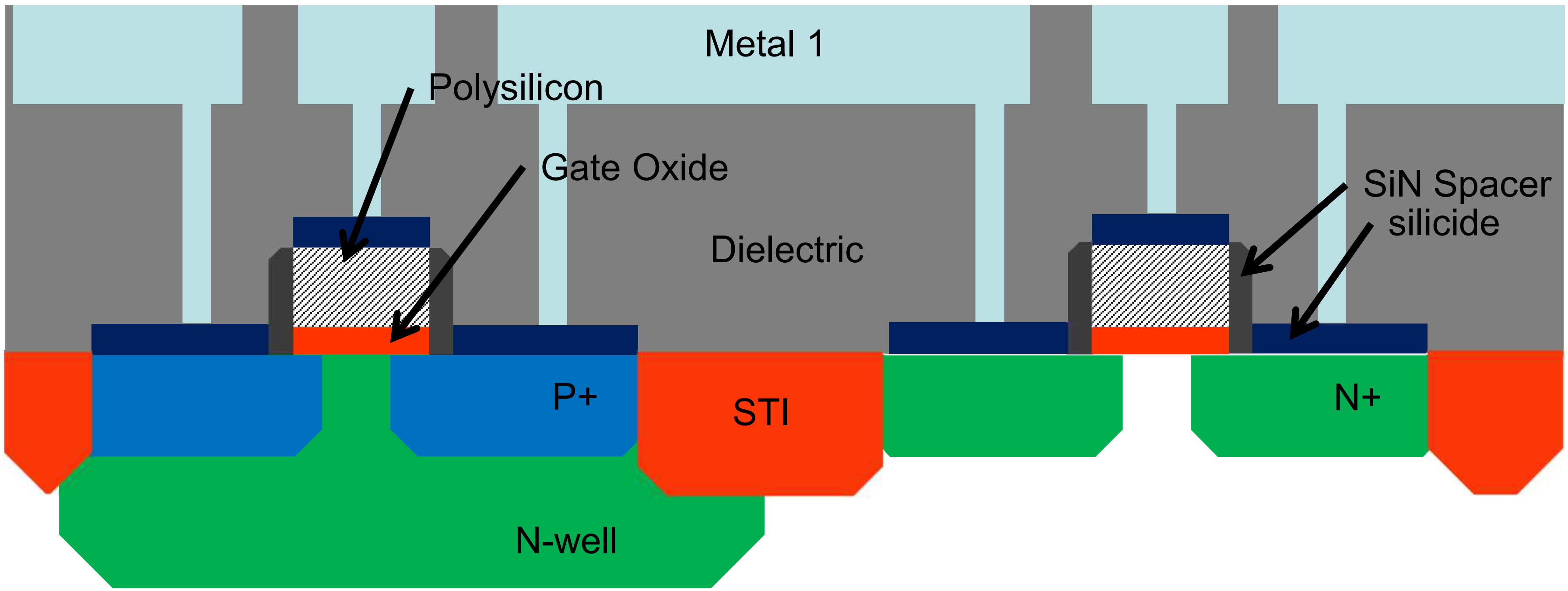


- **Layout**



Lecture 9: Si Waveguides

- **CMOS Structure**



➔ Simplified fabrication steps follow

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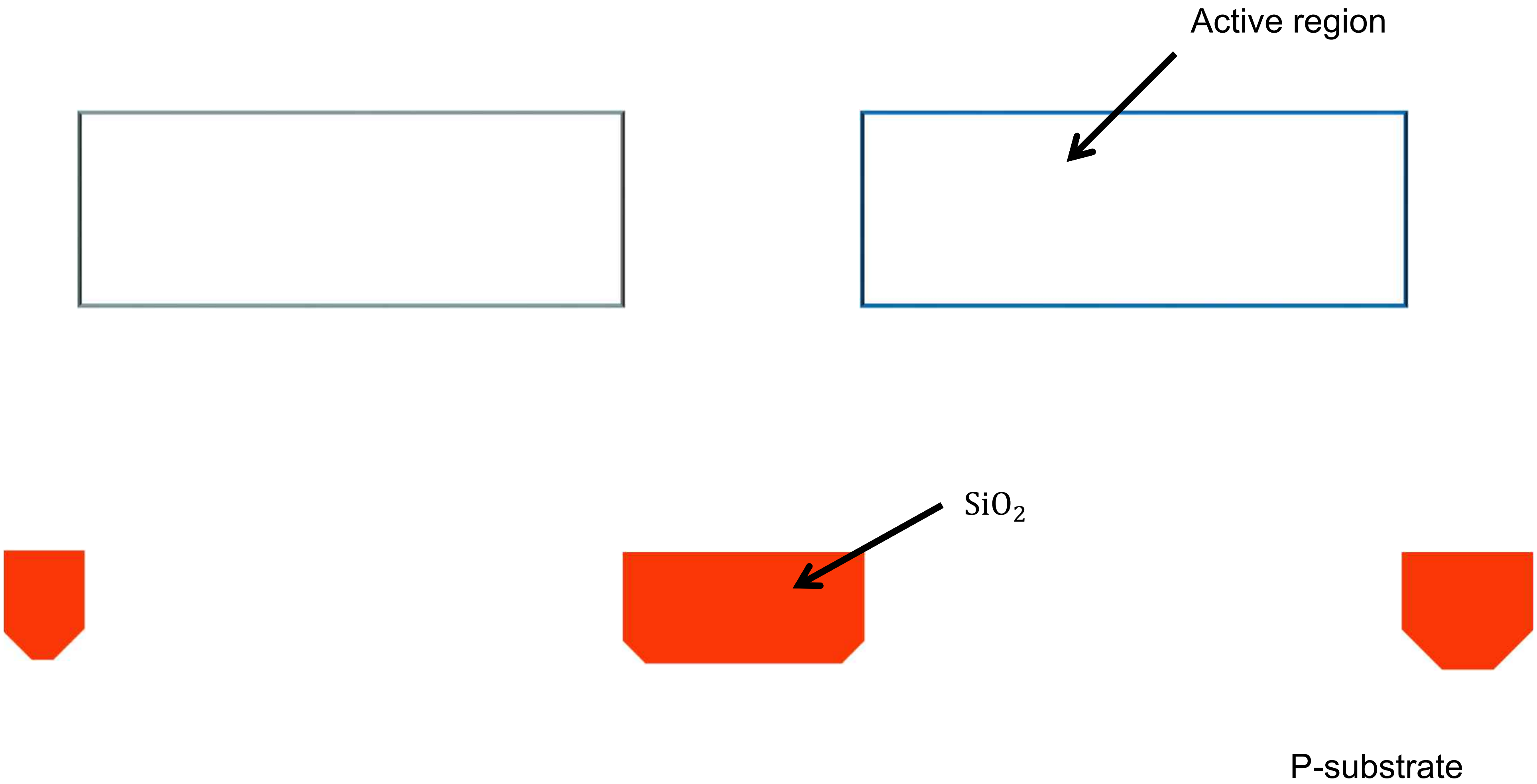
- **Shallow Trench Isolation(STI) (for printing)**



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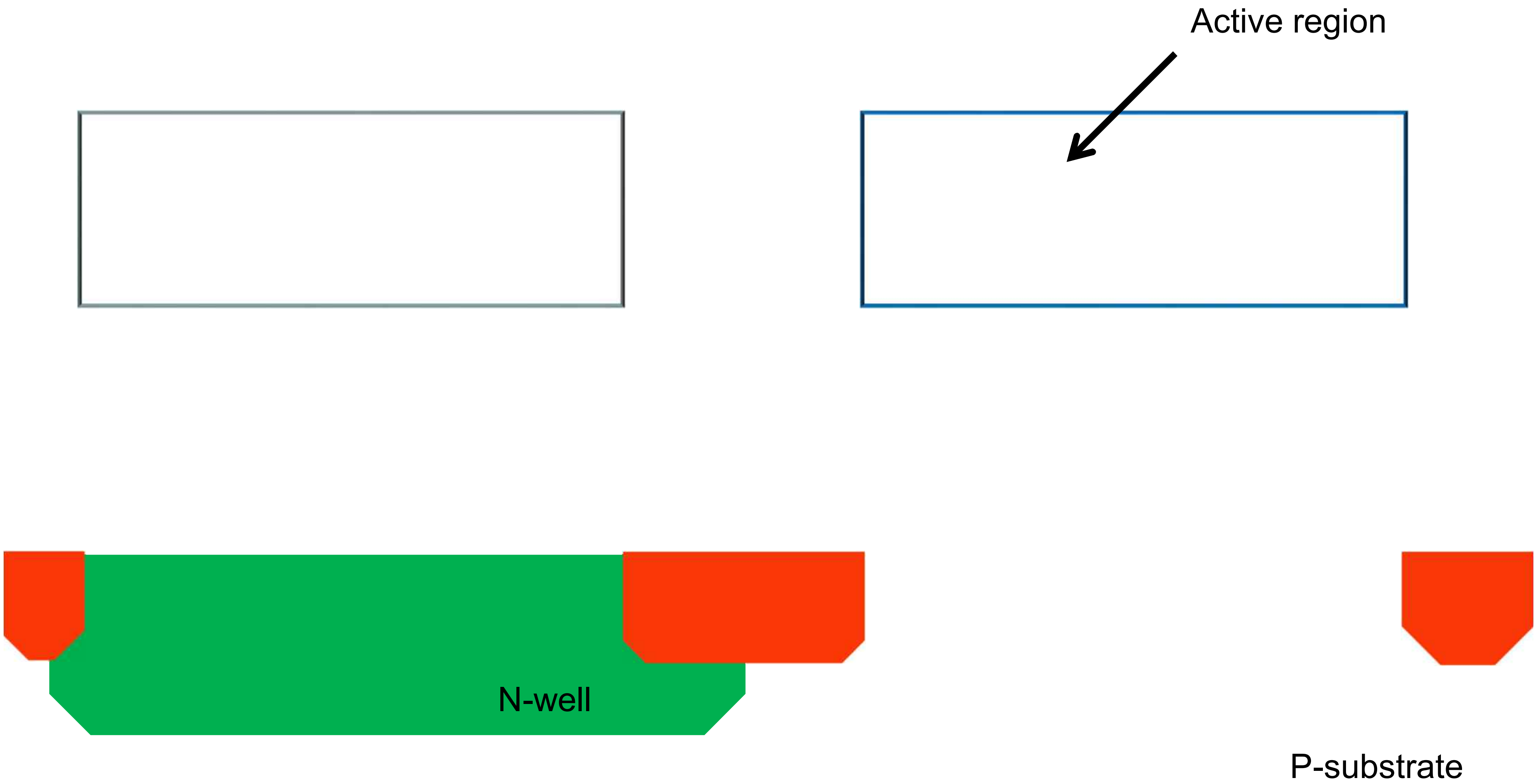
- **Well Formation (for printing)**



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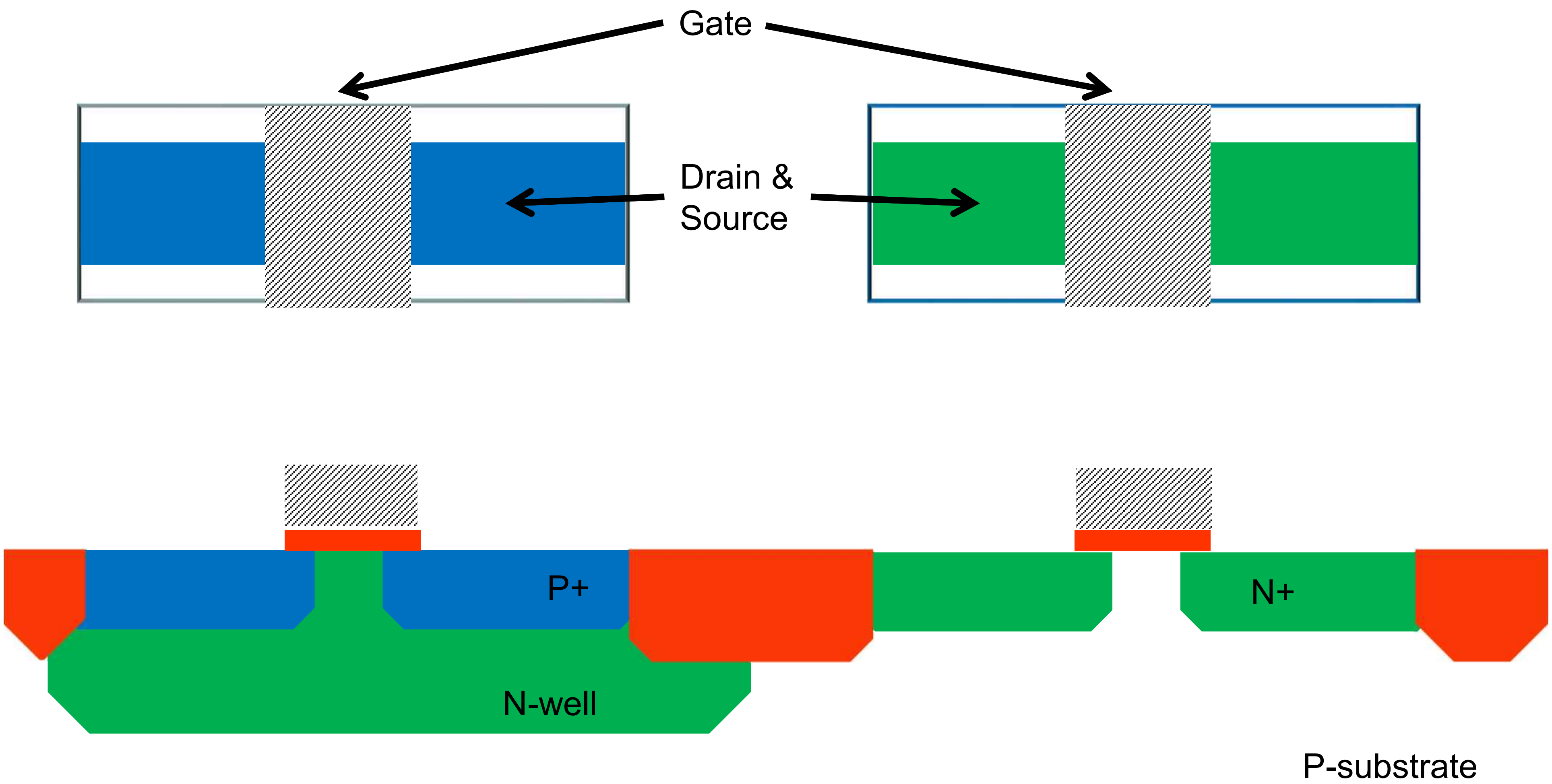
- **Gate and Source/Drain Formation (for printing)**



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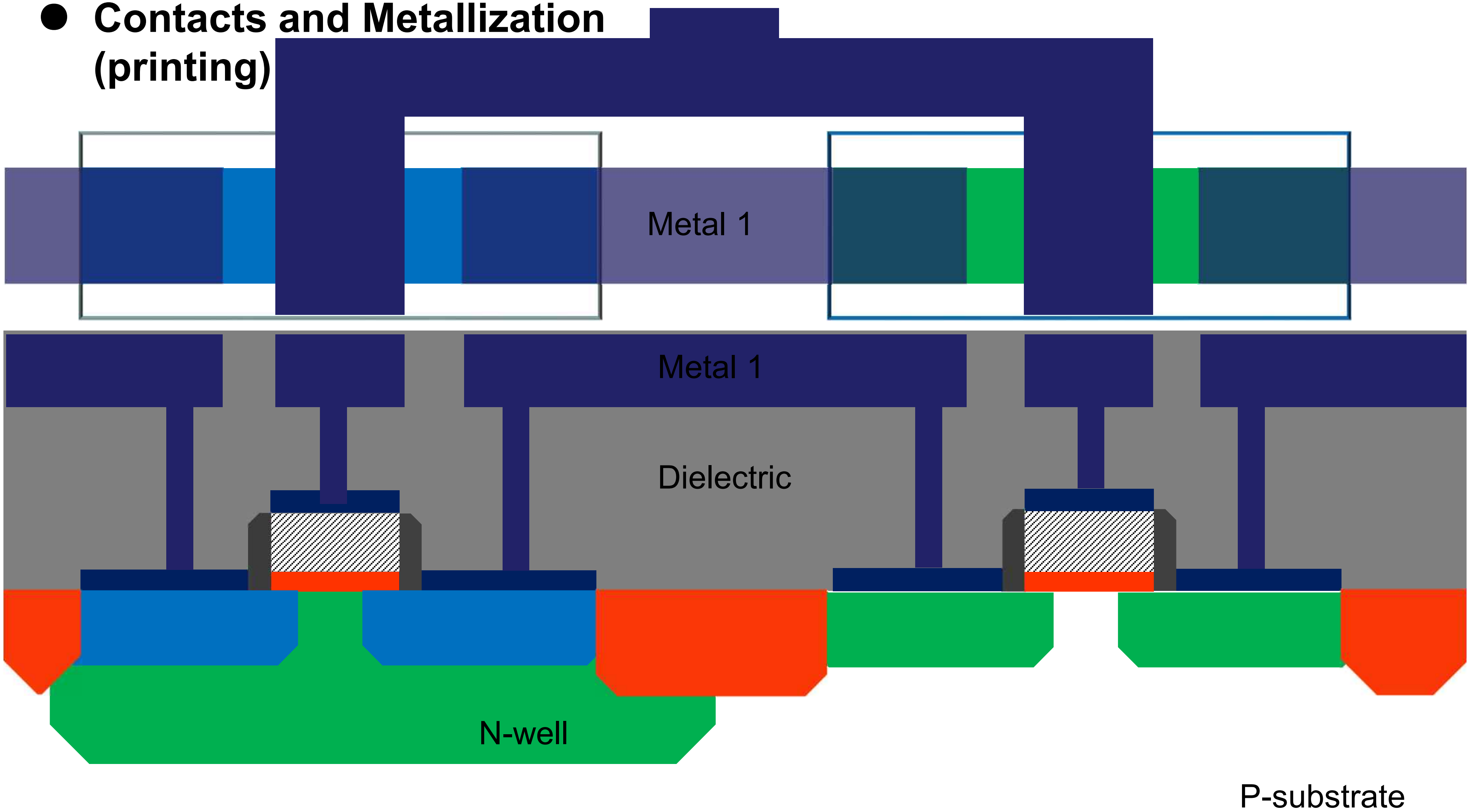
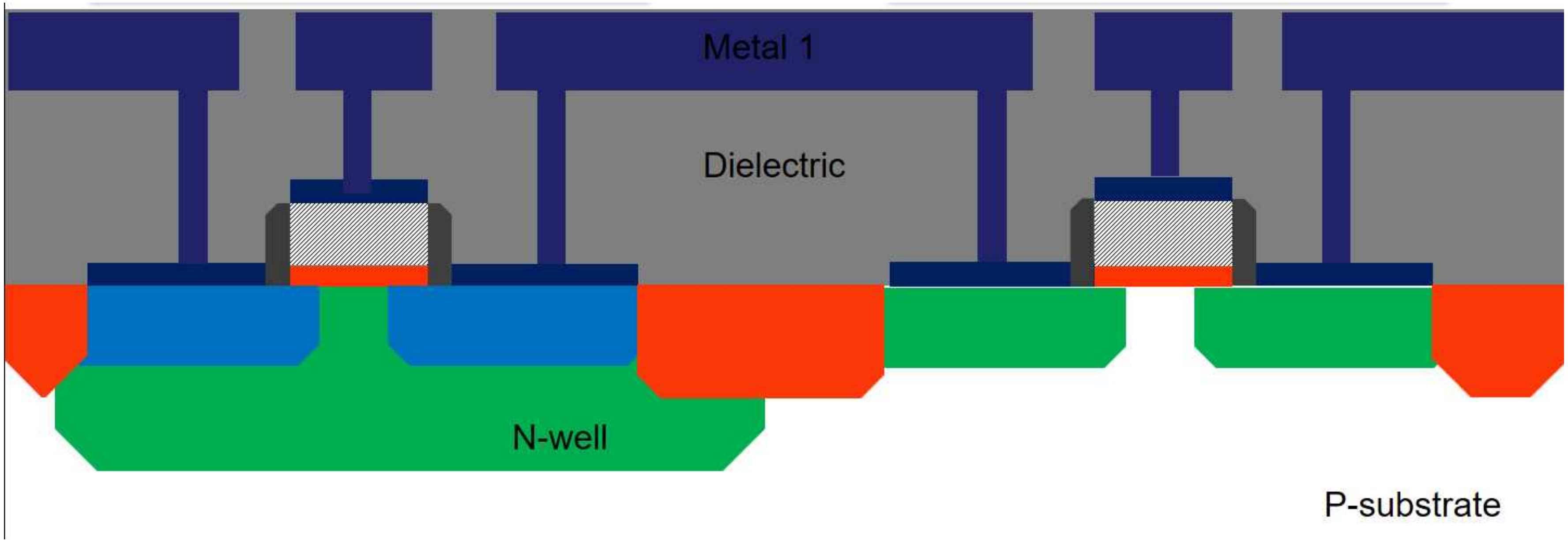
- **Contacts and Metallization (printing)**



Lecture 9: Si Waveguides

Homework #2



List the processing steps that are needed for fabricating above CMOS structure.
For each step, specify the required unit process and draw the cross section