Performance Optimization and Improvement of Silicon Avalanche Photodetectors in Standard CMOS Technology

Myung-Jae Lee, *Member, IEEE*, and Woo-Young Choi, *Member, IEEE*

(Invited Paper)

***Abstract*—This paper discusses design optimization for silicon avalanche photodetectors (APDs) fabricated in standard complementary metal-oxide-semiconductor (CMOS) technology in order to achieve the highest possible performance. Such factors as PN junctions, guard ring structures, active areas, and back-end structures are considered for the optimization. CMOS-APDs reflecting varying aspects of these factors are fabricated and their performances are characterized. In addition, their characteristics are analyzed with technology computer-aided-design simulations and equivalent circuit models. From these investigations, dominant factors that influence the CMOS-APD performance are identified. Furthermore, three different techniques enabling further performance improvements of CMOS-APDs are investigated, which are spatial-modulation, carrier-acceleration, and multijunction techniques. The state-of-the-art CMOS-APDs' structures and performances are presented and compared, and the best optimized CMOS-APD is proposed. These results should be extremely useful for realizing optimal silicon APDs in standard CMOS technology for various applications.**

***Index Terms*—Avalanche photodetector (APD), avalanche photodiode, carrier acceleration, edge breakdown, equivalent circuit model, guard ring, image sensor, inductive peaking, integrated circuit modeling, multiple junction, optical detector, optical interconnect, photodetection bandwidth, photodetector, photodiode, silicon photonics, spatially-modulated avalanche photodetector, standard CMOS technology.**

I. Introduction

DEVELOPMENT of high-performance optical detectors based on silicon technology is attracting a great amount of interests for a wide variety of applications, including optical communications and interconnects, next-generation optical networks, imaging, and sensing. These interests are mainly due to the feasibility of fabricating optical detectors based on the mature silicon complementary metal-oxide-semiconductor (CMOS) fabrication technology [1]–[6]. Basically, there are two lines of research for these: one for $1.3-1.55\ \mu$m applications utilizing germanium on silicon [7]–[14], and the other for 850 nm and visible wavelength applications using silicon as a photodetection material. In the latter case, optical detectors can be fabricated in the standard CMOS technology without any process modification and, consequently, very straight-forward monolithic integration with electronic circuits is possible. 850 nm optical interconnects are actively investigated for such applications as home networks [15], vehicular communications [16], rack-to-rack interconnects within data centers and computer clusters [17], [18], chip-level interconnects [19], and on-board interconnects [20]–[22]. The fact that low-cost vertical-cavity surface-emitting lasers (VCSELs) and multimode fibers (MMFs) are easily available and there are packaging solutions offering the excellent cost-performance ratio makes this approach based on optical detectors fabricated in the standard CMOS more appealing. In particular, CMOS-compatible avalanche photodetectors (CMOS-APDs) with their built-in gain can greatly enhance system performances in many applications including bio-imaging [23], [24], robotic and automotive applications [25], optical wireless communications (OWCs) [26], and visible light communications (VLCs) [27], [28] as well as 850 nm optical interconnects [15]–[22].

Since standard CMOS technology does not provide the optimal fabrication processes for APDs, there have been intense research interests for improving the performance of APDs based on the standard CMOS technology [29]–[43]. In this paper, we present the results of our investigations in which we identify the influence of such factors on CMOS-APD performance as PN junctions, guard rings (GRs), active areas, and back-end processes. For these, many different types of CMOS-APDs are fabricated, and their performances are characterized, which are then analyzed with technology computer-aided-design (TCAD) simulations and equivalent circuit models. From these investigations, dominant factors that influence the CMOS-APD performance are identified, and various techniques to improve the CMOS-APD performance further, especially for higher photodetection bandwidth, are demonstrated.

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M.-J. Lee is with the School of Engineering, École Polytechnique Fédérale de Lausanne, Neuchâtel 2002, Switzerland.

W.-Y. Choi is with the Department of Electrical and Electronic Engineering, Yonsei University, Seoul 03722, South Korea (e-mail: wchoi@yonsei.ac.kr).

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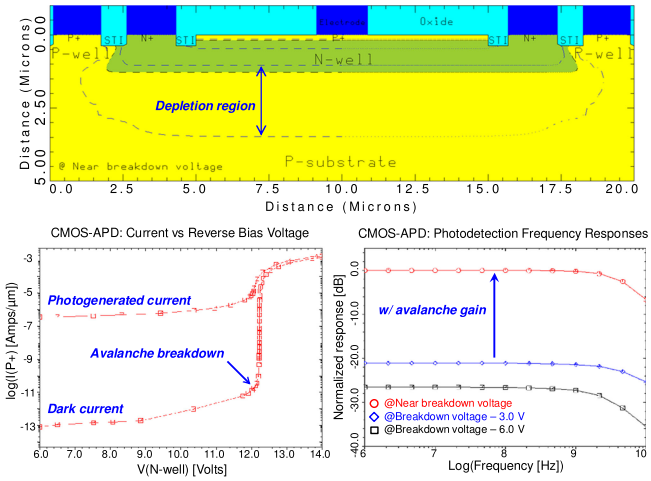

Fig. 1. Examples of TCAD simulation results for CMOS-APDs.

This paper is organized as follows. Section II explains simulation and modeling methods for CMOS-APDs, and Section III describes design considerations such as PN junction, GR, active area, and back end. In Section IV, some techniques to achieve higher performance CMOS-APDs having larger photodetection bandwidth or higher responsivity with wider spectrum range are presented and discussed. Section V summarizes this paper.

II. Simulation and Modeling Methods

A. TCAD Simulation

Many aspects of CMOS-APDs can be accurately simulated using TCAD including doping profiles, dark currents, avalanche breakdown voltages, electric-field profiles, as well as photocurrents, spectral responses, and photodetection frequency responses. Fig. 1 shows some examples of the TCAD simulations for a CMOS-APD in which we can clearly check its depletion region and charge-neutral region at around the breakdown voltage as well as its characteristics like avalanche breakdown voltage, dark current, and photogenerated current, photodetection frequency responses with different bias voltages.

The TCAD simulations provide many helpful guides for device design and fabrication. Although TCAD simulation results may not provide the desired accuracy mostly because every detail of the process steps may not be openly available, it is very helpful to analyze CMOS-APDs and to compare different device structures and parameters. In addition, by doing TCAD calibration with the measured data obtained from the fabricated CMOS-APDs, the device parameters can be extracted, which can be used for next fabrication.

B. Equivalent Circuit Modeling

In order to better understand CMOS-APD characteristics, equivalent circuit modeling for the device is essential. In particular, an accurate equivalent circuit model allows one to identify the amount of contribution for each of several factors that influence the photodetection frequency response of CMOS-APDs. In addition, the equivalent circuit model of CMOS-APDs provide

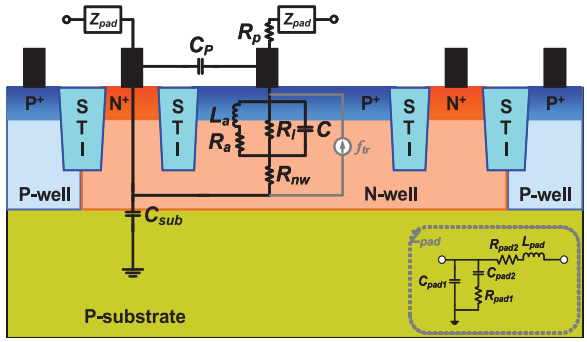

Fig. 2. Equivalent circuit model of CMOS-APDs based on the P^+/N-well junction [42].

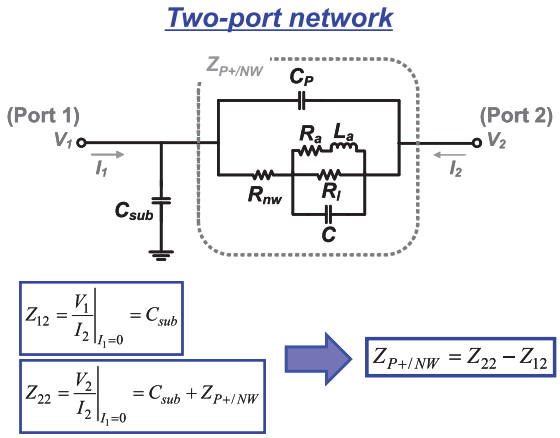

Fig. 3. Parameter extraction for the CMOS-APD equivalent circuit model.

very useful design guides when one tries to design electronic circuits that process photocurrents using the conventional circuit design tools.

Fig. 2 shows an equivalent circuit model for a CMOS-APD based on the P^+/N-well junction. The equivalent circuit includes an inductor with a parallel resistor and a capacitor for the junction in the avalanche regime. L_a represents phase delay between currents and voltages due to impact ionization, and R_a accounts for the finite reverse saturation current and the field-dependent velocity. R_l and C represent resistance and capacitance of the depletion region, respectively, and R_{nw} and C_{sub} are N-well resistance and N-well/P-substrate junction capacitance, respectively. C_p is the parasitic capacitance between N^+ and P^+ electrodes, and R_p is the parasitic resistance at the output of the device. Z_{pad} represents the equivalent circuit for the pad and metal interconnects. In addition, photogenerated currents are modeled as a current source having a single-pole frequency response with f_{tr} representing the 3-dB bandwidth of the current source.

The parameter values for the equivalent circuit elements are extracted from two-port Z-parameters determined from measured S-parameters. As shown in Fig. 3, C_{sub} is easily determined from Z_{12}, which is independent of other parameters. Then, $Z_{P+/NW}$ can be determined from $Z_{22} - Z_{12}$. The extracted values of the model can be confirmed with the theoretical estimation [35]. Once the parameter values are extracted, the current source is added as shown in Fig. 2, and by fitting

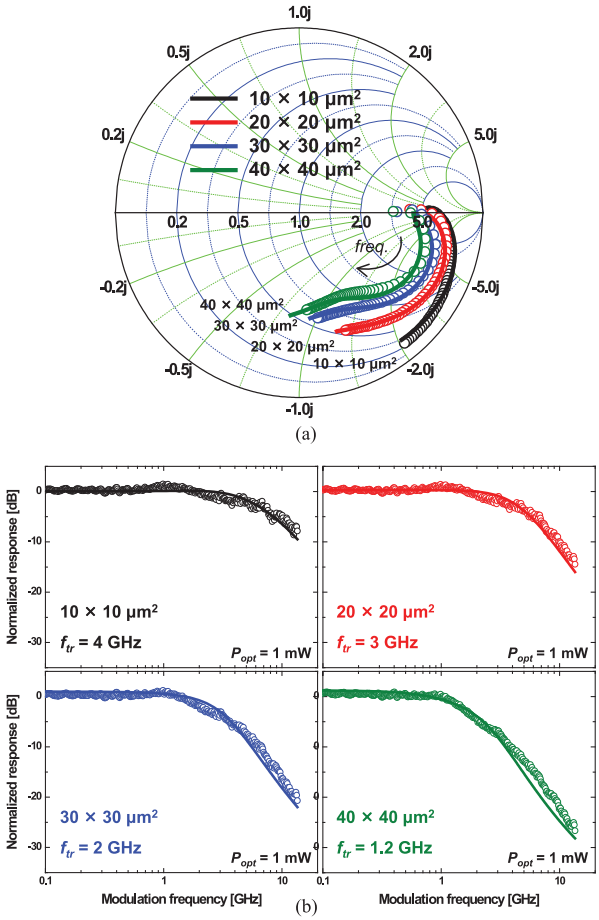

Fig. 4. (a) Measured and simulated electrical reflection coefficients and (b) photodetection frequency responses for different CMOS-APDs. Hollow circles represent the measured data and solid lines as the simulated results [39].

TABLE I
EXTRACTED PARAMETERS FOR CMOS-APDS [39]

	10×10 [μm²]	20×20 [μm²]	30×30 [μm²]	40×40 [μm²]
L_a [nH]	13			
R_a [Ω]	150			
R_l [kΩ]	1.2			
C [fF]	35	140	315	560
R_{nw} [Ω]	60	50	40	30
C_{sub} [fF]	15	45	90	150
C_p [fF]	20	60	120	180

the simulation results to the measured photodetection frequency response, the f_{tr} value is extracted.

Fig. 4(a) shows measured and simulated electrical reflection coefficients at the P^+ port of the device on Smith chart from 50 MHz to 13.5 GHz for CMOS-APDs having different active areas, and Fig. 4(b) shows normalized measured and simulated photodetection frequency responses for the CMOS-APDs [39]. As shown in these figures, the measured and simulated results show good matching. The extracted values of equivalent circuit parameters for the simulations are listed in Table I.

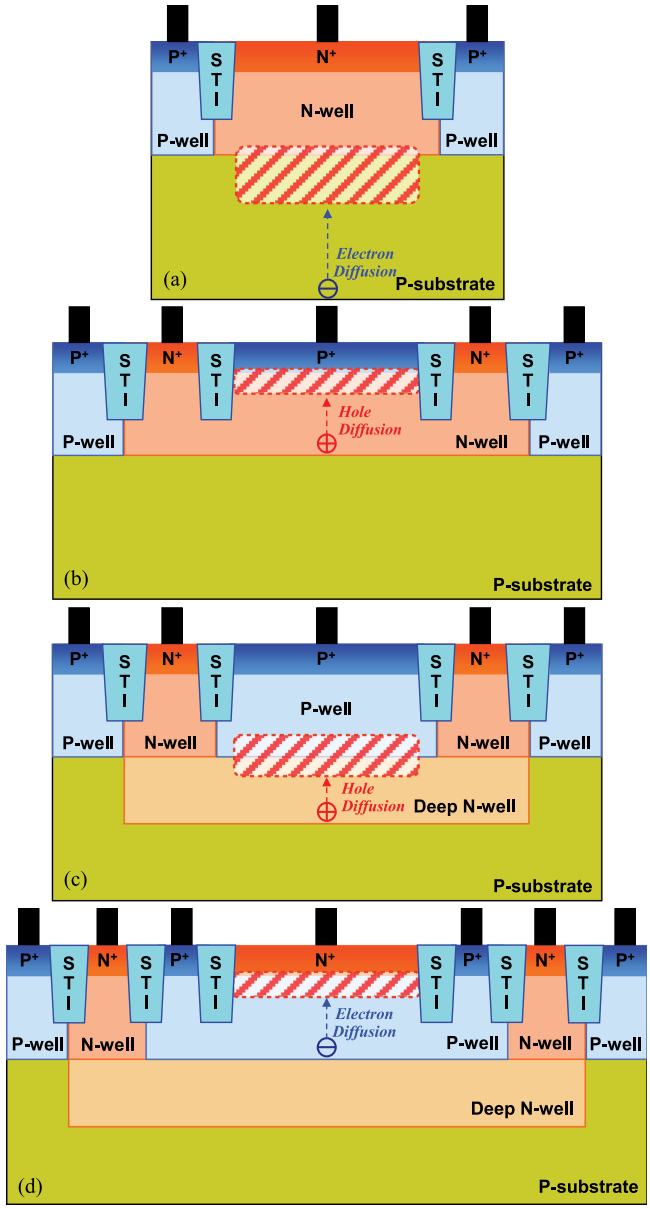

Fig. 5. Cross sections of CMOS-APDs: (a) N-well/P-substrate, (b) P^+/N-well, (c) P-well/DNW, and (d) N^+/P-well CMOS-APDs.

III. DESIGN CONSIDERATIONS AND DISCUSSIONS

In order to identify the factors that influence the CMOS-APD performance and achieve the optimal CMOS-APD performance, several design considerations are investigated, including PN junction, GR, active area, and back end.

A. PN Junction

The simplest way of realizing a CMOS-APD in standard CMOS technology is using N-well/P-substrate junction as shown in Fig. 5(a). It has an advantage of wider depletion regions, enabling better responsivity than any other PN junctions available in standard CMOS technology. However, it is virtually impossible to realize a GR structure at the edge of the junction so that it has a disadvantage of premature edge

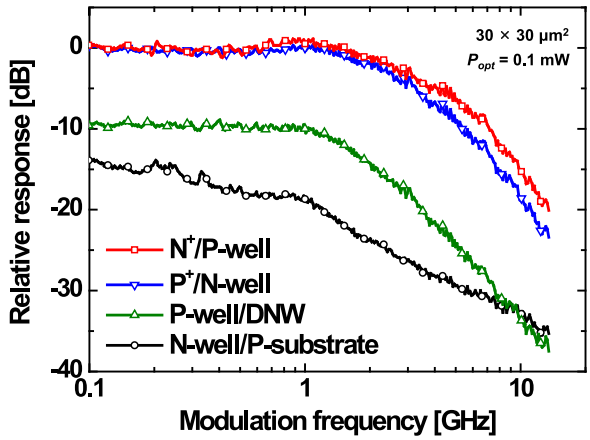

Fig. 6. Relative photodetection frequency responses of CMOS-APDs realized with different PN junctions.

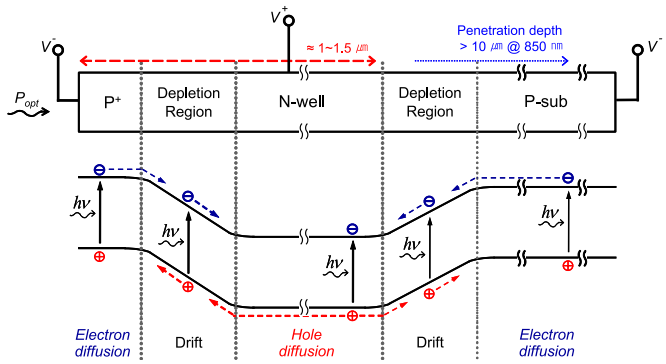

Fig. 7. Simplified band diagrams for P^+/N-well CMOS-APDs.

breakdown which results in low avalanche gain. Furthermore, this type of CMOS-APD has very small photodetection bandwidth in the MHz range, because many photons are absorbed in the charge-neutral P-substrate region where no electric field exists and photogenerated carriers reach the electrode by slow diffusion process. Therefore it shows worse performance than other types in terms of both responsivity and photodetection bandwidth as shown in Fig. 6. In contrast, CMOS-APDs based on P^+/N-well junction show much higher responsivity and larger photodetection bandwidth, because it has larger avalanche gain achieved by a GR structure provided by the shallow trench isolation (STI) as shown in Fig. 5(b) and the smaller charge-neutral region inside N-well. Fig. 7 shows a simplified band diagram where the electron diffusion in the P-substrate and the hole diffusion in the N-well can be observed.

If deep N-well (DNW) or buried N-well is available that can isolate the P-well region from the P-substrate, CMOS-APDs based on the P-well/DNW and N^+/P-well junctions are possible as shown in Fig. 5(c) and (d), in which the influence of the P-substrate can be excluded using the DNW. As can be seen in Fig. 6, the P-well/DNW CMOS-APD shows better photodetection bandwidth than the N-well/P-substrate CMOS-APD because the contribution of slow diffusion photogenerated carriers in the P-substrate region is excluded. Its responsivity is less than that of the P^+/N-well CMOS-APD since it does not have a GR structure at the edge of the junction. The N^+/P-well

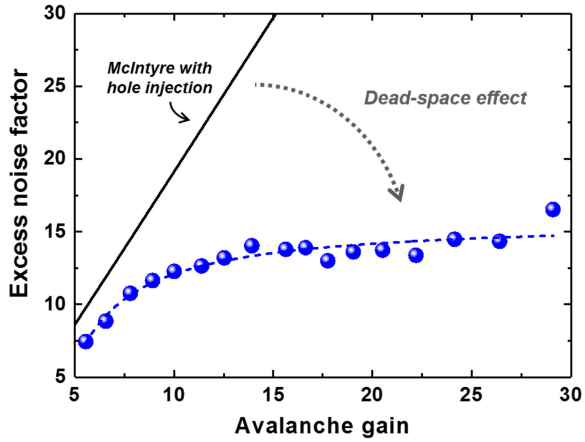

Fig. 8. Excess noise factor of a P^+/N-well CMOS-APD as a function of avalanche gain. The solid line indicates the prediction of McIntyre' model in the case of hole injection.

CMOS-APD achieves high responsivity just like the P^+/N-well CMOS-APD, and moreover it provides larger photodetection bandwidth than the P^+/N-well CMOS-APD, because electrons move faster in P-well than holes in N-well.

Fig. 8 shows the excess noise factor of the P^+/N-well CMOS-APD at the wavelength of 850 nm with McIntyre's model with hole injection, which is the case for the CMOS-APD since the avalanche process of the device is mostly based on hole-initiated multiplication at the long wavelength. It is notable that the noise factor for the CMOS-APD is much smaller than that with McIntyre's model. This is due to the dead space, the minimum distance a newly generated carrier must travel to gain sufficient energy for impact ionization. In standard deep-submicron CMOS technology, the multiplication region is quite narrow due to high doping concentrations so that the excess noise factor is greatly influenced by the dead-space effect [40], [44]. With the smaller excess noise, the P^+/N-well CMOS-APD has good signal-to-noise ratio [45], which enables high-performance CMOS optical receivers with reasonable sensitivity for optical interconnection applications [46] and also should be advantageous for many applications. Since the electron ionization rate is much higher than the hole ionization rate in silicon, the excess noise factor with electron injection is significantly lower than that with hole injection in CMOS-APDs, and therefore, in order to achieve lower avalanche multiplication noise than that of the P^+/N-well CMOS-APD, it is preferable to use the N^+/P-well junction, in which the avalanche multiplication process is mostly initiated by an electron.

In consideration of the depth of the junctions and optical penetration depth, the performance of the CMOS-APDs at 850 nm shown in Fig. 6 can be greatly improved at shorter wavelength in both responsivity and photodetection bandwidth due to higher quantum efficiency and less diffusion effect, respectively. For example, the peak responsivity occurs at around 500 nm with shallow junctions, because the penetration depth for 500 nm wavelength is about 1 μm while the N-well and P-well depths are around 1 um and between 550 and 800 nm for deeper junctions [44].

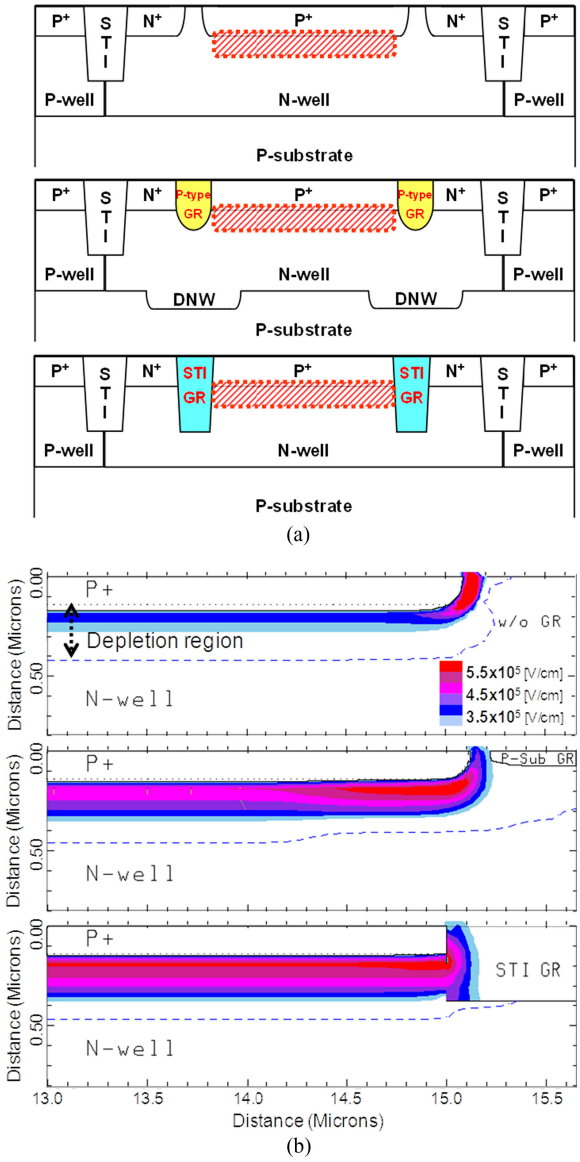

Fig. 9. (a) Cross sections and (b) simulated electric-field profiles of CMOS-APDs: (i) w/o GR, (ii) w/ P-type GR, and (iii) w/ STI GR [38].

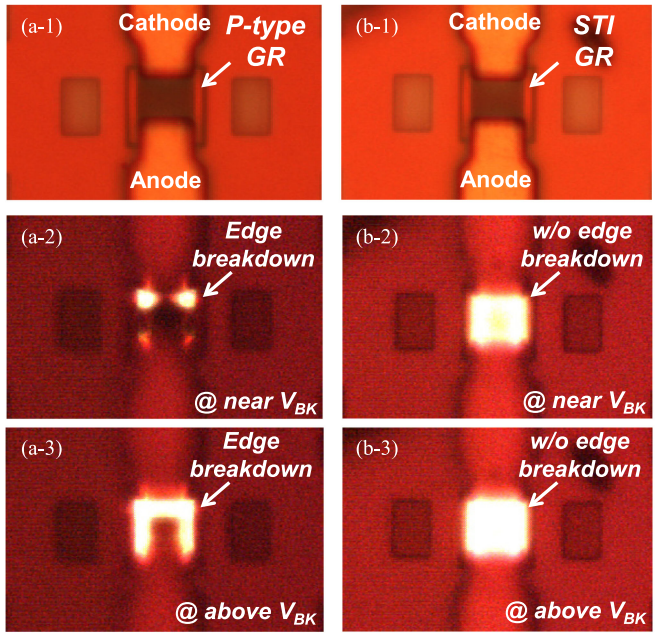

Fig. 10. Light emission tests of the fabricated CMOS-APDs: (a) w/ P-sub GR and (b) w/ STI.

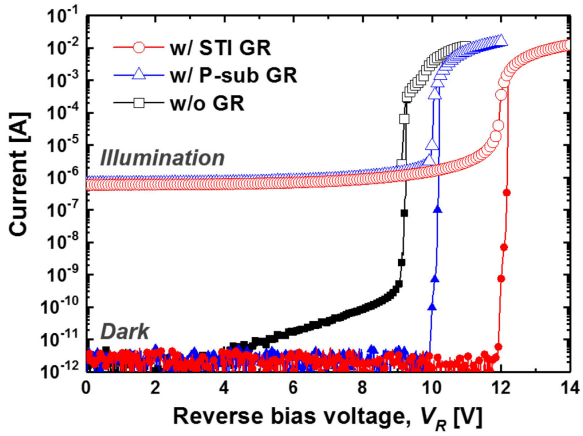

Fig. 11. Current-voltage characteristics of the CMOS-APDs under dark and illumination conditions: (i) w/o GR, (ii) w/ P-sub GR, and (iii) w/ STI GR [38].

B. Guard Ring

CMOS-APDs can suffer from premature breakdown at the junction edge due to locally concentrated electric fields. Therefore, they must have a GR structure with which high electric fields can be uniformly spread over the planar junction. Fig. 9(a) shows P^+/N-well CMOS-APDs (i) without GR, (ii) with a P-type GR, which can be formed by lateral diffusion of two closely spaced N-well regions or DNW, and (iii) with a GR formed by STI, which is used in standard CMOS technology for device isolation by depositing silicon dioxide into the shallow trench [38]. Fig. 9(b) shows simulated electric-field profiles using TCAD. Without any GR, the electric field is much stronger at the edge of the junction than at the planar junction, resulting in premature breakdown at the junction edge, which prevents photogenerated carriers to experience sufficient avalanche gain. With GRs, however, this premature edge breakdown is alleviated, enabling higher electric fields at the planar junction.

Such results also can be directly observed from CMOS-APDs' light emissions. Fig. 10 shows micrographs of the fabricated CMOS-APDs with (a) P-sub GR and (b) STI GR at near and above their breakdown voltages. These figures clearly show that electric fields are uniform over the planar junction with STI GR while premature edge breakdown occurs with P-sub GR. Fig. 11 shows measured current-voltage characteristics of CMOS-APDs under dark and illumination conditions. The increased dark current for the CMOS-APD without GR is due to tunneling at the edges of P^+ regions within N-well since these lateral edges have significantly steep doping profile gradients. For CMOS-APDs with P-sub GR and STI GR, all P^+ and N^+ regions are surrounded by lightly-doped P-sub or STI, which suppresses tunneling at the edges and results in lower dark

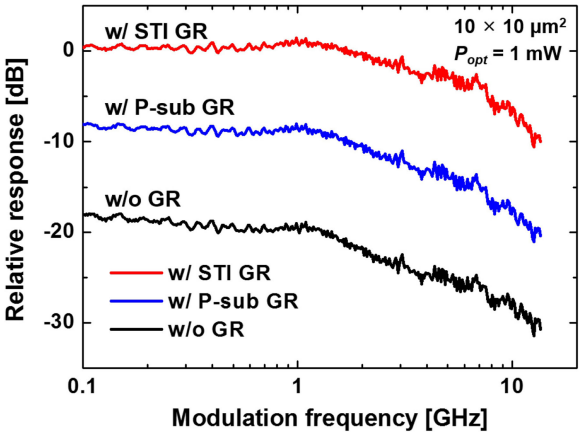

Fig. 12. Measured photodetection frequency responses of the fabricated CMOS-APDs without GR, with P-sub GR, and with STI GR [38].

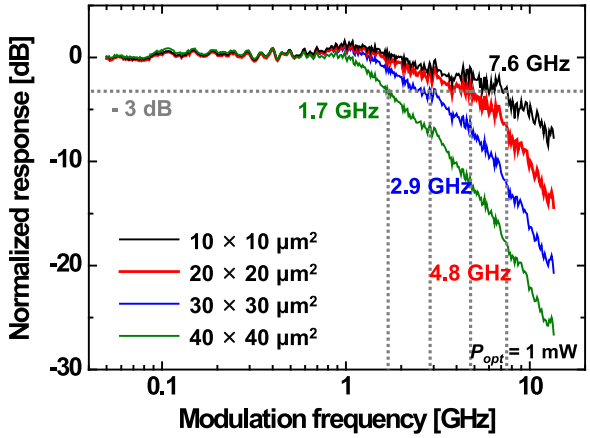

Fig. 13. Normalized photodetection frequency responses of CMOS-APDs having different device areas [39].

currents down to the detection limit of about 5 pA. The avalanche breakdown voltage is about 9.25 V without GR, but it increases to about 10.2 V for P-sub GR and 12.2 V for STI GR. With the higher breakdown voltage, STI GR allows the highest electric field before breakdown, resulting in the highest responsivity with the largest avalanche gain as shown in Fig. 12. Using the values of the depletion width and maximum electric field for each case obtained from the simulations shown in Fig. 9(b), the avalanche gain of the CMOS-APDs can be estimated with the ionization rate, which match well with the measurement results [38].

If retrograde well is available in a CMOS technology, a virtual GR structure can be implemented. Although it shows good performance for Geiger-mode APDs in terms of low dark count rates [47], it has not been demonstrated for CMOS-APDs yet. Its performance can be highly dependent on the retrograde profile, which is hard to control. Nevertheless, it can be useful for CMOS-APDs based on the P-well/DNW junction for which the STI GR is not available.

C. Active Area

It is very important to consider CMOS-APD's active area as a design parameter because it decides the device capacitance as well as the lateral diffusion path. Fig. 13 shows measured photodetection frequency responses of the fabricated P^+/N-well CMOS-APDs having different active areas of 10 × 10, 20 × 20, 30 × 30, and 40 × 40 μm^2. It clearly shows that smaller devices provide larger photodetection bandwidth, reaching 7.6 GHz for 10 × 10 μm^2 CMOS-APD [39].

The photodetection frequency response of the CMOS-APD is influenced by following factors: (i) transit time of photogenerated carriers, (ii) device RC time constant, (iii) inductive-peaking effect, and (iv) parasitics. From the analysis based on the CMOS-APD equivalent circuit model, the photodetection frequency responses due to selected factors can be simulated, and those factors that limit the photodetection bandwidth can be identified. Determination of parameter values for the equivalent circuit model is done by matching simulation results to measured S-parameter and photodetection frequency response

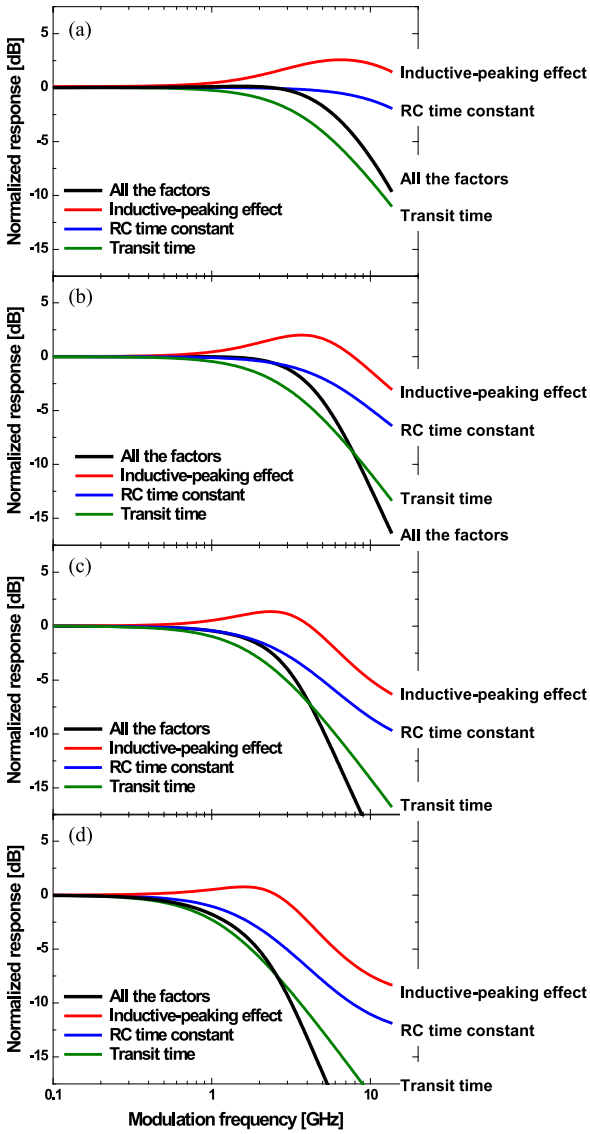

Fig. 14. Normalized photodetection frequency responses of CMOS-APDs for the photogenerated-carrier transit time, the RC time constant, the inductive-peaking effect, and all the factors according to device areas [39]. (a) 10 × 10 μm^2, (b) 20 × 20 μm^2, (c) 30 × 30 μm^2 and (d) 40 × 40 μm^2.

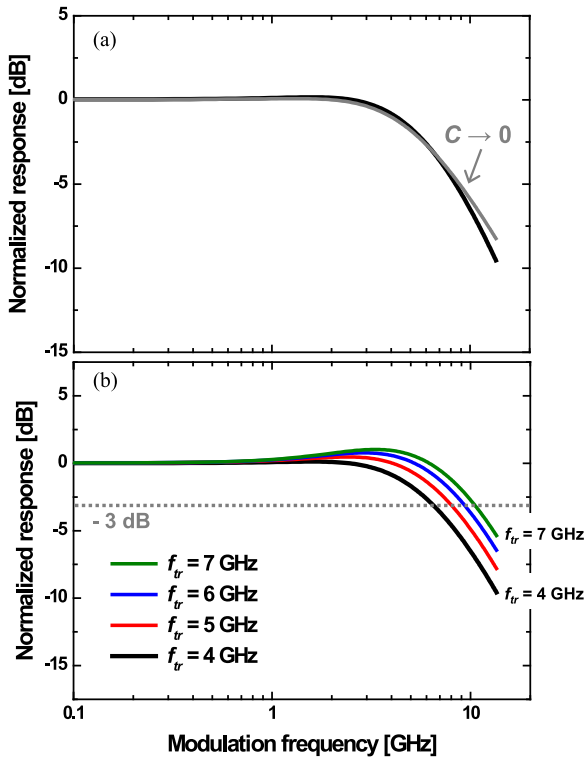

Fig. 15. Normalized photodetection frequency responses of the $10 \times 10\,\mu\text{m}^2$ CMOS-APD (a) with minimization of capacitance and (b) with increasing f_{tr}.

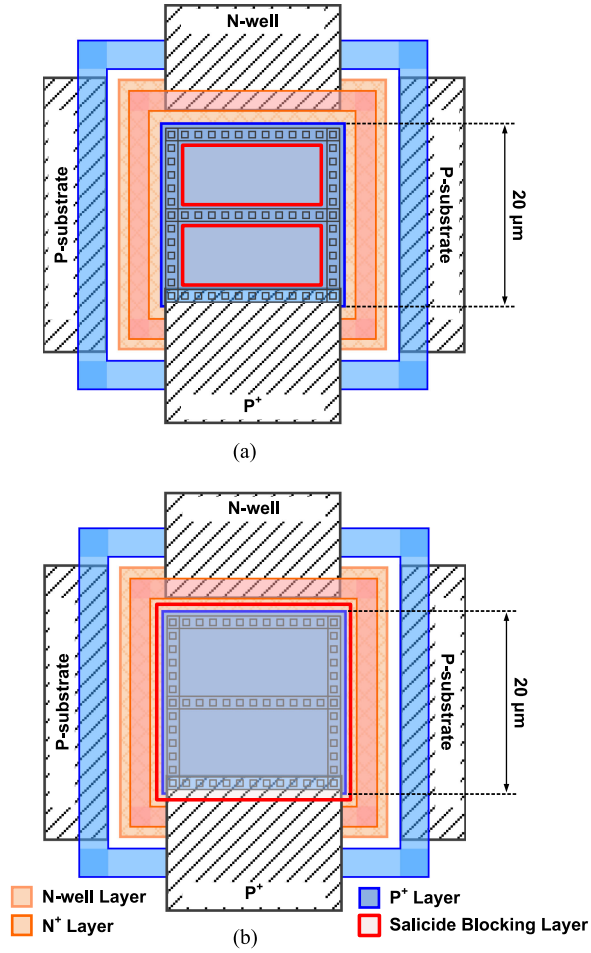

Fig. 16. Simplified P^+/N-well CMOS-APD layouts (a) with silicide and (b) without silicide [42].

measurement results as shown in Fig. 4 and Table I as described in Section II-B. Fig. 14 shows simulated photodetection frequency responses for the four different devices. For each type of device, four different simulation results are shown: one that considers only the photogenerated-carrier transit time (not including L_a, R_a, R_l, C, R_{nw}, C_{sub}, C_p, and R_p), another that considers only the RC time constant (not including f_{tr} in the current source as well as L_a and R_a), third that considers the inductive-peaking effect (not including f_{tr} in the current source), and fourth that includes all the factors. As can be observed from these figures, the photogenerated-carrier transit time is the dominant bandwidth-limiting factor for CMOS-APDs, because holes photogenerated in the charge-neutral N-well must transport by the slow diffusion process. Even with this limitation, however, higher total bandwidth can be achieved in the CMOS-APDs, because inductive peaking provides high-frequency boosting. With the inductive-peaking effect at 6.5 GHz, the $10 \times 10\,\mu\text{m}^2$ CMOS-APD achieves 7.6-GHz photodetection bandwidth while its f_{tr} is 4 GHz.

Since smaller devices have smaller transit time and higher inductive-peaking frequency with smaller capacitance, they achieve larger photodetection bandwidth. By further reducing the active area smaller than $10 \times 10\,\mu\text{m}^2$, the photodetection bandwidth of the CMOS-APD can be enhanced with the decreased transit time as shown in Fig. 15, which shows estimated results using the equivalent circuit model with minimizing the device capacitance and decreasing the device transit time (i.e., increasing f_{tr}). However, it is expected that the bandwidth enhancement with shrinking the area further is ultimately limited by the high parasitic resistance because the number of contacts and vias in the output electrode may not be sufficient. In addition, with shrinking the area, the optical coupling loss can increase due to the area occupied by electrodes.

D. Back End

Although the back-end design for silicides, contacts, and electrodes can affect the CMOS-APD performance as much as other parameters, there have been almost no studies focusing on this. For the injection of optical signals into the CMOS-APD, optical window is formed by blocking the self-aligned silicide (salicide) process during the fabrication process. Fig. 16 shows two different back-end designs using the salicide blocking layer (i) only for the optical-window area but not for the electrodes (i.e., with silicide) and (ii) for all the optical-window area (i.e., without silicide). As can be seen in Fig. 17, the measured photodetection frequency responses clearly show that the CMOS-APD with silicide has higher responsivity and 63% higher photodetection bandwidth as well [42]. The higher responsivity is due to the fact that the parasitic resistance of the CMOS-APD with silicide is negligible while the CMOS-APD without silicide has a non-negligible parasitic resistance which causes a voltage drop and

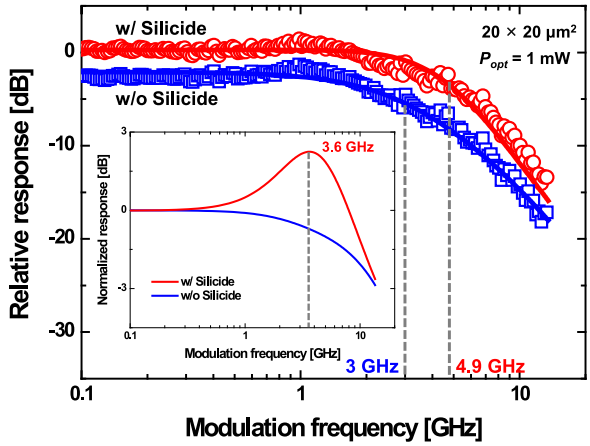

Fig. 17. Measured and simulated photodetection frequency responses of CMOS-APDs with and without silicide. Hollow circles represent measured data and solid lines simulated results with the equivalent circuit model. The inset shows normalized photodetection frequency responses of CMOS-APDs without the photogenerated-carrier transit time [42].

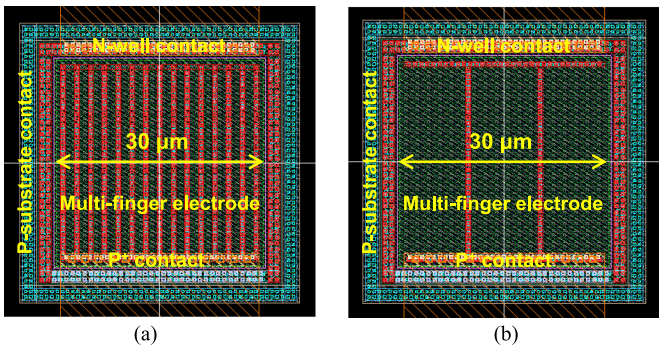

Fig. 18. Simplified CMOS-APD layouts with (a) 1.3 μm and (b) 9.6 μm spacing multi-finger electrodes on 30 × 30 μm^2 optical windows.

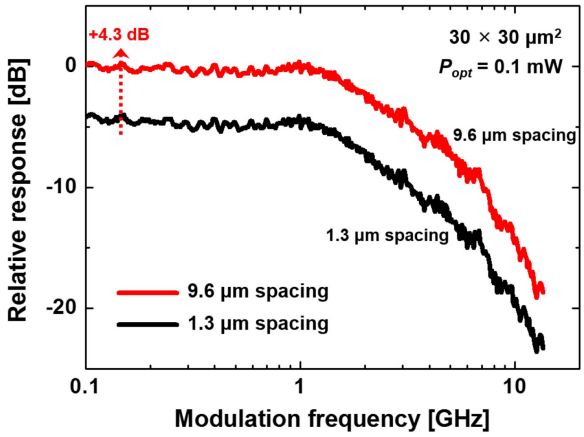

Fig. 19. Measured photodetection frequency responses of CMOS-APDs having (a) 1.3 μm and (b) 9.6 μm spacing multi-finger electrodes on optical windows.

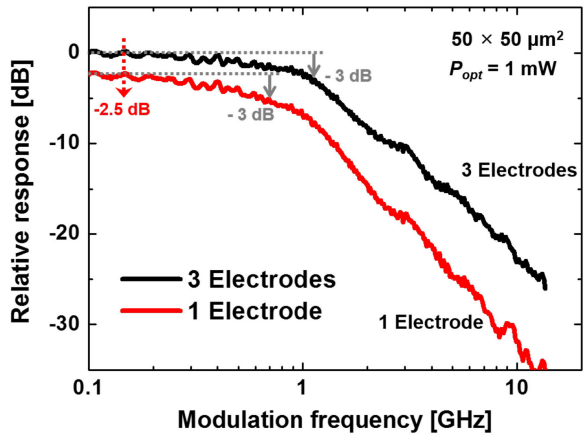

Fig. 20. Measured photodetection frequency responses of CMOS-APDs having (a) three electrodes and (b) only one electrode on optical windows.

eventually lower avalanche gain and responsivity. The bandwidth difference can be identified with the equivalent circuit simulation in a similar manner done in Section III-C. Without silicide the parasitic resistance is increased from 0 to 30 Ω, deactivating the inductive peaking effect [42], while the CMOS-APD with silicide shows clear inductive peaking at 3.6 GHz as shown in the inset of Fig. 17. These show that the parasitic resistance introduced by the back-end process has great effects on both the gain and photodetection bandwidth of CMOS-APDs.

Electrode structures on the optical window should be also considered. For effective collection of the photogenerated carriers, multi-finger electrodes can be considered in CMOS-APDs. Fig. 18 shows simplified layouts of CMOS-APDs based on the P$^+$/N-well junction. Multi-finger electrodes shown in Fig. 18(a) reduce the lateral transit time of photogenerated carriers as well as the parasitic resistance, although optical coupling efficiency can be reduced due to the narrow multi-finger spacing. Fig. 19 shows measured photodetection frequency responses for the CMOS-APDs having 1.3 μm and 9.6 μm spacing for multi-finger electrodes on their optical windows. The response for the CMOS-APD with 9.6 μm spacing is about 4.3 dB higher without photodetection bandwidth degradation, because the larger finger spacing (i.e., a few electrodes on the optical window) gives better responsivity for the CMOS-APD due to better optical injection. There is no degradation of the photodetection-bandwidth performance because the increased lateral transit time in the P$^+$ region has little influence on the bandwidth performance since the dominant bandwidth-limiting factor is the hole diffusion time in N-well. However, it should be noted that there is a lower limit of the number of electrodes and contacts as shown in Fig. 20, which are obtained from other CMOS-APD samples having larger active area fabricated in a different technology. If the number of contacts, vias, and electrodes are not sufficient, the parasitic resistance increases, degrading both responsivity and photodetection bandwidth.

Since standard CMOS technology is not optimized for optical devices, APDs as well as photodiodes suffer from coupling loss due to light reflection and refraction at the boundaries of the dielectric stack. Therefore, they have wavelength-dependent characteristics and lower responsivity [48], [49]. Unfortunately, any modifications and/or custom designs of the dielectric layers are not allowed in standard CMOS technology. In order to alleviate the effect and increase the responsivity, two approaches can be considered: (i) using a CMOS image sensor process or

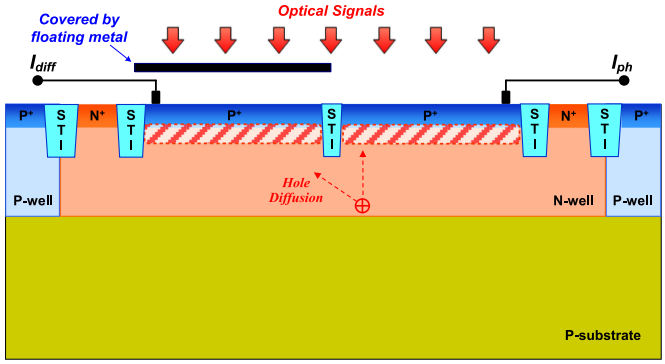

Fig. 21. Cross section of SM-APDs based on the P^+/N-well junction [43].

CMOS-Opto process offering anti-reflection coatings (ARCs) and (ii) removing the entire stack layers on the optical window of the CMOS-APD and depositing an ARC through custom process steps.

IV. Performance Improvement Techniques

In this section we present techniques that can further enhance CMOS-APD photodetection bandwidth, responsivity, and spectrum.

A. Spatial-Modulation Technique

CMOS-APDs based on P^+/N-well and N^+/P-well junctions to exclude the slow diffusion currents from the P-substrate region provide large photodetection bandwidth in the GHz range along with high responsivity by a GR, but the photodetection bandwidths of the CMOS-APDs are still limited by the diffusion process in the charge-neutral regions inside the well. The simplest way to reduce the hole transit time is reducing well thickness, but this is not possible with the standard CMOS technology. Instead, a spatial-modulation technique can be used in which photocurrents due to diffusion can be eliminated at the device output. Fig. 21 shows a spatially-modulated CMOS-APD (SM-APD) based on the P^+/N-well junction. The active area is divided into two regions with one region covered by a floating metal to block the incident light. In this blocked region, there are hole diffusion currents, I_{diff}, coming from the uncovered region. By subtracting I_{diff} from I_{ph}, photocurrents from the uncovered region, the slow diffusion components in the I_{ph} can be excluded, enabling larger photodetection bandwidth. A differential-type transimpedance amplifier (TIA) can easily function as the subtractor for the SM-APD without increasing circuit complexity.

Fig. 22(a) shows measured photodetection frequency responses of the fabricated $5 \times 5\ \mu m^2$ CMOS-APD and SM-APD [43]. I_{ph} shows about 6-dB lower response than the CMOS-APD because of the light-blocking metal. I_{diff} shows much smaller response and photodetection bandwidth than the I_{ph} because that is composed of diffused photocurrents from the uncovered region. By subtracting I_{diff} from I_{ph}, the SM-APD achieves larger photodetection bandwidth than the CMOS-APD as shown in Fig. 22(b), because the bandwidth-limiting diffusion components are partially removed.

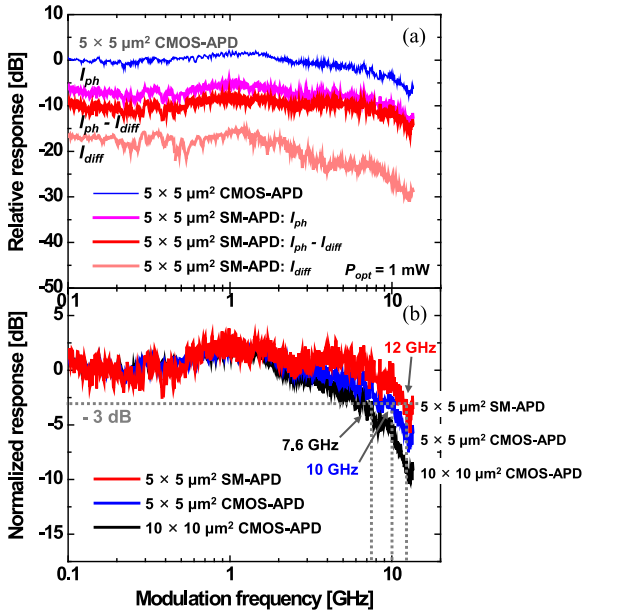

Fig. 22. (a) Measured photodetection frequency responses of the $5 \times 5\ \mu m^2$ CMOS-APD and SM-APD. (b) Normalized photodetection frequency responses of the APDs [43].

For this SM-APD, there are one covered and one uncovered regions so that optical coupling loss can be minimized. SM-APDs can have more segments, which can further enhance photodetection bandwidth with more efficient reduction of the slow diffusion components, although the coupling loss increases due to redundant STI areas between segments.

B. Carrier-Acceleration Technique

Another way to reduce the effect of the slow diffusion process is using a carrier-acceleration technique. In case of the P^+/N-well CMOS-APD, by applying bias voltages between two different N-well ports, an electric field is produced inside the charge-neutral N-well region, which accelerates photogenerated holes, resulting in the enhanced photodetection bandwidth. Fig. 23(a) shows a movement of a hole photogenerated in the charge-neutral N-well region with the extrinsic electric field. Fig. 23(b) and (c) are TCAD simulation results [41], which clearly show that high electric fields larger than 5×10^5 V/ cm are produced all over the junction as well as the lateral electric field inside the N-well region. Measured photodetection frequency responses at three different bias voltages applied to N-well are shown in Fig. 24. The photodetection response decreases with the increasing bias voltage applied to N-well, because the electric field near NW2 port decreases as shown in Fig. 23(b), but at the same time the photodetection bandwidth increases by the electric field inside N-well as shown in Fig. 24(b).

This technique, however, has two limitations. One is the forward threshold voltage of the N-well/P-substrate junction, which can be reached if the NW2 bias voltage is too large. With NW2 bias voltage of -1.0 V, it does not exceed the forward threshold voltage due to the distance between the junc-

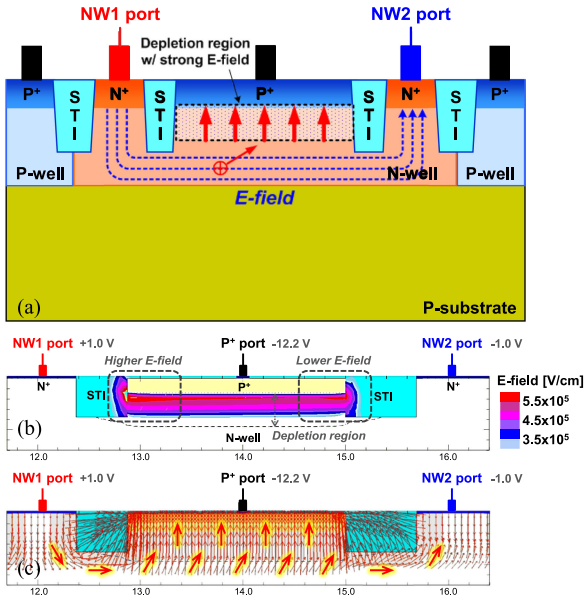

Fig. 23. (a) Movement of photogenerated carriers in N-well with an extrinsic electric field inside the charge-neutral N-well region. (b) Simulated electric field profile and (c) electric field lines of the CMOS-APD. 1.0 V and −1.0 V bias voltages are applied to NW1 and NW2 ports, respectively, at the reverse bias voltage of 12.2 V for the P^+/N-well junction [41].

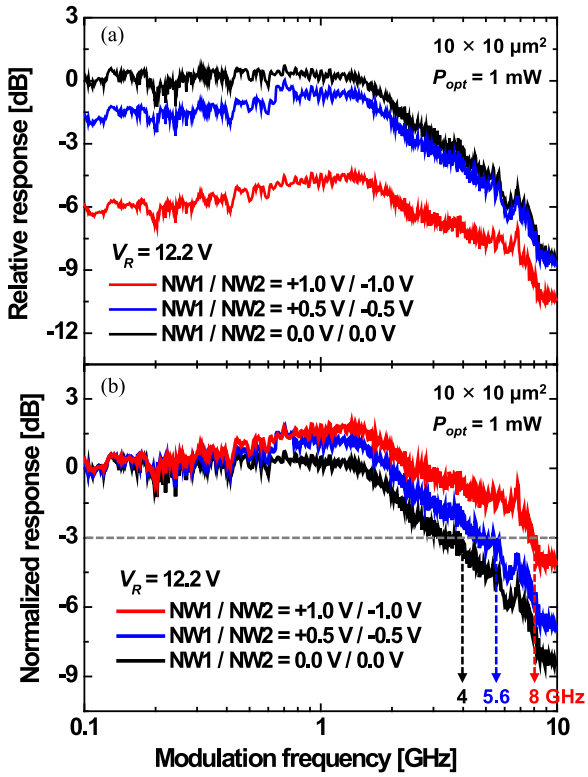

Fig. 24. (a) Relative and (b) normalized photodetection frequency responses of the CMOS-APD with different bias voltages applied to N-well [41].

tion and the NW2 port, but it cannot operate with NW2 bias voltage above −1.0 V. The other is the increased dark current with earlier breakdown. As shown in the TCAD simulation results, the P^+/N-well junction near the NW1 port has higher electric fields so that the avalanche breakdown occurs earlier with the increasing NW1 bias voltage. With NW1 bias voltage of 1.0 V, large dark currents are produced [41]. However, it is remarkable that with NW1 bias voltage of 0.5 V, where the device does not suffer from the high dark current, the CMOS-APD achieves 40% bandwidth enhancement with just 15% loss in responsivity as shown in Fig. 24.

C. Multi-Junction Technique

The multi-junction technique can be implemented with lateral multi junctions or vertical multi junctions. The lateral multi-junction technique has been applied for several different types of CMOS-APDs [29]–[32], [41], as it can reduce lateral diffusion time of photogenerated carriers. In addition, this technique can increase the effect of carrier acceleration because shorter spacing between NW1 and NW2 ensures a larger electric field inside the charge-neutral N-well region. However, this technique causes higher optical coupling loss due to redundancy areas between junctions. Fig. 25 shows lateral multi-junction and vertical multi-junction CMOS-APD structures. The vertical multi-junction technique is implemented with two or more vertical junctions. The CMOS-APD with vertical multi junctions has lower photodetection bandwidth due to the increase of slow diffusion components from several charge-neutral regions. The advantage of this technique is that with several junctions at different depths the device can cover wide spectrum range including blue, green, and red light, and therefore it can be used

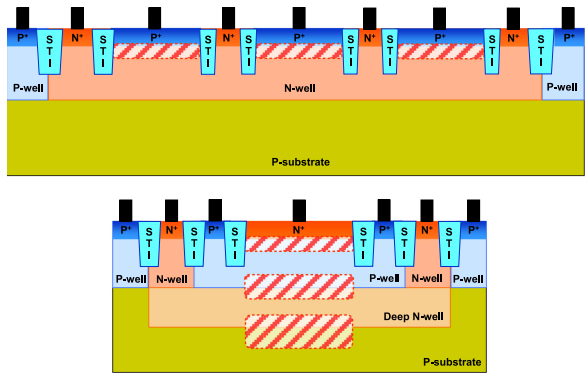

Fig. 25. Cross sections of (a) lateral and (b) vertical multi-junction CMOS-APDs.

for color-sensitive sensor applications such as vision sensors [50], [51], lab-on-a-chip and biosensor [24]. In addition, it can be also used for improving photodetection bandwidth of the main junction by extending the depletion width of the below junction, resulting in the reduction of the charge-neutral region for the main junction [33].

V. Summary and Conclusion

Table II compares structures and performances of CMOS-APDs reported in recent publications. It shows that the state-of-the-art CMOS-APDs are based on P^+/N-well or N^+/P-well (P-substrate) with DNW in which slow diffusion photogenerated carriers from P-substrate are blocked and the

TABLE II
COMPARISON OF STATE-OF-THE-ART SILICON APDS FABRICATED IN STANDARD CMOS TECHNOLOGY

	[31]	[32]	[33]	[39]	[41]	[43]	
Technology	0.18 μm CMOS	0.18 μm CMOS	40 nm CMOS	0.13 μm CMOS	0.25 μm CMOS	0.13 μm CMOS	
PN Junction	N^+/P-sub	N^+/P-well	P^+/N-well/P-sub	P^+/N-well	P^+/N-well	P^+/N-well	
GR	STI	STI	STI	STI	STI	STI	
Area (Shape)	50 × 50 μm² (Octagon)	10 × 10 μm² (Square)	70 × 70 μm² (Square)	10 × 10 μm² (Square)	10 × 10 μm² (Square)	5 × 5 μm² (Square)	
Technique	Lateral multi junction (isolated by DNW)	Lateral multi junction (isolated by DNW)	Vertical multi junction	–	Lateral multi junction and carrier acceleration	–	Spatial modulation
Optical Power (Wavelength)	380 μW (823 nm)	20 μW (830 nm)	127 μW (850 nm)	1 mW (850 nm)	1 mW (850 nm)	1 mW (850 nm)	1 mW (850 nm)
Bias Voltage	11.4 V	8.3 V	8.41 V	10.25 V	12.2 V	10.0 V	9.7 V
Gain	–	10	11	15.4	16.7	28.4	10.6
Responsivity	0.018 A/W	0.05 A/W	0.84 A/W	0.48 A/W	0.2 A/W	0.35 A/W	0.03 A/W
Bandwidth	8.7 GHz	10 GHz	0.7 GHz	7.6 GHz	5.6 GHz	10 GHz	12 GHz

most effective GR structure, STI, can be used. Many of them use the lateral multi-junction technique for improving the photodetection bandwidth performance, and the device with the vertical multi-junction technique shows high responsivity but low photodetection bandwidth. The CMOS-APD having smaller active area of $5 \times 5\,\mu m^2$ achieves larger photodetection bandwidth along with high responsivity, and with using the spatial-modulation technique 12 GHz bandwidth is achieved, which is the largest bandwidth ever reported for silicon photodetectors in standard CMOS technology.

It is expected that higher photodetection bandwidth than 12 GHz is achieved along with better responsivity compared to the results achieved by the SM-APD [43], if the CMOS-APD is realized with the N^+/P-well junction with DNW, STI GR, small active area less than $5 \times 5\,\mu m^2$, lateral and vertical multi-junction technique, and carrier-acceleration technique in a feature size smaller than 0.13 μm. Fig. 26 shows the proposed CMOS-APD and estimated photodetection frequency responses with the equivalent circuit model. With the small active area, the dominant bandwidth-limiting factor is the diffusion time, and the extracted f_{tr} value for $5 \times 5\,\mu m^2$ P^+/N-well CMOS-APD is 5.5 GHz [43]. Using the N^+/P-well junction, electron diffusivity is about 2.3 times higher than hole diffusivity at doping concentration of about 10^{17} cm^{-3} [52], which corresponds to f_{tr} of 12.65 GHz, resulting in photodetection bandwidth of 18.4 GHz with the inductive-peaking effect. In addition, with the 1 V different bias voltage applied to P-well, electron drift velocity is about 2.4 times higher than hole drift velocity at the extrinsic electric field of about 3×10^3 V/ cm [52], and therefore about 40% f_{tr} improvement is also expected in the N^+/P-well junction with the carrier-acceleration technique similar to the P^+/N-well. Consequently, as shown in Fig. 26(b), it is estimated that the proposed CMOS-APD provides higher photodetection bandwidth over 23 GHz along with higher responsivity over 0.3 A/W. In addition, by applying a bias voltage to the DNW, the photodetection bandwidth can be further enhanced due to the reduction of the charge-neutral P-well region. Moreover, with the DNW biasing, since the P-well/DNW junction does not reach its forward threshold voltage, the bias voltage of the PW1 port can be increased above +1.0 V, enabling even higher bandwidth with the enhanced carrier-acceleration technique. Furthermore, this electron-injection type CMOS-APD reduces the excess noise of the device, enabling higher SNR and therefore higher-performance CMOS optical receivers having better sensitivity. The optimized high-speed and high-responsivity CMOS-APDs can play an important role in a wide spectrum of next-generation applications described in Section I by enabling monolithic electronic-photonic integrated circuits based on the mature CMOS technology.

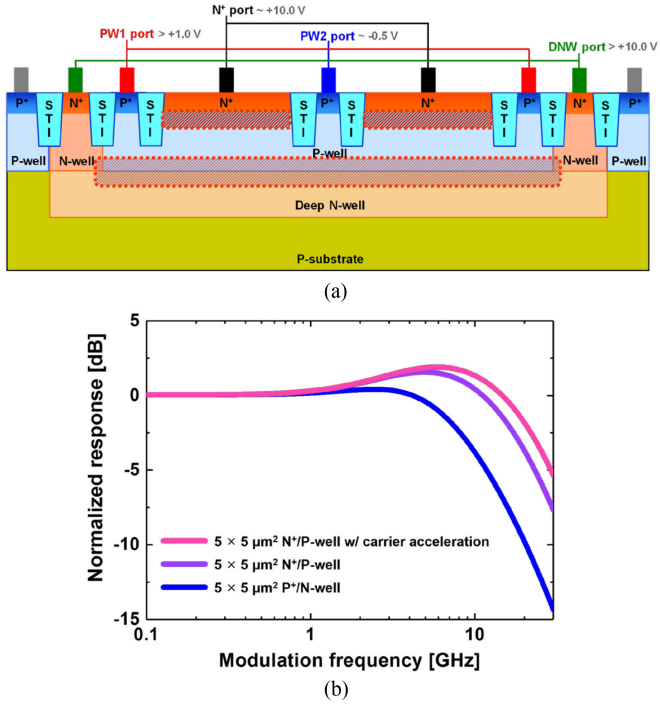

Fig. 26. (a) Proposed CMOS-APD based on the N^+/P-well junction with DNW and STI GR utilizing vertical multi-junction technique as well as lateral multi-junction and carrier-acceleration techniques. (b) Estimated photodetection frequency responses of proposed CMOS-APDs.

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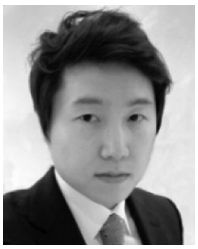

Myung-Jae Lee (S'08–M'13) received the B.S., M.S., and Ph.D. degrees in electrical and electronic engineering from Yonsei University, Seoul, South Korea, in 2006, 2008, and 2013, respectively. His doctoral dissertation concerned silicon avalanche photodetectors fabricated with standard CMOS/BiCMOS technology. From 2013 to 2017, he was a Postdoctoral Researcher at the Faculty of Electrical Engineering, Delft University of Technology, Delft, The Netherlands, where he worked on single-photon image sensors and applications based on single-photon avalanche diodes. In 2017, he joined the School of Engineering, École Polytechnique Fédérale de Lausanne, Neuchâtel, Switzerland, working on advanced single-photon image sensors and applications as well as coordinating and managing several research projects. His research interests include single-photon avalanche diodes, LiDAR sensors, biosensors, image sensors, CMOS- and BiCMOS-compatible photodetectors and receivers, avalanche photodetectors, silicon photonics, and optical interconnects.

Woo-Young Choi (M'92) received the B.S., M.S., and Ph.D. degrees in electrical engineering and computer science from the Massachusetts Institute of Technology, Cambridge, MA, USA, in 1986, 1988, and 1994, respectively. His doctoral dissertation concerned the investigation of molecular-beam epitaxy-grown InGaAlAs laser diodes for fiber-optic applications. From 1994 to 1995, he was a Postdoctoral Research Fellow at NTT Opto-Electronics Laboratories, where he worked on femtosecond all-optical switching devices based on low-temperature grown InGaAlAs quantum wells. In 1995, he joined the Department of Electrical and Electronic Engineering, Yonsei University, Seoul, South Korea, where he is currently a Professor. His research interests include the area of high-speed circuits and systems that include high-speed optoelectronics, high-speed electronic circuits, and silicon photonics.