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"Over the Barrier, Toward the Next"

공지사항
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FAQ
자주 묻는 질문과 답변
1. 소규모 보조 영역이 있습니까?
2. 사전 등록 및 참가자 가이드라인?
<table>
<thead>
<tr>
<th>Session</th>
<th>Time</th>
<th>Title</th>
<th>Authors</th>
<th>Institution</th>
</tr>
</thead>
<tbody>
<tr>
<td>TA2-L-1</td>
<td>10:40</td>
<td>A 1.2 V CMOS-based Temperature Sensor in the Subthreshold Operation</td>
<td>Woosul Shin, Jun-Seok Na, Bong-Choon Kwak, Seong-Kwan Hong, and Oh-Kyong Kwon</td>
<td>Department of Electronic Engineering, Hanyang University</td>
</tr>
<tr>
<td>TA2-L-2</td>
<td>10:55</td>
<td>SIDO DC-DC 컨버터의 부하 범위 확장을 위한 cross regulation 감쇠 방법</td>
<td>정현수, 흥호천, 김승목, 백광현</td>
<td>Chung-Ang University</td>
</tr>
<tr>
<td>TA2-L-3</td>
<td>11:10</td>
<td>Fast-transient Output-capacitorless LDO Regulator for SoC Applications</td>
<td>Eun-Taek Sung, Jeong-Yun Lee, Keum-Won Ha, Ye-Seul Baek, and Donghyun Baek</td>
<td>School of Electrical Engineering, Chung-Ang University</td>
</tr>
<tr>
<td>TA2-L-5</td>
<td>11:40</td>
<td>Design of a Transceiver Transmitting Power, Clock, and Data over a Single Optical Fiber for Future Automotive Network System</td>
<td>Woorham Bae and Deog-Kyoon Jeong</td>
<td>Department of Electrical and Computer Engineering, Seoul National University</td>
</tr>
<tr>
<td>TA2-L-6</td>
<td>11:55</td>
<td>A 3/6/12-Gb/s Multi-Rate Clock and Data Recovery Circuit with a Multi-Mode Rotational Bang-Bang Phase Detector</td>
<td>Ki-Hyun Pyun, Dae-Hyun Kwon, and Woo-Young Choi</td>
<td>Department of Electrical and Electronic Engineering, Yonsei University</td>
</tr>
</tbody>
</table>
A 3/6/12-Gb/s Multi-Rate Clock and Data Recovery Circuit with a Multi-Mode Rotational Bang-Bang Phase Detector

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For many serial data communication applications such as display interface, multi-rate operation is required. For this, clock and data recovery (CDR) circuits have to operate for several different data rates. Implementing CDRs with wide tuning-range VCOs is the most straight-forward approach, but it is very challenging to design a wide tuning-range VCO with constant VCO gain, which is required for CDR stability, over the required entire frequency band. We propose a new multi-rate CDR architecture based on a multi-mode rotational bang bang phase detector (MRBBPD), which can operate at 3, 6 and 12-Gbps. Fig. 1 shows the schematic of our CDR. The MRBBPD supports full-rate, half-rate, and quarter-rate phase detection operations enabling the multi-rate operation of the CDR without a wide tuning-range VCO. The MRBBPD is composed of eight DFFs, three rotational muxes, and two XOR gates and requires 8-phase clock signals from VCO. The rotational muxes produce different output signals depending whether it is in the full-rate, half-rate, or quarter-rate mode as shown in the timing diagram given in Fig. 1(b). Fig. 1(c) shows the 65-nm CMOS post-layout simulated eye-diagrams of the recovered data for 2^7-1 PRBS input data at three different data rates of 3Gb/s, 6Gb/s and 12Gb/s. Data recover is successfully done. Compared to conventional quarter-rate CDR, our CDR has less six XORs and three charge-pumps, which results in significant reduction of power consumption and area occupation.

Fig. 1. (a) Block diagram of MRBBPD (b) Timing diagram of Full/Half/Quarter-rate operation (c) Eye diagram of 3Gb/s (d) Eye diagram of 6Gb/s (e) Eye diagram of 12Gb/s