Multi-Rate Clock and Data Recovery Circuit with a Multi-Mode Rotational Bang-Bang Phase Detector and a Frequency Band Detector

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by

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Yonsei University

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Abstract

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A new type of multi-rate CDR circuit is realized that can operate at multiple data rates of 3.5-, 7.0- and 14.0-Gb/s. A multi-mode rotational bang-bang phase detector (MRBPD) supports full-rate, half-rate and quarter-rate phase detections to enable the multi-rate CDR operation with only one voltage-controlled oscillator. In addition, a new type of frequency band detector (FBD) is employed which selects the

appropriate mode of MRBPD for the correct data-rate without any external control signals. A prototype CDR circuit implemented in 65-nm CMOS technology successfully demonstrates the multi-rate operation. The circuit achieves the energy efficiency of 0.64 pJ/bit and has the chip size of 0.025 mm^2, both of which are much less than those of conventional multi-rate CDR circuits.

Keywords: Bang-Bang phase detector, clock and data recovery (CDR), frequency band detector, multi-rate operation.

1. Introduction

1.1. High-Speed Serial Interface

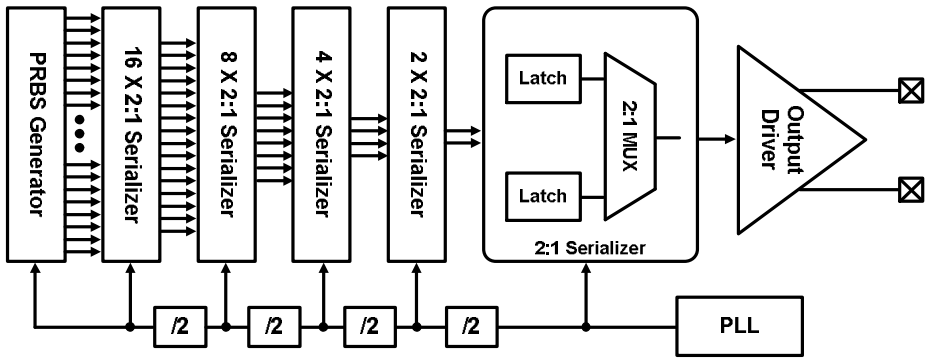
In display interface applications, the amount of data is rapidly increasing due to continuous demands for high resolutions, 3-D display, color depth, and frame rates. To transmit this greater data capacity and faster data, there are two ways. We can transmit either parallel or serial link. In the parallel method, each bit is transmitted through each wire and all data have to be transmitted at the same time. This method is implemented easily for high-speed transmission. However, a large number of I/O pins are necessary to satisfy the specifications of various applications by using parallel link method. The parallel data transmission can increase package cost due to large number of pins and multiple identical building block. In addition, this method can produce problems such as skew problem and crosstalk.

These problems mentioned in the parallel link method can be solved by using the serial link method. In the serial link method, all the parallel data are converted to serial data, and this serial data is transmitted by single lane. This serial link method widely uses in diverse applications such as USB (Universal Serial Bus), SATA (Serial

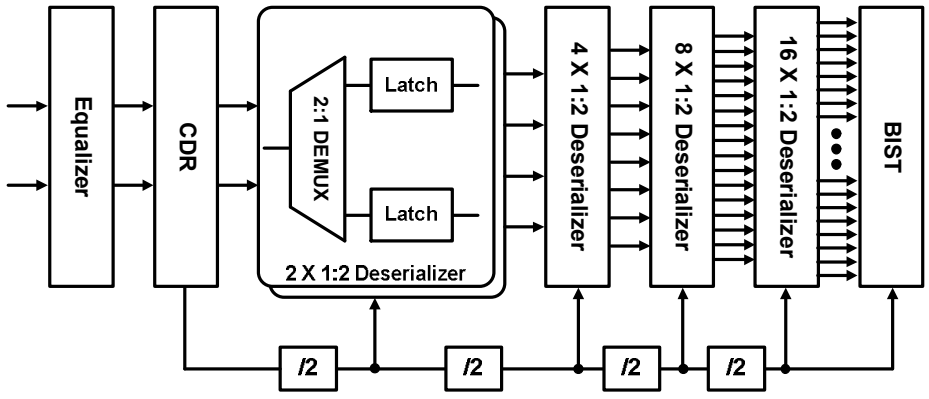
Advanced Technology Attachment), and HDMI (High-Definition Multimedia Interface). One of the great advantages in the serial link method is that they use fewer I/O pins and consequently can save board electrical connection, package legs, and connection pin. However, this method can have the design complexity because of data mixing and demuxing process for serial data transmissions.

Fig. 1.1 (a) shows the block diagram of conventional transmitter for serial interface. The transmitter consists of PRBS generator, serializer, frequency divider, output driver, and PLL. The transmitter needs low- jitter high frequency clock signals to make serial data stream. Therefore, the PLL is usually utilized to generate high frequency clock signals. This high frequency clock signals are used for frequency divider and last 2:1 MUX.

Fig. 1.1 (b) shows the block diagram of conventional receiver for serial interface. The receiver is composed of equalizer, clock and data recovery circuit (CDR), de-serializer, and frequency divider. The receiver has the problem to be limited bandwidth due to physical effect on channels and increasing transmitted data rate. To prevent the signal distortion, the equalizer compensating the characteristic of channel loss is used for the first stage of receiver. Since the clock is not mostly transmitted separately to save the channel and pad for external clock



(a)



(b)

Fig. 1-1. Block diagram of conventional (a) transmitter and (b) receiver

signal, clock information should be extracted from the transmitted input data stream. The CDR can extract the clock information from the input data stream. A precisely recovered clock suppresses the skew and jitter originated from a noisy input data stream, in other to achieve a low bit error rate (BER) of the CDR. Minimizing the timing error between the input data and the recovered clock is a critical design goal for the CDR, which determines the overall receiver system performance. The retimed data are de-serialized into parallel low-speed data, and then are transported. In conclusion the CDR circuit is the key in the receiver for high-speed serial interface.

1.2. Overview of the CDR Application

In serial links, the CDR circuit in the receiver is the important block. The goal of CDR circuit is generating synchronized clock signal by extracting the clock information from the received data, and then resampling the received data with the recovered clock which is generally the center of the received data. Fig. 1.2 (a) shows the function of the CDR in the data communication. The data is retimed by the recovered clock whose phase is controlled by the CDR. The block diagram of conventional CDR is shown in Fig. 1.2 (b). The CDR consists of a phase detector (PD), charge pump (CP), loop filter (LP), voltage controlled oscillator (VCO), and clock tree. The PD detects the phase difference between the incoming data and the clock generated by the VCO, and aligned the generated clock by feedback system. The PD is very important role to determine the direction of the feedback. If the PD can't produce precise phase difference information, the CDR circuit may become unlock condition and cannot generate clock signals synchronized with incoming data. In order to meet these demands, many CDRs have been researching by various groups [1]-[4]. The CDR performance is dependent on the phase detection method in PD. Thus, the many types of the PD have been studied for a long time.

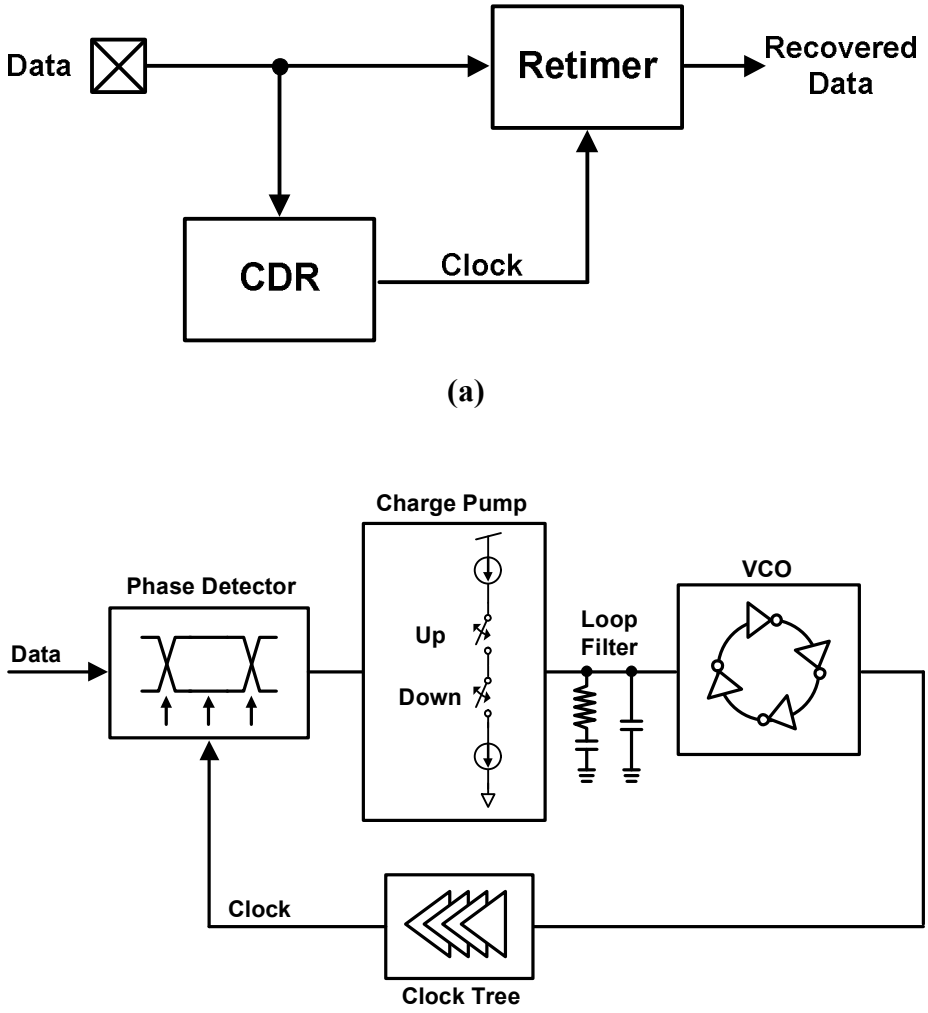


Fig. 1-2. (a) The function of the CDR (b) Block diagram of conventional CDR

1.3. Phase Detector

Requirements for a phase detector in a clock and data recovery (CDR) are described below. The input of CDR circuits is not a periodic signal but a random data. Therefore, phase detectors detect the phase error between the serial data and the recovered clock only when the serial data has transition. It is also preferred that the phase detector has no output when the serial data has no transition. Inherent sampling by the phase detector without another decision unit is also preferred since sampling the serial data by another decision unit causes a systematic timing offset from the setup and hold time variation of samplers.

Traditionally, linear phase detector and binary phase detector are commonly used in CDR application. Linear phase detector is called Hogge PD [5] and binary phase detector is called Bang-Bang (BBPD) [6]. Fig. 1.3 shows the structure and timing diagram of Hogge PD. The Hogge PD can extract the phase difference information between input data stream (Data) and VCO clock (CK). The Hogge PD makes the outputs (UP, DOWN) which have the amount of the phase error as well as the direction of the phase error. The outputs are compared with VCO clock which always has the width of the one period of the clock. Moreover, it is far from the metastability problem unlike the Bang-

Bang PD. In these reasons, the Hogge PD does not own the jitter inducing components, and accommodates the whole system for the linearity, which is rather easy for system analysis. However, the Hogge PD makes a narrow pulse width when the clock is near the optimal position. This narrow pulse width is difficult to deal with in high speed system. Hence, it is difficult to design for high speed CDR.

CDR circuits incorporating Bang-Bang PD (BBPD) have found wide usage in high speed applications due to the speed limitation of Hogge PD. Fig. 1.4 shows the structure and timing diagram of BBPD. The BBPD compares phase of the VCO clock to phase of the incoming data. If the clock is earlier than data, the BBPD makes the clock become slow in order to align phase of the clock. Conversely, if the clock is later than data, the BBPD makes the clock become fast. To determine whether the clock is fast or slow and whether a data transition is present, the BBPD samples input data by using three consecutive clock edges. For example, if the data value sampled by the first clock edge is different from the data values sampled by other edges, the clock is late. Reversely, if the data value sampled by first two edges is different from by the last edge, the clock is early. The timing diagrams of Fig. 1.4 shows the two cases of the BBPD operation. Fig. 1.4 (b) shows the case of clock late. The up signal that makes the clock

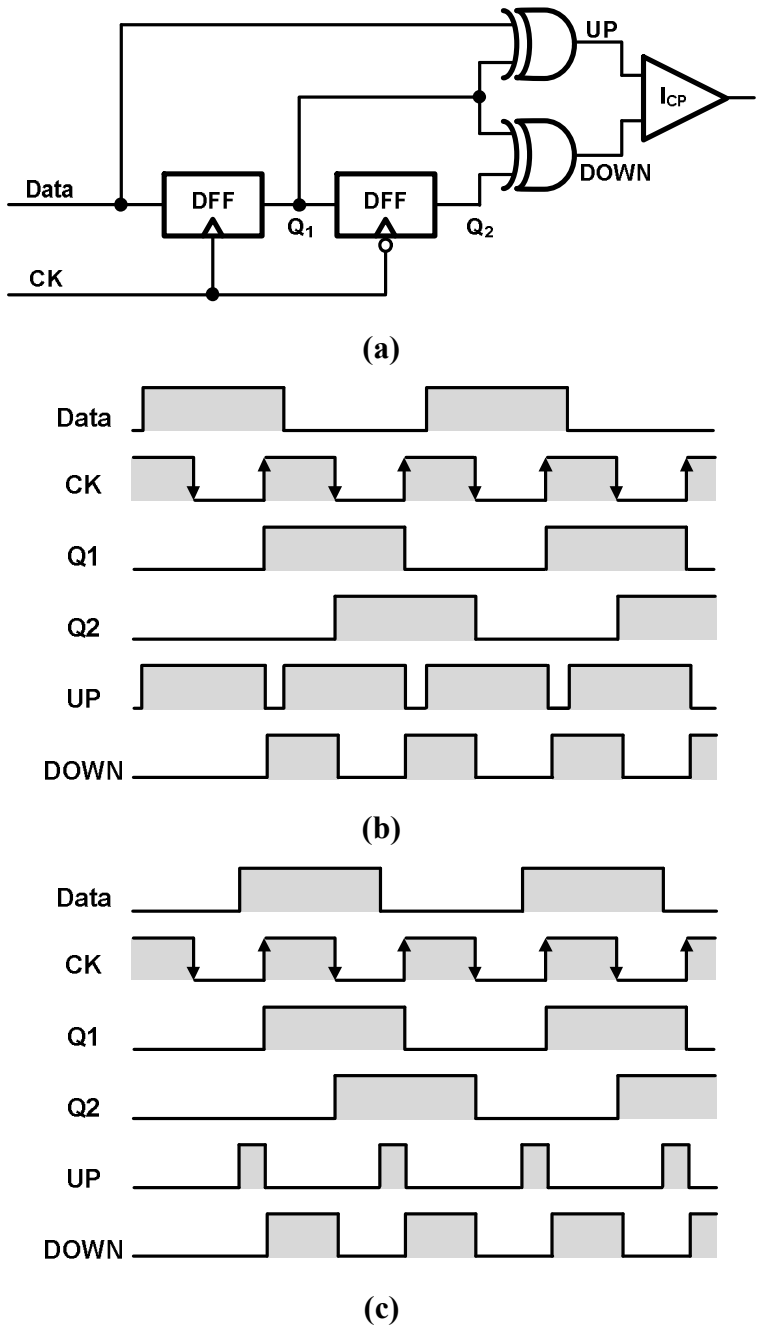
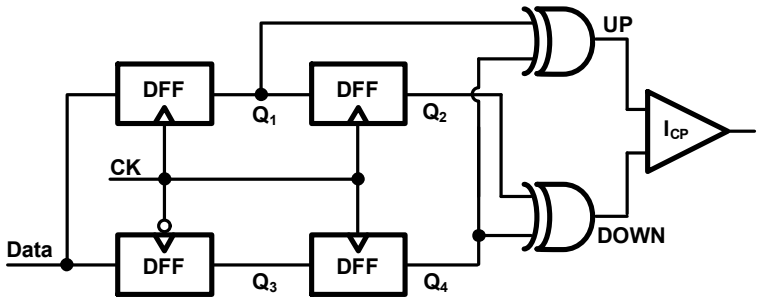


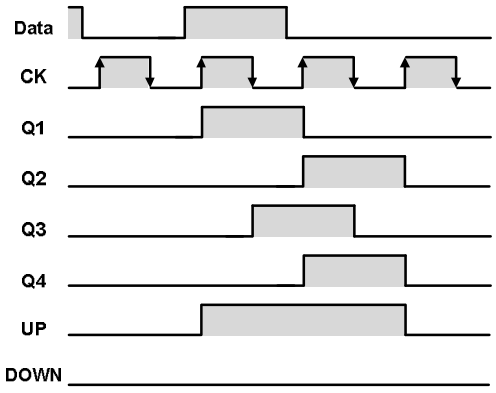
Fig. 1-3. Hogge PD (a) Structure (b) Clock is late condition
(c) Clock is early condition

fast goes high in this case. Fig. 1.4 (c) shows the case of clock early. So the down signal that makes clock slowly goes high. In the absence of data transitions, all three samples are equal and no action is taken. The outputs of BBPD maintain its level for one clock period is key point. Therefore, BBPD can operate two times faster than Hogge PD in principle. In addition, BBPD has digital characteristic because phase error signals generated by BBPD are three-state level digital signals corresponding to whether a data transition is early, late or absent relative to the clock phase within a clock period. Although BBPD structure is very simple and digital characteristic, it has significantly nonlinear characteristic. In small phase difference condition, the output of BBPD is always generated large phase difference. In conclusion, the output of BBPD is same whatever the condition is. Therefore, BBPD cannot detect the magnitude of phase difference between VCO clock and incoming data. And nonlinear characteristic produces large ripples in VCO control node voltage, resulting in larger jitter generation. The most serious problem of BBPD's nonlinear characteristic is nonlinear dynamics for CDR system. Thus, it is very difficult to analyze and optimize the BBPD CDR and very sensitive to process, voltage, and temperature (PVT).

In summary, these two PDs have pros and cons. Fig 1.5 shows the



(a)



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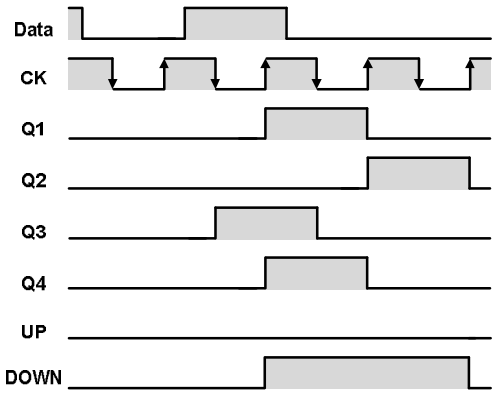
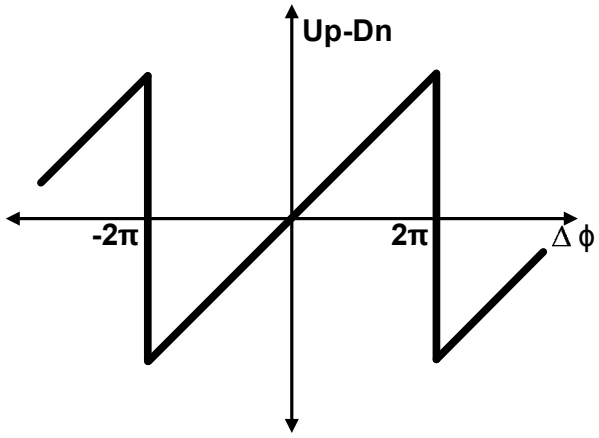


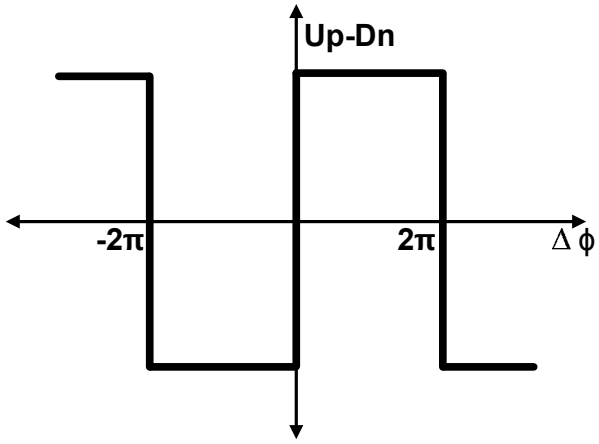
(c)

Fig. 1-4. Bang-Bang PD (a) Structure (b) Clock is late condition
(c) Clock is early condition

gain of the Hogge PD and BBPD. The BBPD has unstable position when the phase error is ‘0’, so it generates undesirable jitter component when the CDR is locked. However, the Hogge PD shows linear characteristic with respect to phase error though it is difficult to deal with short pulse near zero phase error. So the Hogge PD is suitable for optimizing CDR design due to linear characteristic of PD gain. And Hogge PD can decrease the jitter generated by CDR. However, It is difficult to deal with in high speed CDR due to speed limitation. On the other hands, the BBPD can operate a high speed operation, but the BBPD CDR suffers from its high PVT sensitivity and lows design reliability owing to its non-linear characteristic.



(a)



(b)

Fig. 1-5. Phase detector gain (a) Hogge PD (b) Bang-Bang PD

1.4. Multi-Rate Bang-Bang Phase Detector

CDR circuits operating at higher data rate pose difficult challenges with respect to speed, jitter, and signal distribution. We consider the technology limitations in the CDR with full-rate PD shown in Fig. 1.6 (a). The critical issue in Fig 1.6 (a) relates to design of VCO and frequency dividers. It may be difficult to design oscillators that provide an adequate tuning range and high frequency with reasonable jitter in the VCO circuit and suffer from speed limitation in the frequency divider. For this reason, we should consider the half-rate and quarter-rate PD structure shown in Fig. 1.6 (b) and (c). This technique can relax the speed requirements of the phase detector, VCO, and frequency divider. Fig. 1.6 (b) is called half-rate architecture. And half-rate CDR topologies require a phase detector that provides a valid output while sensing a full-rate random data stream and a half-rate clock. The concept of half-rate phase detection can be extended to quarter-rate operation as shown in Fig. 1.6 (c). This structure simply requires that the VCO generate eight phases to sample that every data transition by phase detector. A benefit of quarter-rate structure is that the circuit inherently provides 1-to-4 demultiplexing as well. For such a reason, multiphase CDRs having bang-bang phase detectors (BBPD) are

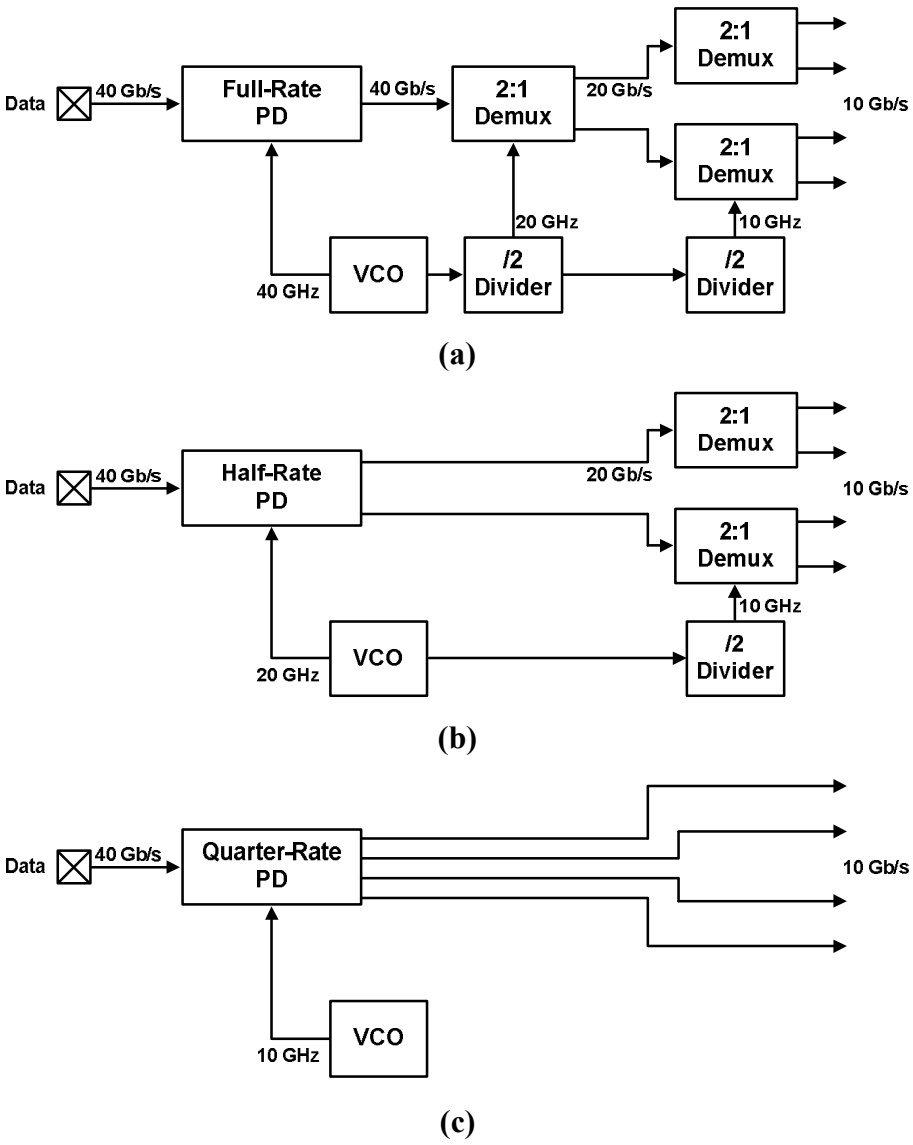


Fig. 1-6. (a) Full-rate CDR architecture (b) Half-rate CDR architecture (c) Quarter-rate CDR architecture

widely used for high-speed applications [7]-[10]. Because they can avoid the speed limitation by utilizing sub-rate clocks and BBPD and the digital nature of BBPD can be relatively easier implementation.

The structure of a half-rate bang-bang PD is shown in Fig. 1.7 (a). The circuit is composed of four D flip-flops, four XOR gates, and two charge pumps [11]-[14]. The half-rate BBPD uses two complementary data transition detectors to detect all the input data transitions. D flip-flops sample the data signal at the positive edges of the clocks. Through four XOR gates, these samples provide four output signals that control the two charge pumps and loop filter to generate the VCO controlling voltage. During the lock condition D flip-flops provide the recovered output data. In this phase detector, a large phase error results in a large voltage step and vice versa. Using four steps, instead of the two steps phase adjustment in full-rate BBPD, increases the linearity of the bang-bang phase detector and results in both low jitter generation and high lock-in range.

Fig. 1.7 (b) shows the structure of quarter-rate bang-bang PD. The circuit consists of eight D flip-flops, eight XOR gates, and four charge pumps [15]-[17]. In similar manner to half-rate BBPD, the quarter-rate BB PD compares every two consecutive samples through means of an XOR gate, generating a high level if the transition has occurred. To

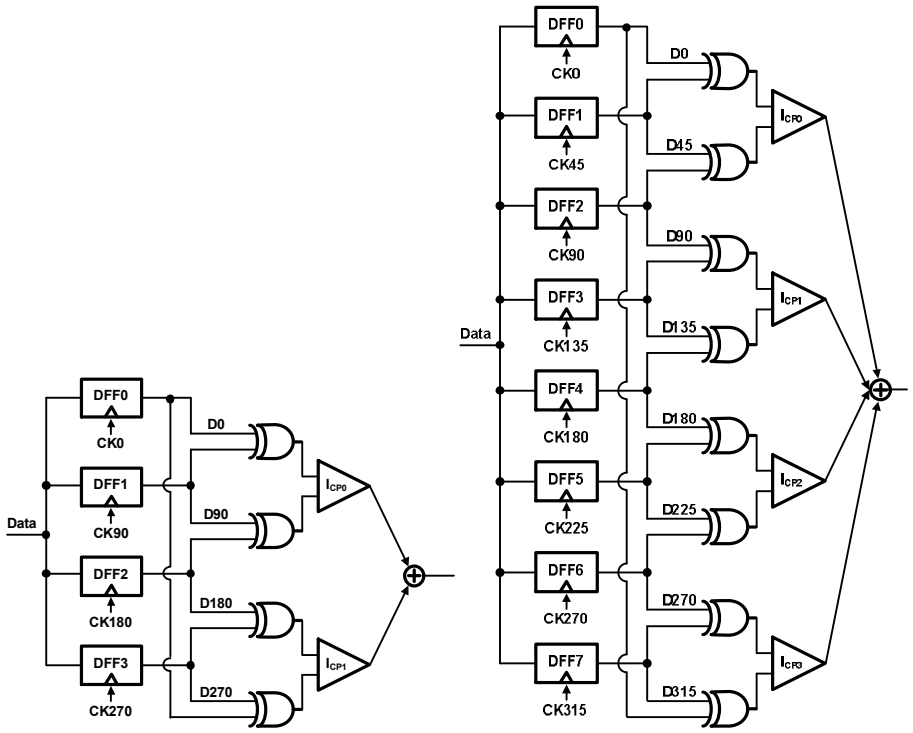


Fig. 1-7. Structure of the (a) Half-rate bang-bang PD and
(b) Quarter-rate bang-bang PD

TABLE 1.1
SUMMARY OF MUITI-RATE BBPD

	Full-rate BBPD	**Half-rate BBPD**	**Quarter-rate BBPD**
# of Clock phase	**2**	**4**	**8**
# of D F/F	**4**	**4**	**8**
# of XOR	**2**	**4**	**8**
# of Charge pump	**1**	**2**	**4**

determine the direction of the phase error from three consecutive samples, the outputs of two XOR gates are applied to a charge pump, which produces a output current if its inputs are not same. In lock condition, every other sample serves as retimed and demultiplexed output.

1.5. Outline of Dissertation

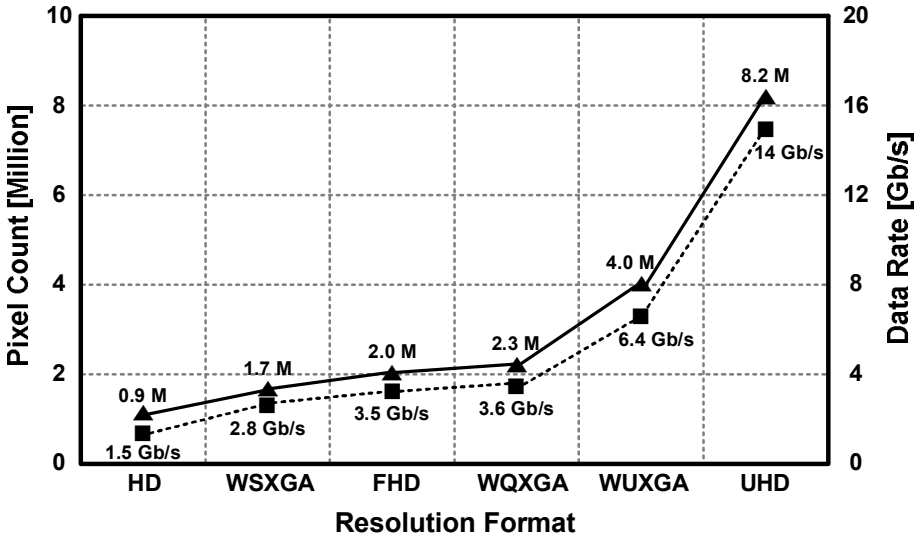
The main goal of this research is to investigate and develop a multi-rate CDR with novel structure of multi-mode rotational BBPD and frequency band detector whose power consumption and chip area is significantly reduced compared to the conventional multi-rate CDR. For this, a 3.5-, 7.0-, and 14.0-Gb/s multi-rate CDR is proposed and its prototype is implemented in 65-nm CMOS technology. The proposed MRBPD supports full-, half-, and quarter-rate operation with simple structure. The frequency band detector enables the selection of the desired frequency band without any external signals. In chapter 2, the basic concepts of CDR dynamics and noise analysis of CDR and conventional multi-rate CDR structure will be reviewed. The operational principle and analysis of proposed MRBPD and FBD are introduced in chapter 3. In chapter 4, the detailed schematic level circuits for our multi-rate CDR and the simulation results are described. In chapter 5, the experimental results will be showed. Finally conclusion is given in chapter 6.

2. Backgrounds and Motivations

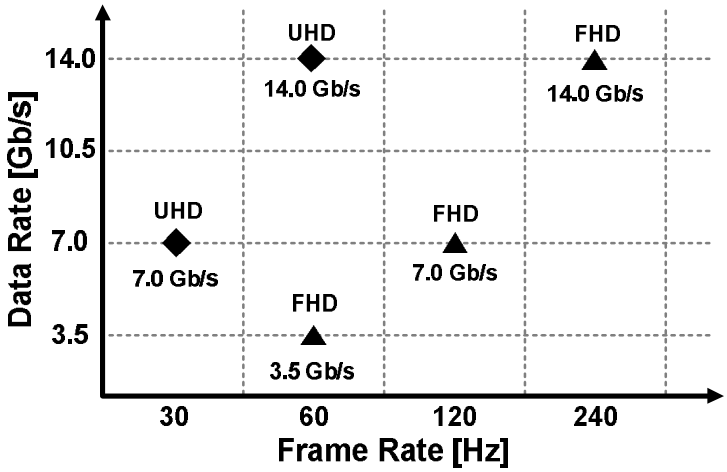
2.1. Display Interface

In display interface applications, the amount of multimedia data is rapidly increasing due to continuous demands for high definition TV (UHD, QUHD), comfortable 3-D display, and etc. As the frame rate, the color depth, and the resolution of display panel gradually increase, conventional display interfaces such as video graphic array (VGA) and digital visual interface (DVI) have trouble in processing the great deal of visual data as well as multimedia data. Therefore, the serialized interface such as HDMI and DisplayPort are used in the display these days. The state-of-the-art display can support WUXGA (2560 x 1600) and UHD (3840 x 2160) resolutions with the maximum data rate over 10 Gb/s as shown Fig. 2.1 (a).

Fig. 2.1 (b) shows the required video rates for FHD (1920 x 1080) and UHD resolutions of several frame rates by video electronics standard association (VESA) standard [18]. As shown in Fig. 2.1 (b), the data rates of 3.5-, 7.0-, and 14.0-Gb/s are particularly important for display high speed serial interface applications. For these applications, CDR circuits that can operate at multiple data rates are of great interest.



(a)



(b)

Fig. 2-1. (a) Maximum pixel count and data rate of resolution format
(b) Data rate of various resolution and frame rate

2.2. Multi-Rate CDR Application

According to display system interfaces as shown Fig. 2.1 (b), the receiver link should support multiple data rates. Therefore, a receiver needs a CDR circuit which is capable of the multi-rate operation. So far, there different design approaches were used to support the multi-rate operation in CDR design. One is by a multi-path design in VCO [19]. The multi-path VCO requires more delay cells and paths. The other approach is using a multi-load in VCO design [20]. The multi-load in VCO increases the capacitance of output node as more loads are used. The VCO also requires more currents to drive each delay cell. The third approach is using multiple VCOs (VCOs) and frequency detector with wide frequency acquisition [21]-[25] as shown Fig. 2.2. With such a structure, it is desired for all the VCOs to have the same gain so that stable CDR dynamics can be achieved. However, it is hard to achieve the constant VCO gain over all different frequency, which changes the loop bandwidth of the CDR circuit and reduces phase margin that is important for stability. Therefore, designing the multiple VCOs with the same gain can be very challenging. In addition, power consumption and chip area due to multiple VCOs can be significant.

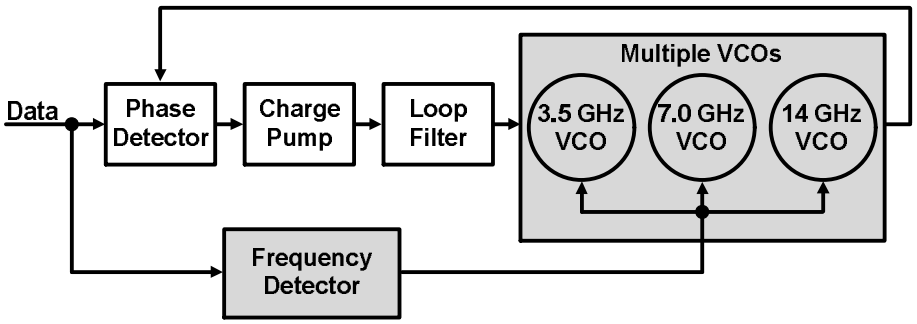


Fig. 2-2. Conventional structure of a multi-rate CDR circuit

2.3. Loop Dynamics of CDR

There are four jitter specifications that define the characteristics of the CDR; jitter transfer (JTRAN), jitter peaking (JPEAK), jitter tolerance (JTOL), and jitter generation (JGEN) [26]. First, jitter transfer means the ratio of the output and input jitter of the CDR. The jitter transfer of the CDR represents the output jitter as the input jitter is varied at different rates. The jitter transfer requires a low-pass response, because the CDR can filter out the jitter component of the input. Jitter peaking means the gain in the jitter transfer function which is undesirable as it leads to accumulation of jitter in a cascade of repeaters. Jitter tolerance is the amount of jitter permitted on the data input signal before the CDR does not make an error at the target specification. It is measure of the ability of the CDR to recover data from a noisy environment. It is desirable to have a large jitter tolerance bandwidth. Large jitter tolerance bandwidth means the CDR can track high-frequency jitter on the input data. Finally, jitter generation is the amount of jitter on the clock output of a CDR when clean input data is inserted into the CDR. It is the measure of how much the CDR generates extra jitter components.

The CDR system can be represented with simplified model to

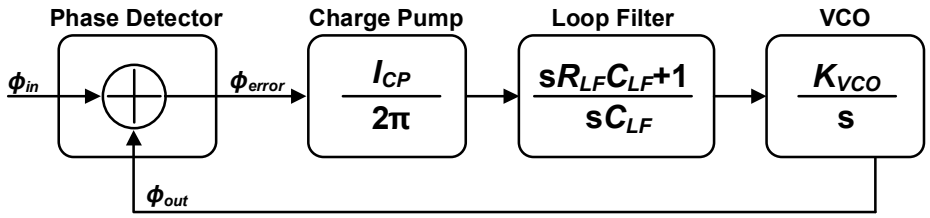


Fig. 2-3. Small signal model for CDR

derive the system transfer function as shown in Fig. 2.3. The simplified model of CDR is determined by design parameters such as phase detector gain (K_{PD}), charge pump (I_{CP}), loop filter (R_{LF} and C_{LF}), and VCO gain (K_{VCO}). The ideal PD can be expressed as a simple substracter and produce an output signal proportional to the two input phase difference. As s-domain analysis is required continuous time analysis, we assume that the charge pump flows continuous current over 2π period time. Therefore, the gain of charge pump has $I_{CP}/2\pi$. The loop filter transfer function can be easily expressed because it is consisted of resistor and capacitor elements. And the VCO transfer function can be represented as K_{VCO}/s, because the VCO has voltage input and phase output. ϕ_{in} is the phase of the input data, ϕ_{out} is the phase of the CDR output clock and ϕ_{error} is the phase difference between input data and CDR output clock. With this transfer function

represented sub-blocks, we can calculate the transfer function of the CDR between input data phase (ϕ_{in}) and output VCO clock phase (ϕ_{out}). First, the transfer function between ϕ_{in} and ϕ_{out} can be derived as below.

$$\frac{\phi_{out}}{\phi_{in}} = \frac{2\zeta\omega_n s + \omega_n^{\,2}}{s^2 + 2\zeta\omega_n s + \omega_n^{\,2}} \qquad (2.1).$$

$$where\ \zeta = \frac{R_{LF}}{2}\sqrt{K_{PD}\, I_{CP} C_{LF}\, K_{VCO}}$$

$$\omega_n = \sqrt{\frac{K_{PD}\, I_{CP}\, K_{VCO}}{C_{LF}}}$$

As can be seen from equation (2.1), the CDR system has a second order system because it consists of the two poles, one zero system. And its natural frequency ω_n, and damping ratio ζ are affected by design parameters. The transfer function depicted in equation (2.1) shows the relationship between the input data recovered clock phase and the recovered clock phase. This transfer function shows the low-pass filter characteristic that rolls off at high frequency. It means that the phase of the input data can be tracked by the VCO clock in the low frequency region, but high frequency region. Next, the transfer function between ϕ_{error} and ϕ_{out} can be derived as below

$$\frac{\phi_{error}}{\phi_{in}} = \frac{1}{2}\,\frac{s^2 + 2\zeta\omega_n s + \omega_n^{\,2}}{s^2} \qquad (2.2)$$

As can be seen from equation (2.2), the transfer function of the phase error between clock and input data shows the high-pass filter characteristics. It means that the high frequency phase error can be filtered out, while the low frequency phase error cannot be. Hence CDR can track the low frequency phase shift of the input data with the VCO clock. Therefore, the CDR can tolerate large amount of low frequency jitter, but high frequency jitter.

To get the good jitter transfer performance, the bandwidth of the CDR should be narrower. However, for the good jitter tolerance performance, the bandwidth of the CDR should be wider. But the jitter transfer and jitter tolerance corner frequencies are both set by ω_{p2}, which making it difficult to meet both specifications simultaneously. Hence, it is important to decide the proper bandwidth of the CDR considering the trade-off between the jitter transfer and jitter tolerance.

Fig. 2.4 shows the bode plot of jitter transfer and jitter tolerance functions. The solid line indicates the jitter transfer function and the dotted line is for jitter tolerance function. The zero ω_z is $1/R_{LF}C_{LF}$ and the pole ω_{p2} is approximately $R_{LF}K_{PD}K_{VCO}$. As shown in Fig 2.4, the characteristics of two transfer functions can be controlled by changing the zero (ω_z) and poles (ω_{p1}, ω_{p2}) position.

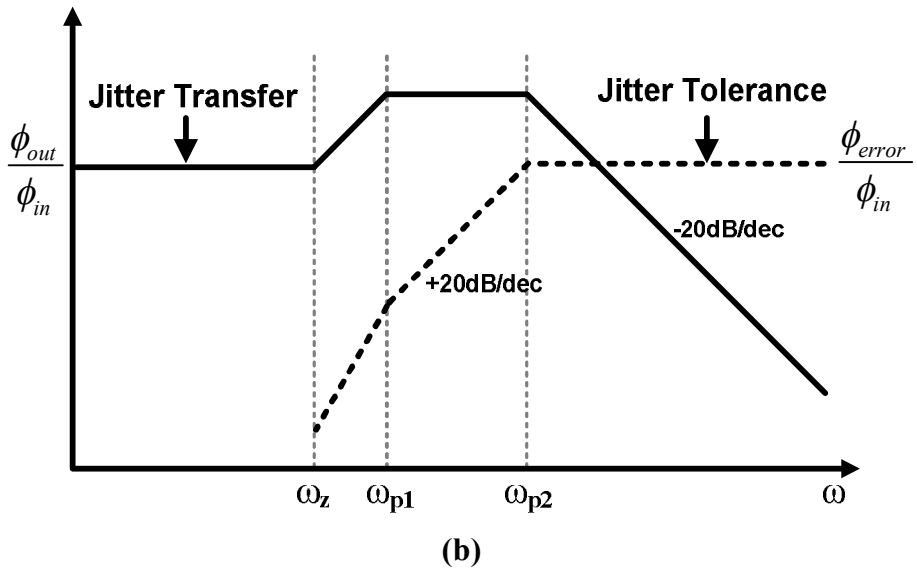


Fig. 2-4. The bode plot of jitter transfer and jitter tolerance function

2.4. Noise Analysis of CDR

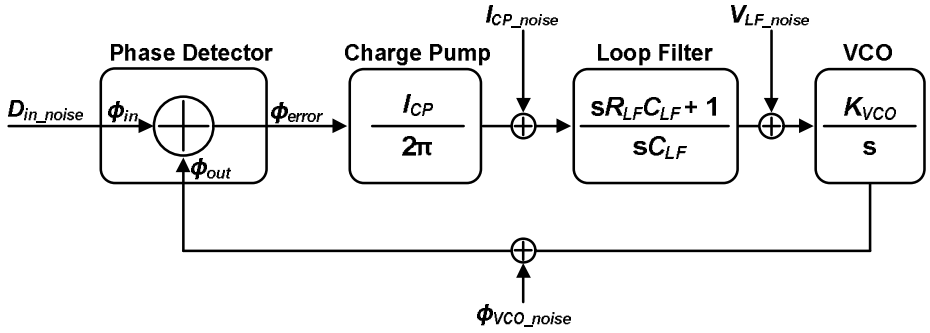


Fig. 2-5. Small signal model for CDR with various noise sources

With this continuous time analysis of CDR, we can get transfer functions in accordance with various input node. The transfer functions in accordance with various input nodes shown in Fig. 2.5 can be derived as

$$H_{in}(s) = \frac{\phi_{out}}{D_{in\_noise}} = \frac{H_{open}(\mathrm{s})}{1 + H_{open}(\mathrm{s})} \tag{2.3}$$

$$H_{CP}(s) = \frac{\phi_{out}}{I_{CP\_noise}} = \frac{H_{open}(\mathrm{s}) / (K_{PD} I_{CP})}{1 + H_{open}(\mathrm{s})} \tag{2.4}$$

$$H_{LF}(s) = \frac{\phi_{out}}{V_{LF\_noise}} = \frac{H_{open}(\mathrm{s}) / (K_{PD} I_{CP} Z_{LF})}{1 + H_{open}(\mathrm{s})} \tag{2.5}$$

$$H_{VCO}(s) = \frac{\phi_{out}}{\phi_{VCO\_noise}} = \frac{1}{1 + H_{open}(\mathrm{s})} \tag{2.6}$$

Where, $H_{open}(\mathrm{s}) = (K_{PD} I_{CP} Z_{LF} K_{VCO})/\mathrm{s}$ and $Z_{LF} = (\mathrm{s}R_{LF}C_{LF}+1)/\mathrm{s}$. The transfer functions are plotted in Fig. 2.6. To get the plotted simulation

results, we are used with these design parameters such as K_{PD}=1, I_{CP}=10mA, R_{LF}=100Ω, C_{LF}=100pF and K_{VCO}=300MHz/V. The transfer function between the phase of input data and phase of the recovered clock has low filter characteristics as shown in Fig. 2.6 (a), it can be filtered out high frequency phase variation of input data. As can be seen in Fig. 2.6 (b), the transfer function for the charge pump current noise (I_{CP_noise}) also has low pass filter characteristic. This means that we do not have to consider the fast changing I_{CP} because this I_{CP} variation can be filtered out by CDR feedback mechanism. On the other hand, the transfer function for the VCO noise (ϕ_{VCO_noise}) has high pass filter characteristic as can be seen in Fig. 2.6 (c). This means that slow jitter elements generated by the VCO are suppressed but fast jitter elements are. In the case of noises from loop filter (V_{LF_noise}) such as the thermal noise of resistor and capacitor, it has band pass filter characteristic as can be seen from Fig. 2.6 (d). To get optimum loop dynamics of CDR, first of all, we should closely consider a noise characteristic of each noise source. For instance, if the VCO phase noise is relatively larger than other phase noises, wide ω_n is required to filter the VCO phase noise as much as possible. On the other hand, if the I_{CP_noise} is larger than other noises, narrow ω_n is required to filter the I_{CP_noise}.

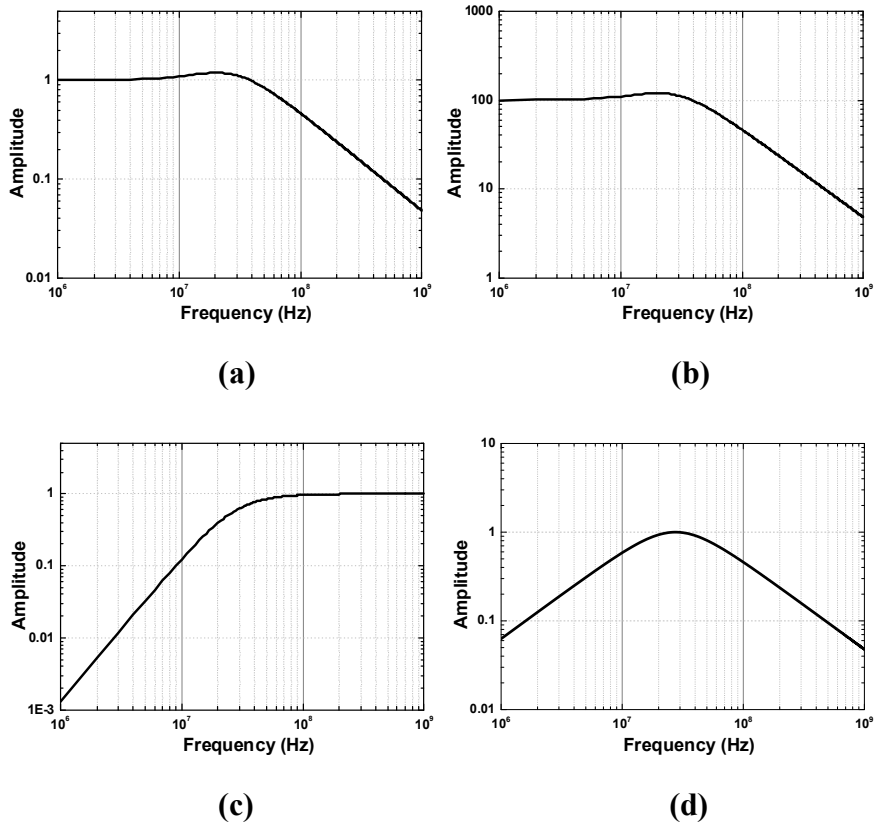


Fig. 2-6. Noise analysis of CDR (a) Input data vs ϕ_{out} (b) I_{CP_noise} vs ϕ_{out} (c) V_{LF_noise} vs ϕ_{out} (d) ϕ_{VCO_noise} vs ϕ_{out}

3. Multi-Rate CDR with MRPBD and FBD

3.1. Frequency Acquisition Process

Fig. 3.1 explains the frequency acquisition process in detail. When the loss of lock signal is low condition, the frequency tracking loop would be initialized. Initially, both FBD0 and FBD1 are set to low. With these signals, MRBPD operates in the full-rate operation and starts to track the input data frequency and achieves frequency lock or harmonic lock depending on the input data rate. Since clock frequency of the VCO can be tuned from 1.5 to 4.5 GHz, in the 3.5-Gb/s data rate, it achieves the frequency lock. In the others, it achieves the frequency harmonic lock. After the frequency tracking is finished, the FBD operates to achieve the appropriate MRBPD mode depending on the input data rate and generates its output signals (FBD0, FBD1). If the data rate is 3.5-Gb/s, FBD0 and FBD1 are both low. So MRBPD operates in the half-rate operation and resampling the received data. If the data rate is 7.0-Gb/s, FBD0 is low and FBD1 is high. Therefore, MRBPD operates in the half-rate operation. If the data rate is 14.0-Gb/s, FBD0 is high and FBD1 is high. Therefore, MRBPD operates in the quarter-rate operation. With FBD0 and FBD1 signals, the controller

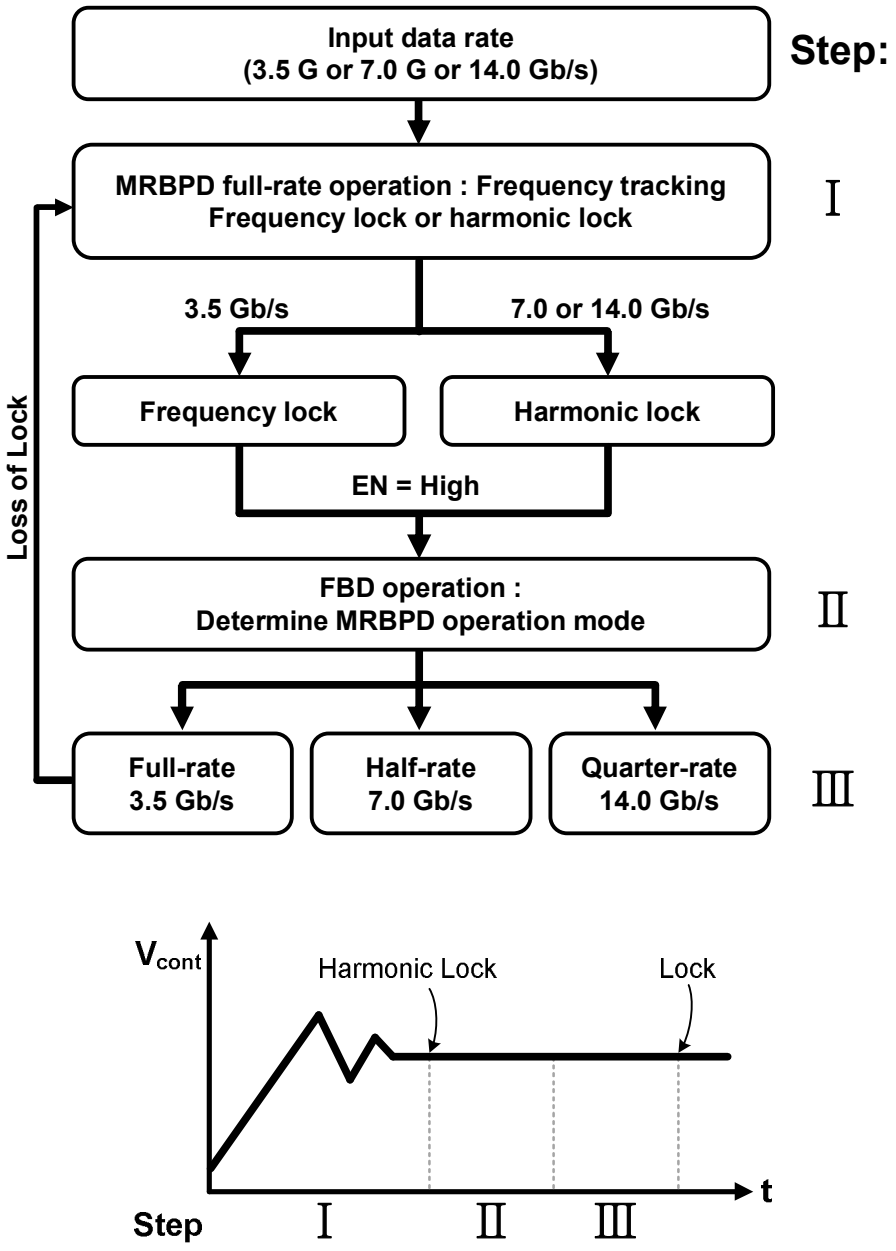


Fig. 3-1. Frequency acquisition sequence

generates rotating 4-bit control signals (T0~T3), which determine the MRBPD operation mode corresponding to the input data rate. When the CDR lost the phase lock temporarily, the frequency acquisition process is restarted. To demonstrate this frequency acquisition process, firstly, we check whether the circuit achieves the frequency lock or harmonic lock according to three different input data rates with full-rate operation. This simulation result comes from behavioral models of PD, CP, and VCO coded using Verilog_A. For this simulation, three different CDRs have same I_{CP}=500uA, K_{VCO}=100MHz/V, R_{LP}=40 Ω and C_{LP}=100pF. For easy timing measurement, the input data rates do not have noise source in this simulation. The input data rate only changes 3.5-, 7.0-, and 14.0-Gb/s to prove the frequency lock and harmonic lock. With the setting conditions, we can confirm that our CDR operates normally. Fig. 3.2 shows the timing diagrams for three different data rates. If the data rate is 3.5-Gb/s, it achieves the frequency lock and FBD0 and FBD1 signal are both low. If the data rate 7.0-Gb/s, it achieves the harmonic lock and FBD0 is low and FBD1 is high. If the data rate 14.0-Gb/s, it achieves the harmonic lock and FBD0 and FBD1 signal are both high.

In conclusion, due to the frequency harmonic locking characteristic of phase detector and frequency detector, we proposed the novel frequency band detector and prove the operation as shown fig. 3.2.

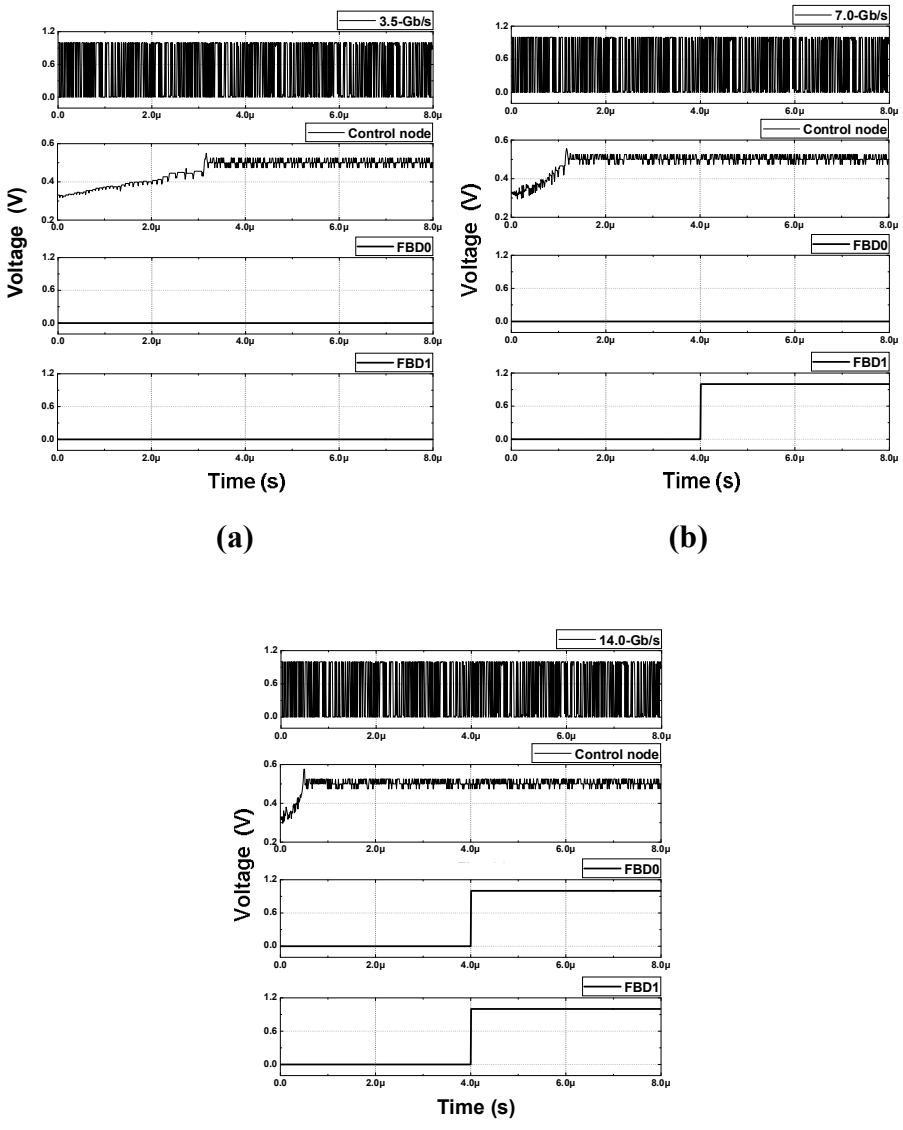


Fig. 3-2. Frequency acquisition simulations for three different data rates (a) 3.5-Gb/s (b) 7.0-Gb/s (c) 14.0-Gb/s

3.2. Multi-Mode Rotational Bang-Bang Phase Detector

3.2.1. Operational Principle

Conventionally, multi-mode Bang-Bang phase detector (BBPD) is composed of eight D flip-flops (DFFs), four Charge pumps, twelve XOR gates, twelve Latches, and four 4:1 MUXes as shown Fig. 3.3. [27]

Fig. 3.4 shows the half-rate and quarter-rate operation of the conventional multi-mode BBPD. When the CDR changes from the quarter-rate mode to the half-rate mode, data transition density (D) is reduced to 0.5D. Therefore, when the operation mode changes from the quarter-rate mode to the half-rate mode, the loop bandwidth is also reduced to 1/2 times. To prevent the bandwidth reduction, DN_{H0}/UP_{H0} and DN_{H1}/UP_{H1} are connected to $DN_{[Q0:Q1]}/UP_{[Q0:Q1]}$ and $DN_{[Q2:Q3]}/UP_{[Q2:Q3]}$, respectively. By this connection, the injected current by a single output pulse of the PD in half-rate operation is two times larger than a quarter-rate operation and thus the loop bandwidth can remain constant whatever operation mode is. However, this multi-mode BBPD is large power consumption and chip area due to complex structure. In addition, clock loading is much larger than conventional

quarter-rate BBPD due to operating the one DFF and two latches. The most serious problem of this structure is that there are many transistor paths from input node to the output node. Due to long signal path, signal latency is happened. As increasing signal latency, the CDR might happen to unlocking problem. In addition, this multi-mode BBPD can support half- and quarter-rate operations but not full-rate operation.

To overcome the problems, we develop the multi-mode rotational bang-bang phase detector (MRBPD) that is simple in its structure and supports full-, half-, and quarter-rate operations, resulting in much reduced power consumption and chip area. Fig. 3.5 shows the schematic of our MRBPD. The MRBPD changes the phase detection ratio for the multi-rate operation. This MRBPD operates 4-stage operation by the 4-bit signals (T0~T3) which are control signal to determine the phase direction. When only T0 signal is high, the MRBPD operates in State 1 and D_0, D_1, and D_2 are used as inputs to XOR gates as shown in Fig. 3.6 (a). When only T1 signal is high, the MRBPD operates in State 2 and D_4, D_5, and D_6 are used as inputs to XOR gates as shown in Fig. 3.6 (b). When only T2 signal is high, the MRBPD operates in State 3 and D_2, D_3, and D_4 are used as inputs to XOR gates as shown in Fig. 3.6 (c). When only T3 signal is high, the MRBPD operates in State 4 as and D_6, D_7, and D_0 are used as inputs to

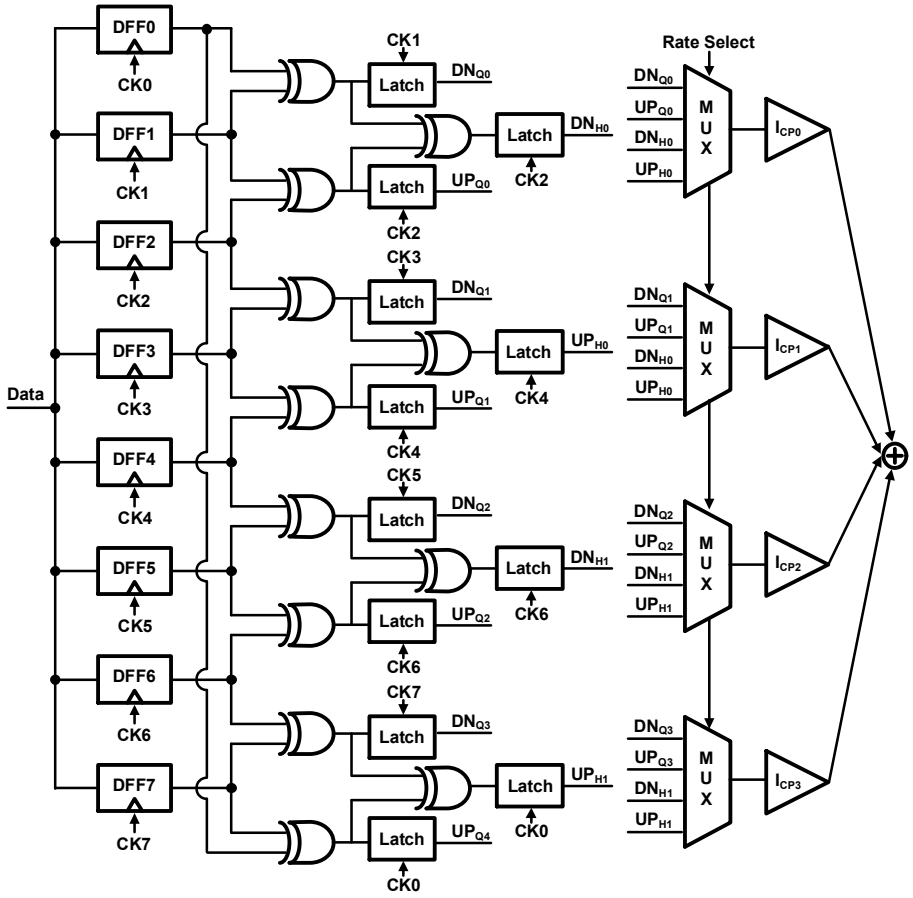
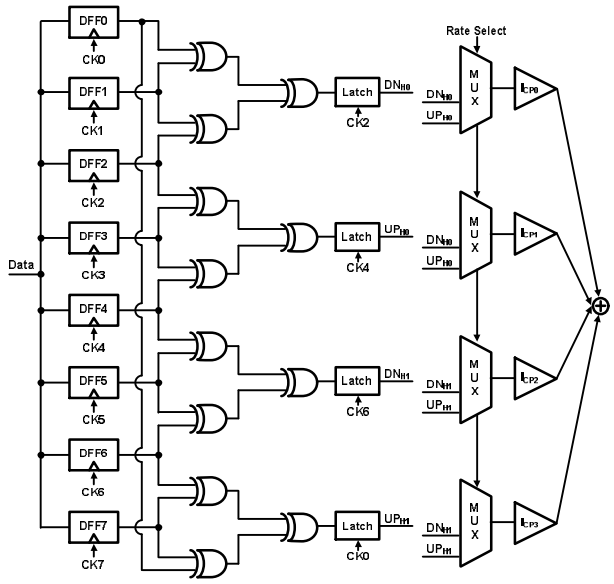
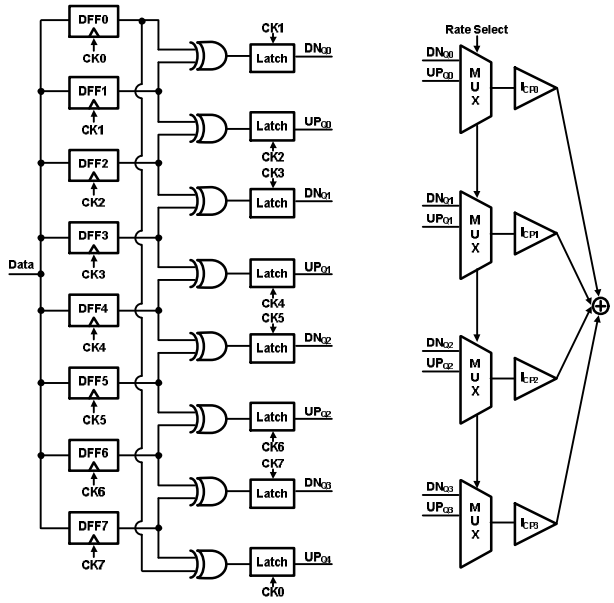


Fig. 3-3. Conventional multi-mode bang-bang phase detector



(a)



(b)

Fig. 3-4. Operation of the conventional multi-mode bang-bang phase detector (a) Half-rate operation (b) Quarter-rate operation

XOR gates shown in Fig. 3.6 (d). With this method, it supports full-, half- and quarter-rate operation by rotating the 4-bit control signals (T0~T3), which cause three MUXes (m1, m2, m3) within MRBPD realized with transmission gates to produce different sampled data depending on the mode.

Fig. 3.7 shows the timing diagrams for three different data rates. If the data rate is 3.5-Gb/s, FBD0 and FBD1 signals are both low. The controller only operates in State 1 and m1, m2, m3 produces D_0, D_1, D_2, respectively. These data are used as inputs to XOR gates, which generate UP and DN pulses to the charge pump. The XOR gates always operate to detect data transitions using only sampled data pair of D_0~D_2. The charge pump uses these pulses to compensate the phase error between received data and recovered clock. And the sampled data (D_5) by CK225 is used as the retimed data. With this, MRBPD operates as a full-rate bang-bang PD. If the data rate is 7.0-Gb/s, FBD0 is low and FBD1 is high. In this case, the controller alternates between State 1 and State 2 and m1, m2, m3 produces D_0, D_1, D_2 when in State 1 and D_4, D_5, D_6 when in State 2. The XOR gates alternately operate to detect data transitions using two sampled data pairs of D_0~D_2 and D_4~D_6 during the rotational period time. And the sampled data (D_3 and D_7) by CK135 and CK315 are used as the retimed data. Thus, MRBPD operates as a

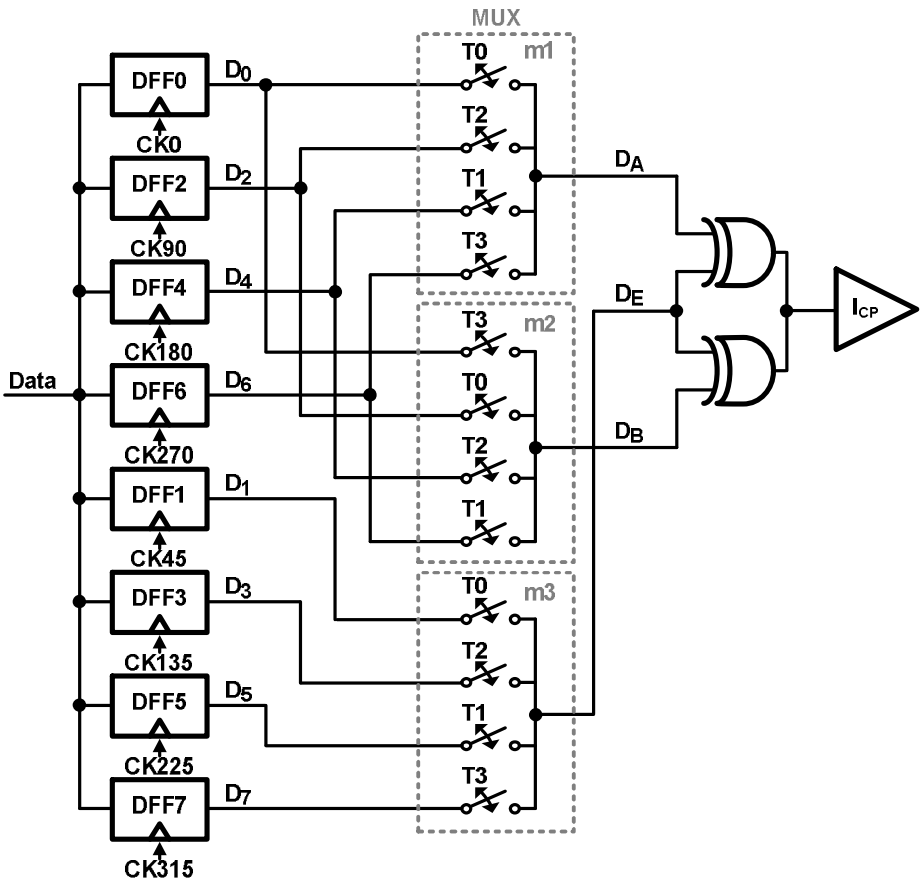
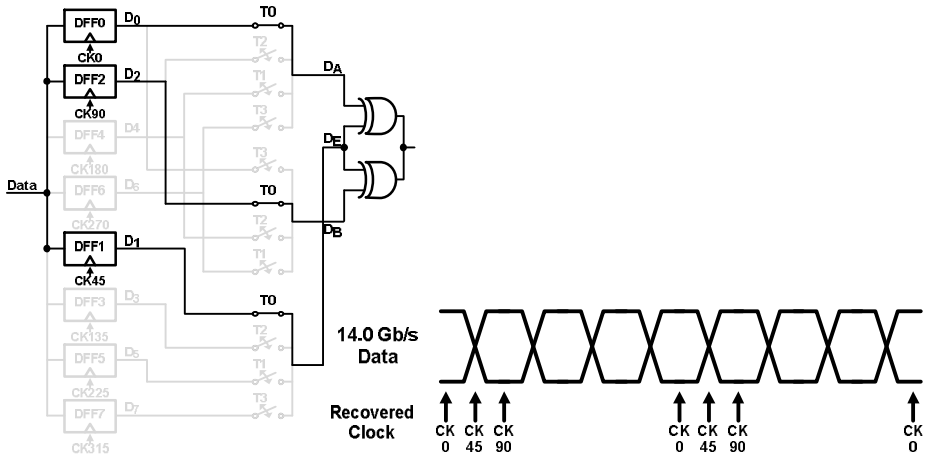
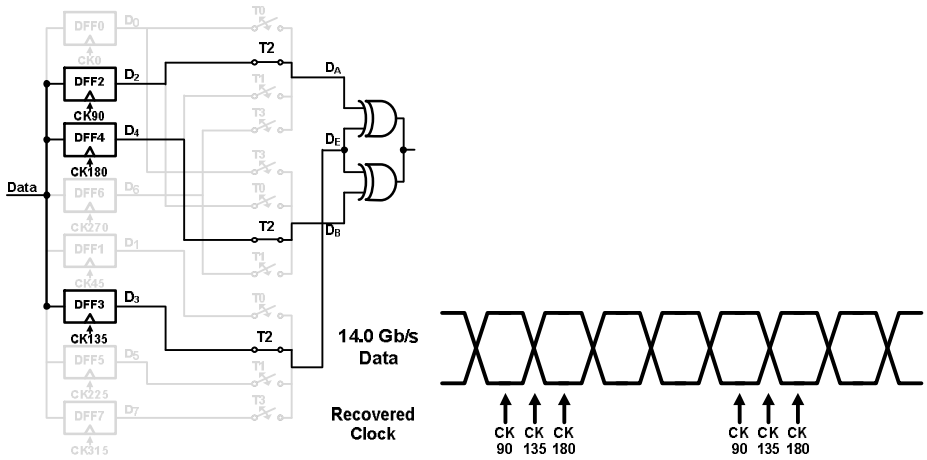


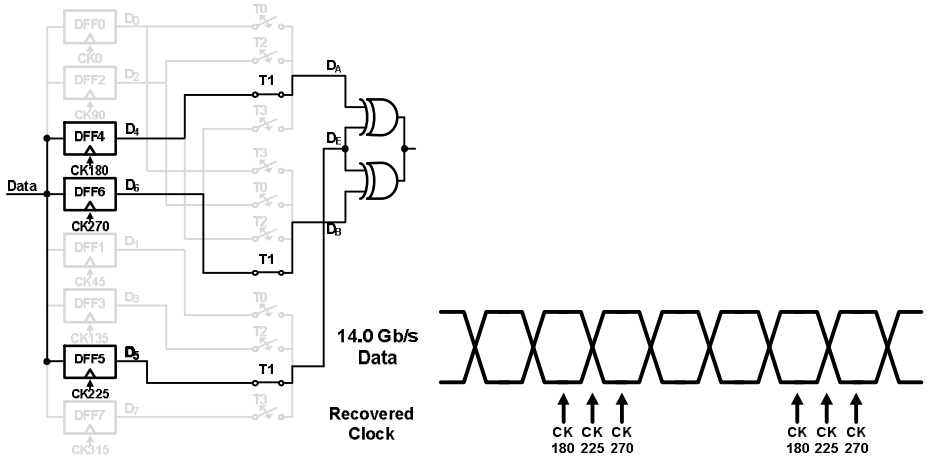
Fig. 3-5. Block diagram of proposed multi-mode rotational bang-bang phase detector (MRBPD)


DFF0
D0
CK0
DFF2
D2
CK90
DFF4
D4
CK180
DFF6
D6
CK270
DFF1
D1
CK45
DFF3
D3
CK135
DFF5
D5
CK225
DFF7
D7
CK315
Data
T0
T2
T1
T3
DA
DB
DE
14.0 Gb/s
Data
Recovered
Clock
CK 0
CK 45
CK 90
CK 0
CK 45
CK 90
CK 0

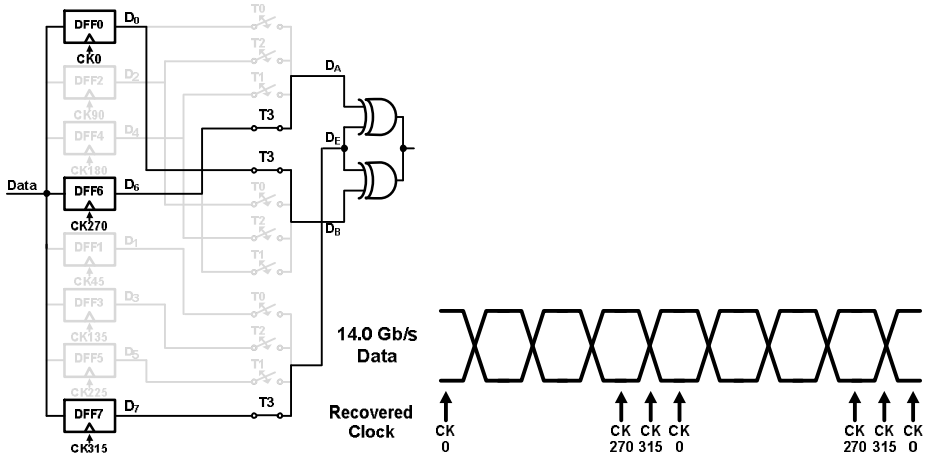
(a)


DFF0
D0
CK0
DFF2
D2
CK90
DFF4
D4
CK180
DFF6
D6
CK270
DFF1
D1
CK45
DFF3
D3
CK135
DFF5
D5
CK225
DFF7
D7
CK315
Data
T0
T2
T1
T3
DA
DB
DE
14.0 Gb/s
Data
Recovered
Clock
CK 90
CK 135
CK 180
CK 90
CK 135
CK 180

(b)



(c)



(d)

Fig. 3-6. MRBPD operation states (a) Stage 1 (b) Stage 2 (c) Stage 3 (d) Stage 4

TABLE 3-1
STRUCTURE COMPARISON AMONG MULTI-MODE BBPD

	Reference	Our MRBPD
Operation	**Half / Quarter**	**Full / Half / Quarter**
# of Clock phase	**8**	**8**
# of D F/F	**8**	**8**
# of Latch	**12**	**0**
# of XOR	**12**	**2**
# of Charge pump	**4**	**1**
# of 2:1 MUX	**4**	**0**
# of 4:1 MUX	**0**	**3**

Reference) W.Y. Lee, *et al.*, "A 5.4/2.7/1.62-Gb/s Receiver for DisplayPort Version 1.2 with Multi-Rate Operation Scheme" *IEEE TCAS-I*, 2012.

half-rate bang-bang PD. If the data rate is 14.0-Gb/s, FBD0 and FBD1 are both high. In this case, the controller rotates among State 1, State 2, State 3, and State 4. Then, m1, m2, m3 outputs are: D_0, D_1, D_2 when in State 1; D_2, D_3, D_4 when in State 2; D_4, D_5, D_6 when in State 3; D_6, D_7, D_8 when in State 4. The XOR gates alternately operate to detect data transitions using four sampled data pairs of D_0~D_2, D_2~D_4, D_4~D_6, and D_6~D_0. And the sampled data (D_0, D_2, D_4, and D_6) by CK0, CK90, CK180 and CK270 are used as the retimed data. Thus MRBPD operates as a quarter-rate bang-bang PD. With our MRBPD, six XOR gates, and there charge pumps can be eliminated compared to conventional quarter-rate PD circuits [17], resulting in reduced power consumption and chip area.

	T0	T1	T2	T3	D_A	D_E	D_B
State 1	1	0	0	0	D_0	D_1	D_2
State 2	0	1	0	0	D_4	D_5	D_6
State 3	0	0	1	0	D_2	D_3	D_4
State 4	0	0	0	1	D_6	D_7	D_0

Fig. 3-7. Timing diagram of the (a) Full-rate operation, (b) Half-rate operation, and (c) Quarter-rate operation

3.2.2. The Gain of MRBPD

The loop dynamics of CDR is determined by design parameters such as VCO gain (K_{VCO}), charge pump (I_{CP}), input data transition density (D_T), and PD gain (K_{PD}). Therefore, designer should carefully select the resistor and capacitor values of the loop filter considering each design parameters such as K_{VCO}, I_{CP}, and K_{PD}. In linear-PD CDR case, if the noise characteristic of each block in CDR is well-modeled, it is relatively easy to select design parameters and loop filter values because the well-known linear analysis can apply to the linear-PD CDR. However, the presence of the bang-bang phase detector (BBPD) introduces a hard non-linearity in the loop. Therefore, the loop filter value cannot be defined in a strict sense. Because the frequency domain approach cannot be used for BBPD CDR, the analysis completely in time domain is recently researched [28]. Even if these time domain analysis for BBPD CDR have been recognized, these research do not provide sufficient insight for designing BBPD CDR. Designers still want to have ways to explain them in linear control term. A way of describing BBPD CDR in the context of linear control theory by using effective linearized gain concept for BBPD is also presented in [29]-[30].

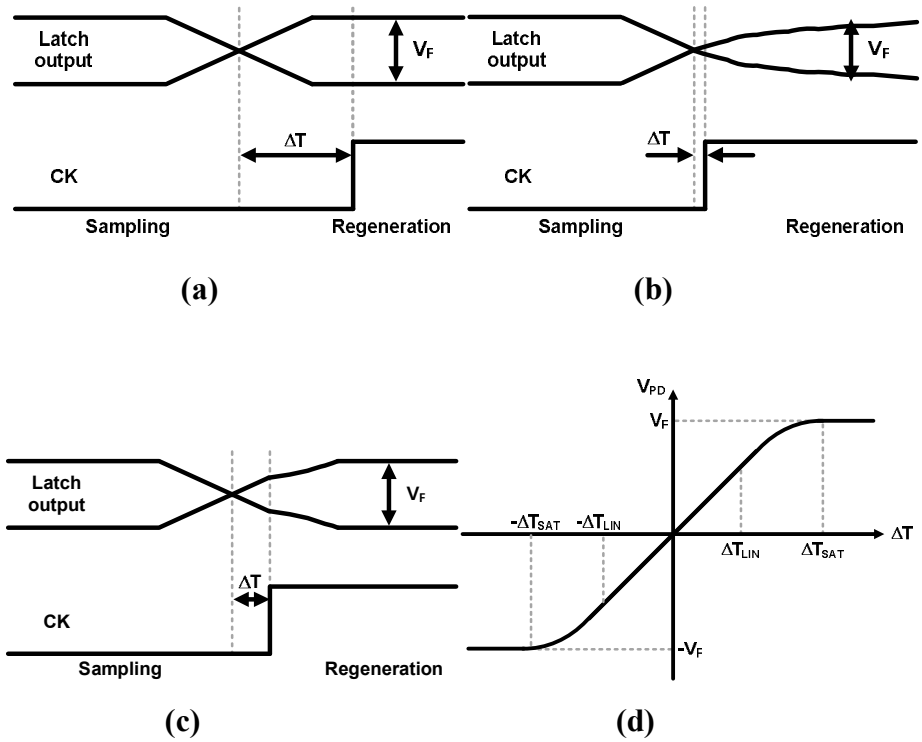


Fig. 3-8. (a) BBPD output for complete differential pair switching
(b) BBPD output for partial differential pair switching
(c) BBPD output for incomplete output for differential pair switching
(d) Typical BBPD characteristic

The linear region of BBPD is generated by two phenomena as explained in [29]. First, when the zero-crossing points of the recovered clock rise in the vicinity of data transitions, the flip-flops comprising the PD may experience metastability, thereby generating an output lower than the full level for some time. In other words, the average output produced by the PD remains below the saturated level for small phase differences between input data and recovered clock.

Fig. 3.8 indicates three distinct cases that determine certain points on the BBPD characteristic. If the phase difference between recovered clock and input data, ΔT, is large enough, the latch output reaches the saturated level, V_F, in the sampling mode as shown in Fig. 3.8 (a). By contrast, if ΔT is small, the regeneration in half a clock period does not amplify latch output to V_F due to metastability of practical latch circuits. The smaller is the lower the latch output in regeneration mode is as can be seen in Fig. 3.8 (b) and (c). Since the current delivered to the loop filter is proportional to the area under difference between two latch outputs, the average output is indeed linearly proportional to ΔT. Fig. 3.8 (d) summarizes these concept. ΔT_{LIN} *and* ΔT_{SAT} can be depicted as

$$\Delta T_{LIN} = \frac{V_F}{2kA_{pre}\exp(T_b / 2\tau_{reg})} \tag{3.1}$$

$$\Delta T_{SAT} = \frac{V_F}{2kA_{pre}} \tag{3.2}$$

Where, $2 \cdot k \cdot A_{pre}$ is the slew rate of latch circuit, τ_{reg} is regeneration time constant, and T_b is one bit period.

The BBPD characteristic is also smoothed out by the jitter inherent in the input data and the recovered clock. Even with abrupt data and clock transitions, the random phase difference resulting from jitter leads to an average output lower than the saturated levels. As illustrated in Fig. 3.9 (a), for a phase difference of ΔT, it is possible that the tail of the jitter distribution shifts the clock edge to the left by more than ΔT, forcing the phase detector to sample a level of $-V_0$ rather than $+V_0$. To obtain the average output under this condition, we sum the positive and negative samples with a weighting given by the probability of their occurrences:

$$V_{PD}(\Delta T) = -V_0 \int_{-\infty}^{-\Delta T} p(x)dx + \int_{-\Delta T}^{-\infty} p(x)dx \tag{3.3}$$

Where *p(x)* denotes the probability density function (PDF) of jitter. As a result, the BBPD characteristic exhibits a relatively linear range as shown in Fig. 3.9 (b).

Fortunately, the BBPD CDR operates within the linear range of BBPD under the lock condition, this concept allows for linear analysis

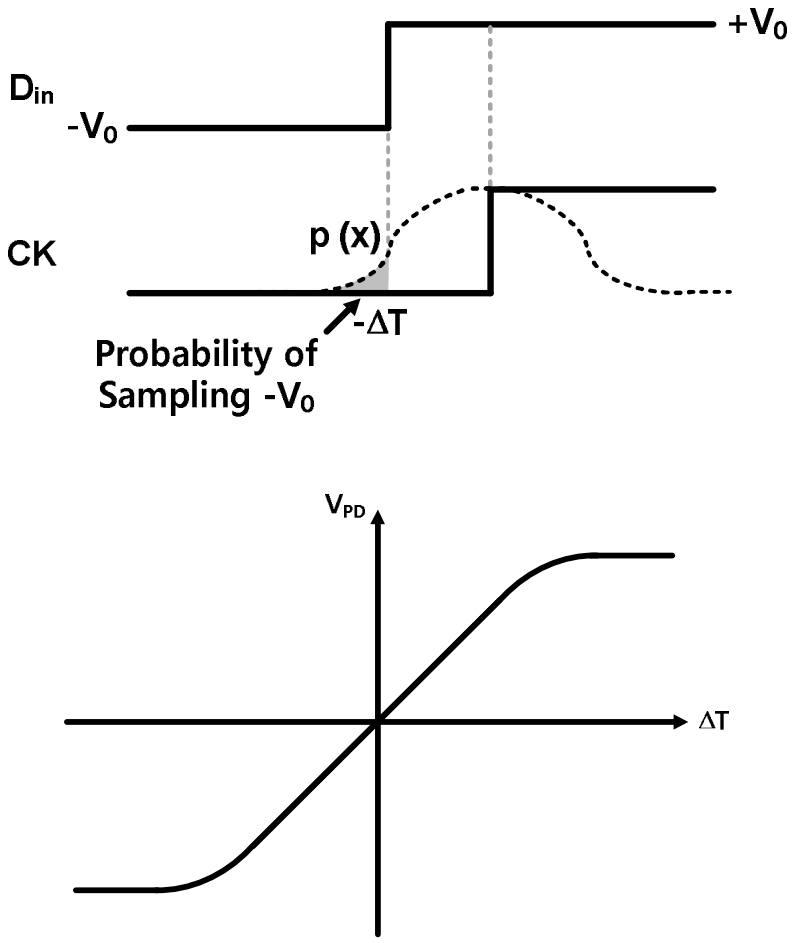


Fig. 3-9. Smoothing of PD characteristic due to jitter

of non-linear bang-bang control loop in a statistical sense.

The multi-rate rotational bang-bang phase detector (MRBPD) has constant PD gain (K_{PD}) regardless of the operation mode, because MRBPD always operates having same VCO clock and detects by clock rising edge. Consequently, the D flip-flops comprising the MRBPD experience same metastability as shown Fig. 3.10. Because of it, the average output of MRPBD remains constant level for a small phase difference between input data and VCO clock. Fig. 3.11 shows the gain of the MRBPD for full-, half-, quarter-rate operations with 3.5-. 7.0- and 14.0-Gb/s input data. This simulation result comes from schematic level. For easy gain of the MRBPD measurement, the input data do not have noise sources in this simulation. The gain of the MRBPD circuit can remain constant regardless of the operation mode. In other words, it achieves the constant K_{PD} over the all frequency data rate. In conclusion, having the constant K_{PD} makes it easy to choose other design parameter to achieve the optimum loop dynamics regardless of the operation mode.

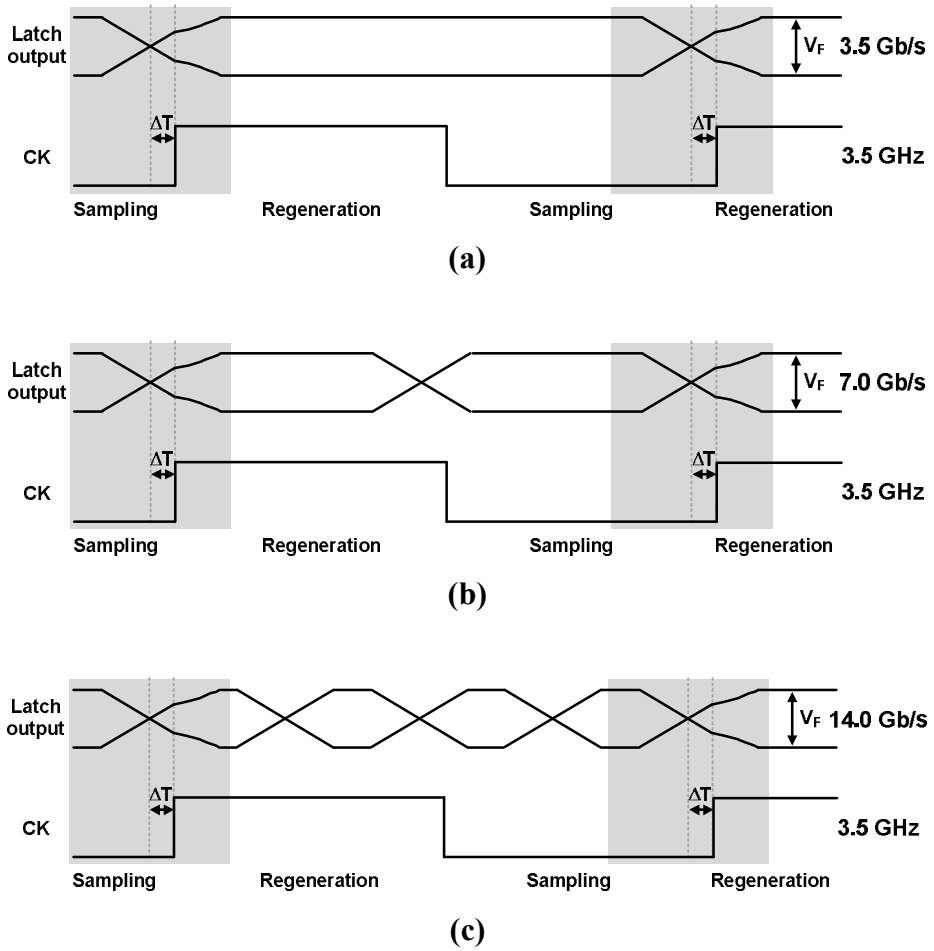


Fig. 3-10. MRBPD output for (a) Full-rate operation, (b) Half-rate operation, and (c) Quarter-rate operation

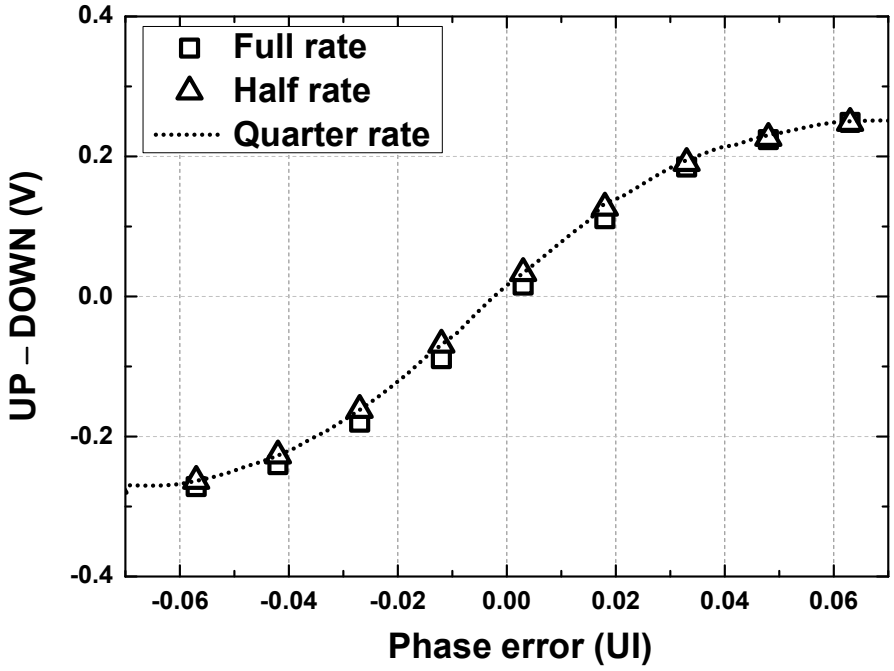


Fig. 3-11. MRBPD gain graph to full-, half-, and quarter-rate operation

3.2.3. The Loop Dynamic of Multi-Rate CDR with MRBPD

Referring to [29], the loop bandwidth of a BBPD CDR circuit (*LBW*) is can be expressed as

$$LBW = DK_{VCO}I_{CP}R_{LF}K_{PD} \tag{3.4}$$

where D is the data transition density, I_{CP} is output current of the charge pump per transition, K_{PD} is the gain of BBPD, and R_{LF} is the resistance for the resistor in the loop filter. If the Conventional multi-rate CDRs with the multi-mode PD changes from the quarter-rate mode to the half-rate mode, D is reduced to 0.5D. Therefore, when the operation mode changes from the quarter-rate mode to the half-rate mode, the loop bandwidth of the half-rate mode is also reduced to 1/2 times the loop bandwidth of quarter-rate mode. To prevent the bandwidth reduction, the injected charge pump current by a single output pulse of the XOR in a half-rate mode operation is two times larger than a quarter-rate mode operation and thus the loop bandwidth can remain constant whatever operation mode is. Thus, Conventional multi-rate PD has the complex structure to resolve the problem. However, in our MRBPD case, since the control signal changes every rotating period time, the data transition detection density of our multi-rate CDR is

same of that of the conventional full-rate CDR [10], and 1/2 of that of the conventional half-rate CDR [12], and 1/4 of that of the conventional quarter-rate CDR [17]. However, this would not have a significant influence on CDR performance because rotation of data sampling is much faster than the CDR loop bandwidth. As a result, Our CDR is designed to have the constant transition density no matter what the mode is, because 2-stage XOR gates compare the same number of data transitions for a given time. And our CDR always operates with constant I_{CP}, R_{LF} and K_{VCO} regardless of the operation mode. Consequently, the loop bandwidth remains constant regardless of the operation mode. As our CDR achieves constant loop bandwidth at three different MRBPD, it is easy to ensure phase margin that is important for stability.

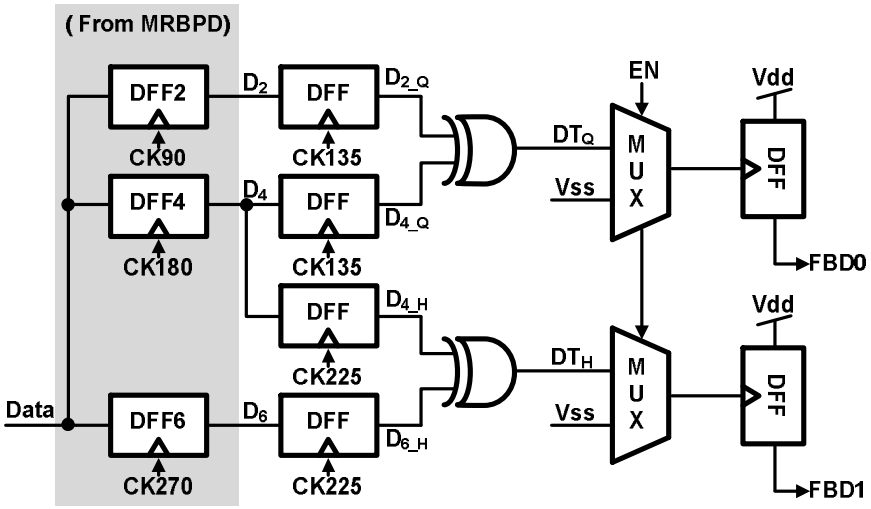
3.3. Frequency Band Detector

Most CDR circuits need a reference clock, which may be supplied by a transmitted signal or fed by external clock source such as crystal. However, the former needs an additional channel to transmit a clock signal, leading to larger power consumption, worse electromagnetic interference, and higher cost. The latter also suffers from problems such as inflexibility of the system to frequency changes and high cost. CDR circuits without using the reference clock signal need to overcome these problems. Several frequency detectors that can extract the frequency information from the input data without using an external clock signal have been proposed [31]-[32]. However, these frequency detectors have a limited acquisition range of about ±50%, and are susceptible to harmonic locking, which is not suitable for display systems links. Wide-range CDR circuits embedded clock signal have been presented in [33]-[35]. However, it takes a long time to acquire the frequency because of the complicated acquisition processes. Furthermore, CDRs in [33] and [35] require periodic predefined patterns, such as repeated comma patterns in 8B10B encoding, for their frequency acquisition processes, or special sync patterns, in addition to the encoding schemes for dc balancing and frequency information acquisition. The proposed FBD structure and frequency acquisition

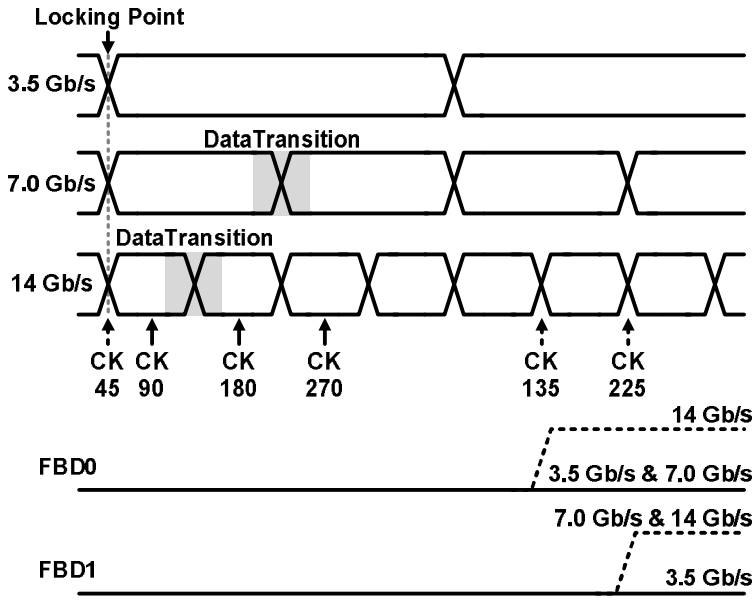
schemes that do not need additional periodic patterns are used to achieve a fast frequency acquisition time and variable data rates. In addition, it consumes the low power because of a simple structure.

The proposed frequency band detector (FBD) is shown in Fig 3.12 (a). In order to select an appropriate operation mode of MRBPD, FBD should have the ability of detecting the harmonic frequency. The enable signal (EN) enables FBD operation when CDR is locked, and the FBD detects the presence of the data transition within each two adjacent multiple clocks. Initially, when powering on, MRPBD operates in full-rate operation and starts to track the input data frequency and phase. As a result, the MRBPD achieves the frequency and phase lock or harmonic lock at CK45 phase point. The FBD uses sampled data at the rising edge of the signal CK90, CK180 and CK270 with the D flip-flops (DFFs) in the MRBPD. The sampled data are aligned with CK135 and CK225 by the DFFs. After this, D_{2_Q}, D_{4_Q}, D_{4_H}, and D_{6_H} are processed by two XOR gates, which generate DT_Q and DT_H. DT_H and DT_Q signals store the data transition information and serve as a key to ensure the appropriate mode operation of MRPBD. Fig. 3.12 (b) shows the timing diagram in the operation condition. If the data rate is 3.5-Gb/s, since there is no data transition, D_{2_Q}, D_{4_Q}, D_{4_H}, and D_{6_H} are always the same. As a result, FBD0 is low and FBD1 is low. If the data

rate is 7.0-Gb/s, there is data transition information between CK180 and CK270, but not between CK90 and CK180. As a result, FBD0 is low and FBD1 is high. If the data rate is 14.0-Gb/s, there is data transition information between CK90 and CK180 and between CK180 and CK270, respectively. As a result, FBD0 is high and FBD1 is high.



(a)



Input data rate	FBD0	FBD1
Full rate (3.5 Gb/s)	LOW	LOW
Half rate (7.0 Gb/s)	LOW	HIGH
Quarter rate (14 Gb/s)	HIGH	HIGH

(b)

Fig. 3-12. Frequency band detector (a) Structure (b) Timing diagram

4. Implementation

4.1. Overall Architecture

The structure of our proposed multi-rate CDR is shown Fig. 4.1. It has newly proposed multi-rate mode rotational bang-bang phase detector (MRBPD), frequency band detector (FBD), charge pump, controller and 8-phase VCO. An off-chip loop filter is adopted in our design for optimizing the performance of our CDR. The 8-phase VCO generates full-swing 8-phase clocks and its output frequency can be tuned from 1.5 to 4.5 GHz with an external coarse tuning voltage. Phase errors between received data and the generated clock are detected by MRBPD which enables the multi-mode operation by rotating the 4-bit control signals (T0~T3). The FBD determines the mode of the MRBPD based on the relationship between data rate and clock frequency. The controller generates 4-bit control signals (T0~T3) depending on the 2-bit signals (FBD0, FBD1) from FBD, which makes MRBPD operates in the desired mode.

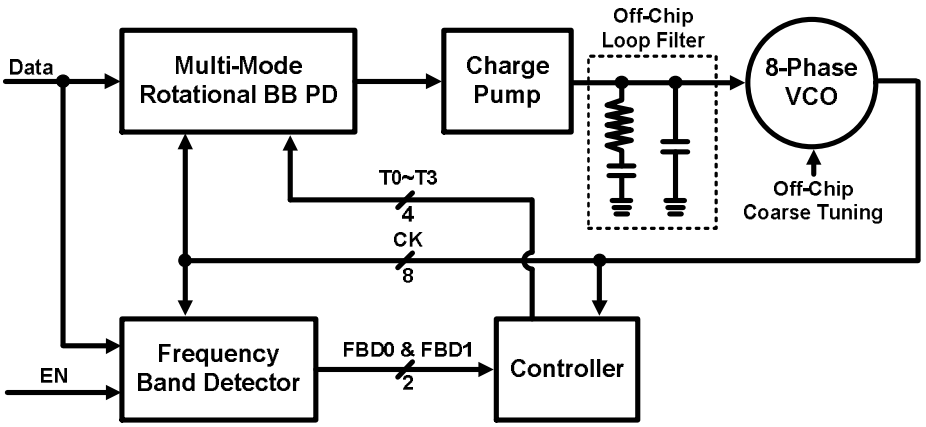


Fig. 4-1. Architecture of proposed multi-rate CDR

4.2. Multi-Mode Rotational Bang-Bang Phase Detector

The structure of our multi-mode rotational bang-bang phase detector (MRBPD) is shown in Fig. 3.4. It has the eight D flip-flops, three 4:1 MUXes, and two XOR gates. All D flip-flops in the MRBPD is used for the sampling input edge and data. The number of D flip-flops in the MRBPD is same as conventional quarter-rate BBPD. The only difference between our MRPBD and conventional quarter-rate BBPD is the number of the XOR gates. With our MRBPD, six XOR gates can be eliminated compared to conventional quarter-rate BBPD circuits, resulting in reduced power consumption and chip area.

The D flip-flop which is a unit building block for MRPBD is realized with sense-amplifier and two NAND gates as shown in Fig. 4.2 (a). This sense amplifier combines strong positive feedback with a high resistive input. The current flow of the differential input transistors connected latch circuit. A small difference between the currents through input transistors converts to a large output voltage. The D flip-flop based on sense amplifier has high input sensitivity by the benefit of the latch operation of sense amplifier. However, the output signal of the sense amplifier generates RZ type data. Therefore, a NAND latch is required for converting RZ type data into NRZ type data.

The XOR and XOR bar gates which are a unit building block for MRPBD is realized with CMOS logics for reducing power consumption as shown in Fig. 4.2 (b) and (c). We need XOR bar gates for generating 'DOWN' signal of MRPBD. Because the chare pump circuit consists of the different type of switching MOS.

The 4:1 MUX is realized with transmission gate CMOS logics for a reduction in number of transistors as shown in Fig. 4.2 (d). It is made by parallel combination of NMOS and PMOS transistors with the input at the gate of one transistor being complementary to the input that gate of the other. The transmission gate acts as a bidirectional switch controlled by the gate signals (C0, C0_bar). When C0 is high, both MOSFETs are on, allowing the signal to pass through the gate. In short, IN = OUT, if C0 = high. On the other hand, C0 is low, places transistors in cut-off, creating an open circuit between IN and OUT.

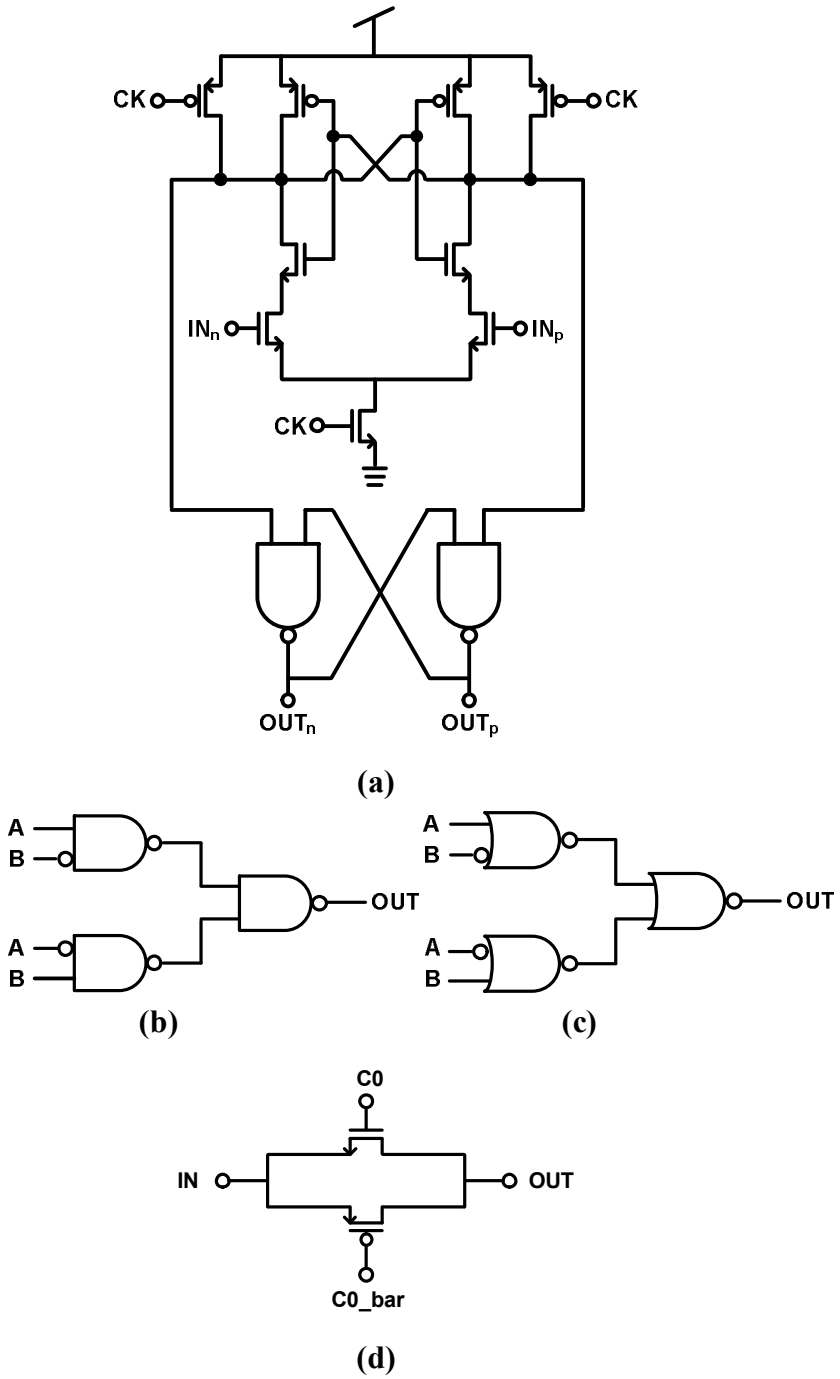
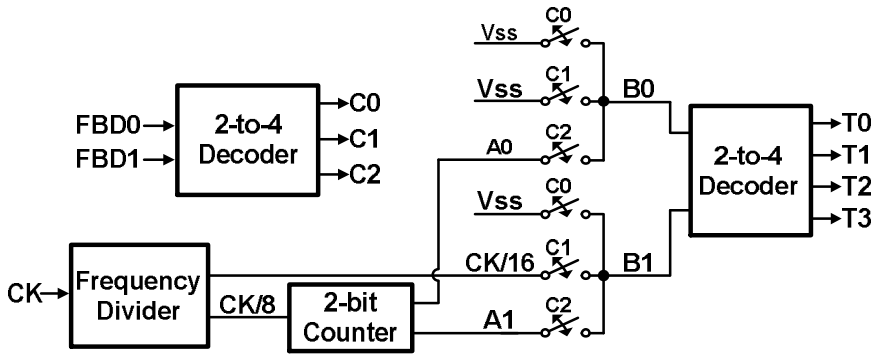


Fig. 4-2. Structure of the (a) D flip-flop, (b) XOR, (c) XOR bar, and (d) MUX

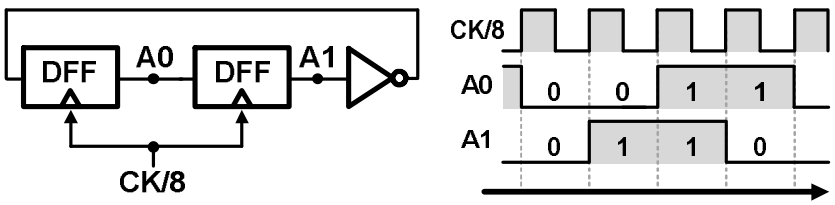
4.3. Frequency Band Detector & Controller

The proposed frequency band detector (FBD) is composed of nine D flip-flops, two XOR gates, and two 2:1 MUXes as shown Fig. 3.12. The D flip-flops (DFFs) which operate with the rising edge of the CK is realized with sense-amplifier and two NAND gates. Because those D flip-flops (DFFs) are necessary to high input sensitivity. And D flip-flops (DFFs) of the last stage is realized TSPC (True Single Phase Clock) because of the rail to rail swing input. The XOR gates are realized CMOS logics and 2:1 MUXes are realized transmission gate logics to store the data transition information.

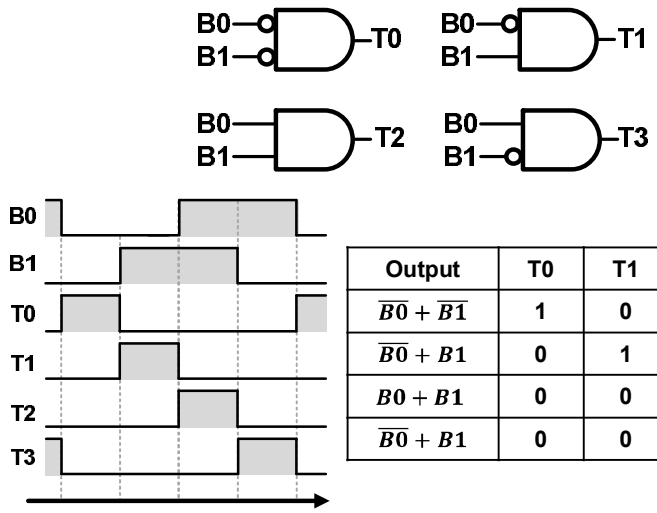
Fig. 4.3 (a) shows the schematic of the controller. The frequency divider generates CK/8 and CK/16 dividing clocks from VCO clock signal. The 2-bit counter, whose schematic is shown in Fig. 4.3 (b), generates 2-bit output signals (A0, A1). The 2-bit counter is designed Johnson courter circuit which is a modified ring counter, where the inverted output from the last D flip-flop is connected to the input to the first. The main advantage of this type of counter is that it only needs half the number of D flip-flops compared to the standard ring counter then its number is halved. So a “n-stage” Johnson counter will circuit a single data bit giving sequence of 2n different states and can therefore



(a)



(b)



Output	T0	T1	T2	T3
$\overline{B0} + \overline{B1}$	1	0	0	0
$\overline{B0} + B1$	0	1	0	0
$B0 + B1$	0	0	1	0
$\overline{B0} + B1$	0	0	0	1

(c)

Fig. 4-3. (a) Controller structure (b) 2-bit counter structure and timing diagram (c) 2-to-4 decoder structure and timing diagram

be considered as a “mod 2n counter”.

The 2-to-4 decoder shown in Fig. 4.3 (c) generates 4-bit control signals (T0, T1, T2, T3) from input signals (B0, B1). The 2-bit counter and the 2-to-4 decoder produce 4-bit control signals (T0~T3) corresponding to FBD0 and FBD1. As a decoder, this circuit takes an n-bit binary number and produces an output on one of 2^n output lines. As the four outputs, T0 to T3 are phase shifted by90 degrees with regards to each other. If we use this circuit as a demultiplexer, we want to add data latches as the outputs to retain each signal while the others are being transmitted. However, this does not apply when we are using this circuit as a decoder.

Fig. 4.4 shows the timing diagrams for full-, half- and quarter-rate operations. For full-rate operation, only T0 is high. For half-rate operation, T0 and T1 signals periodically alternate between high and low having the opposite condition, and other bits are kept low. For quarter-rate operation, only one bit of 4-bit control signals (T0~T3) is sequentially high while others are low. The 4-bit control signals simultaneously control each MUX in the MRBPD.

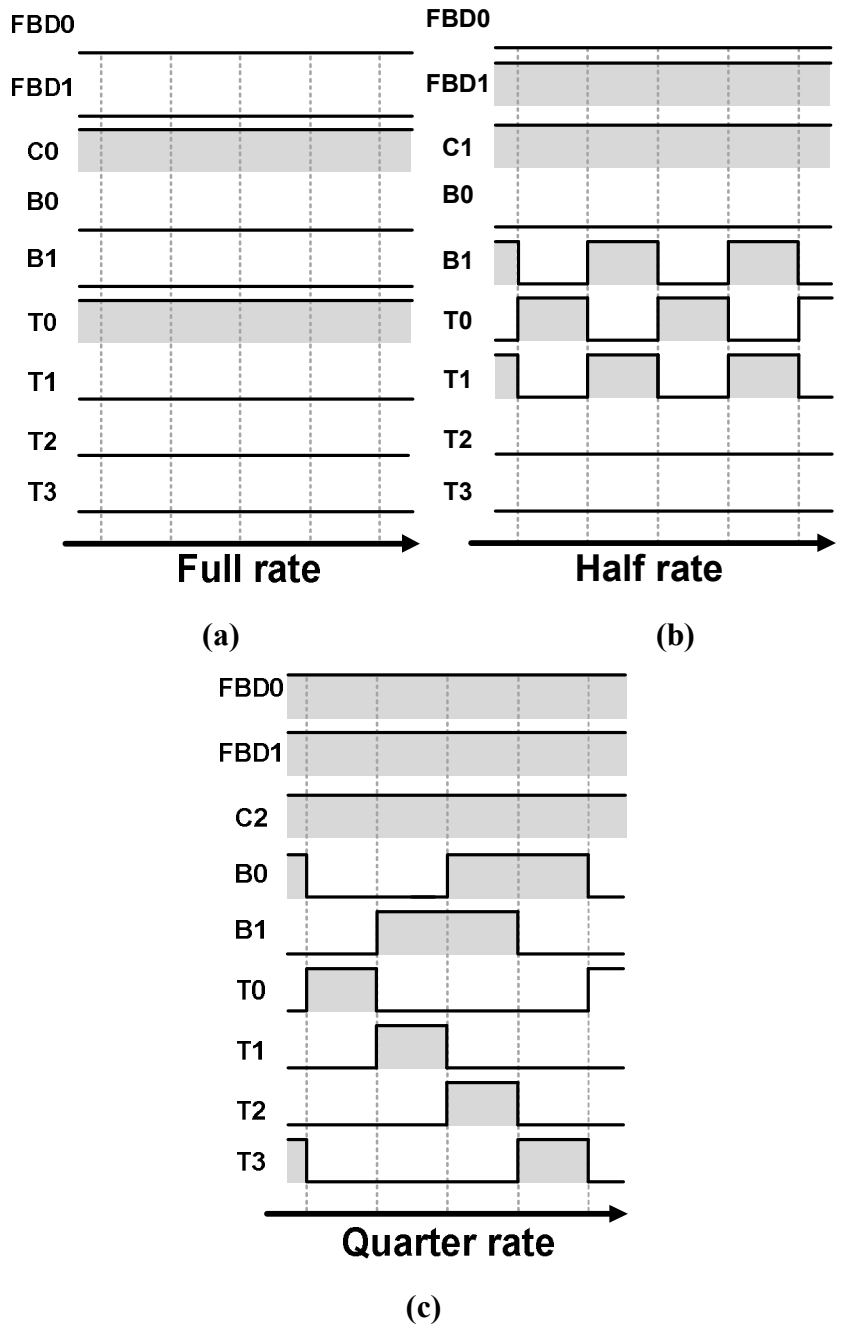
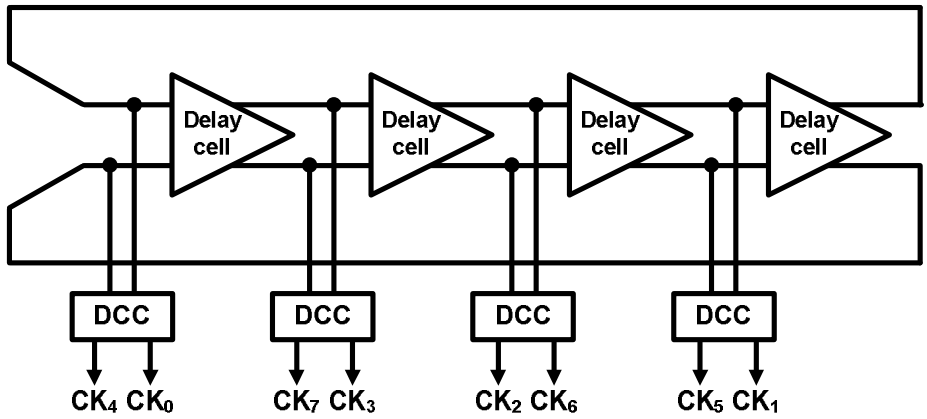


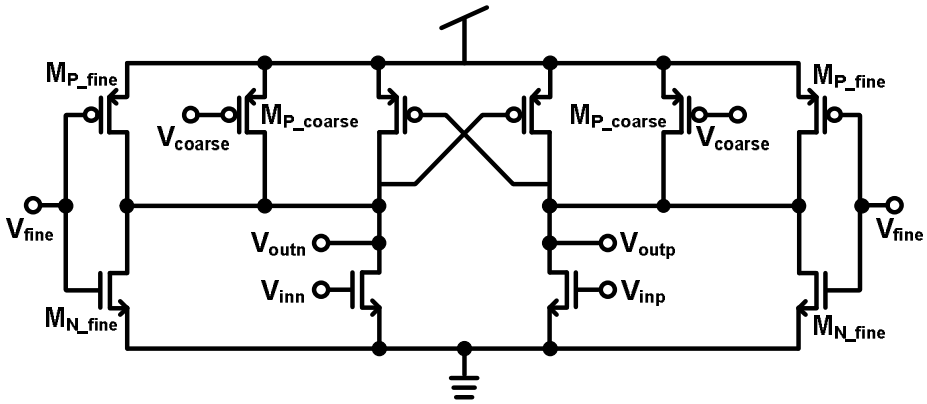
Fig. 4-4. Timing diagram of the (a) Full-rate operation, (b) Half-rate operation, and (c) Quarter-rate operation

4.4. Voltage Controlled Oscillator

Fig. 4.5 (a) shows the schematic to the 4-stage pseudo-differential ring-type VCO with lee-kim delay cell used in our design. The VCO has two control nodes, coarse tuning node for frequency acquisition and fine tuning node for phase acquisition as shown in Fig. 4.5 (b). A coarse tuning node is controlled by externally supplied voltage. Coarse tuning frequency can be determined by M_{P_coarse}. For our design, the output frequency of VCO can be tuned from 1.5GHz to 5.0GHz with an external coarse tuning node voltage. This tuning range can satisfy the target frequency (3.5GHz) regardless of the process condition as shown in Fig. 4.6 (a). A fine tuning node is connected to CDR loop filter and fine tuning frequency can be determined by M_{N_fine} and M_{P_fine}. It is important to achieve the same gain over all frequency tuning range, which changes the loop bandwidth of the CDR circuit and reduces phase margin that is significant for stability. For this reason, it is desirable to minimize the variation of K_{VCO} across all the tuning range. The K_{VCO} of our CDR is about 350MHz/V as shown in Fig. 4.6 (b). In case of phase noise performance, the lee-kim delay cell has better than fully differential delay cell as explained in [36]. However, lee-kim delay cell has problem having the duty-cycle distortion. The

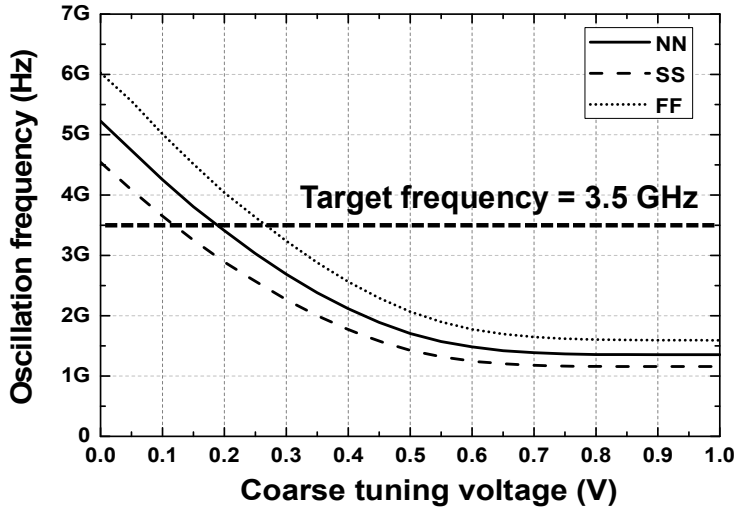


(a)

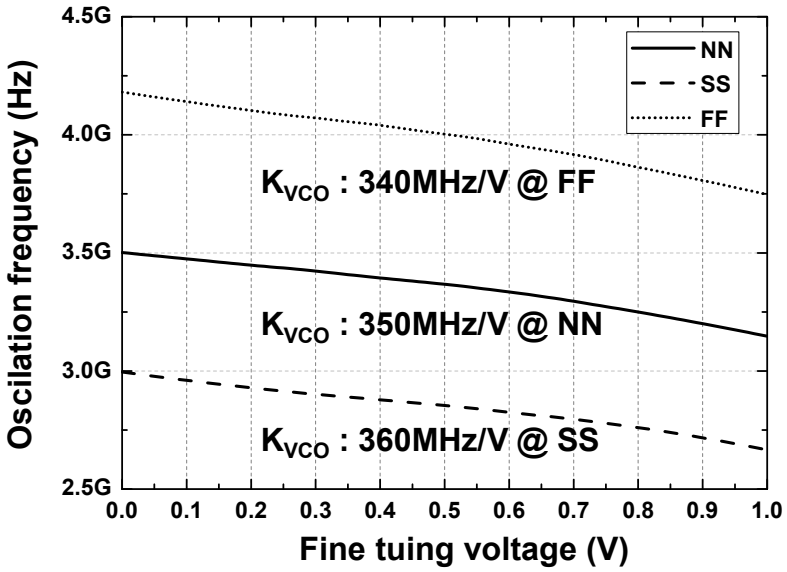


(b)

Fig. 4-5. (a) VCO structure (b) Lee-Kim delay cell



(a)



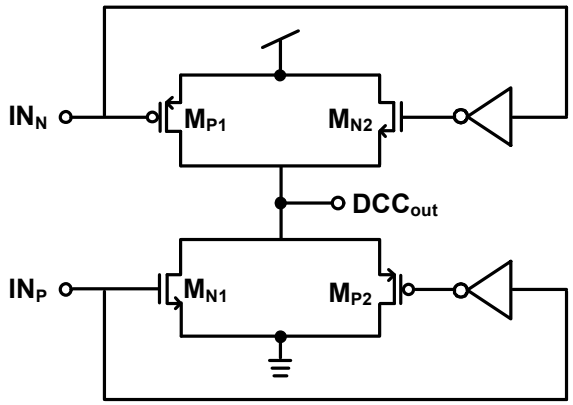
(b)

Fig. 4-6. Simulation result of (a) Frequency tuning range and (b) K_{VCO} in VCO

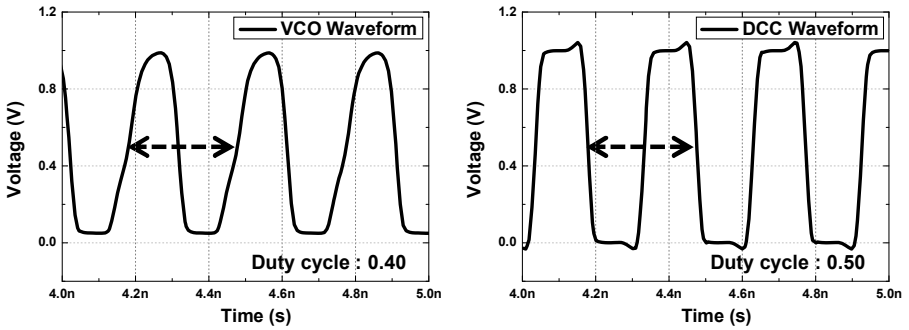
duty cycle distortion can lead to timing margin reduction. Because the rising and falling edge of the clock utilize for edge detection and data retiming in the full-rate CDR.

To prevent this problem, our VCO need to use a feedforward type duty-cycle corrector [37] as shown in Fig 4.7 (a). The duty-cycle corrector utilizes multiphase signals generated from 4-stage differential VCO. The signal IN_N in Fig. 4.7 (a) selected from the multiphase signals turns on M_{P1} and M_{N2}, and charges DCC_{out} output node of the duty-cycle corrector at a moment, because the discharge path of the node DCC_{out} is already off due to the signal IN_P. The signal IN_P is also selected from the multiphase signals is the one whose rising edge is shifted by 180° in phase from that of IN_N. Likewise, the signal IN_P rapidly discharges the node DCC_{out} and delivers the desired 50% duty-cycle signal. As the duty-cycle correction circuit consists of two transmission gates and two inverters, the area is minimal and the power consumption is negligible. Fig. 4.7 (b) shows the waveform compared to VCO output and DCC output. The duty cycle of VCO waveform is about 0.40, while that of DCC waveform is about 0.50.

Fig. 4.8 shows the 8-phase clock waveform. The phase difference of VCO 8-phase is 45 degree because of realizing 4-stage VCO.



(a)



(b)

Fig. 4-7. (a) DCC structure (b) Waveform improvement by using DCC

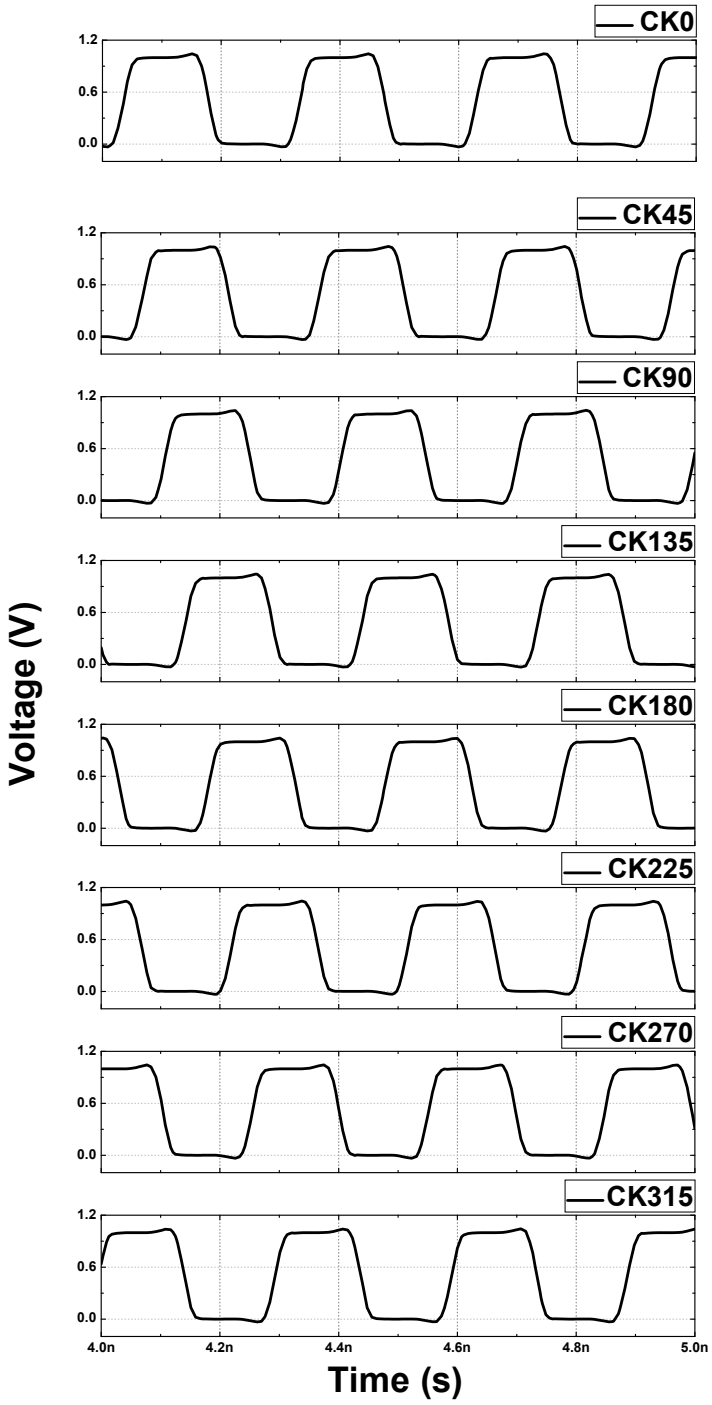
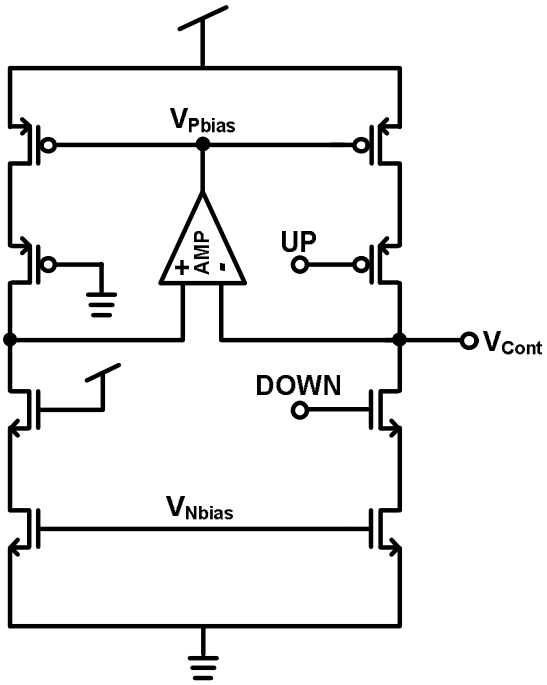


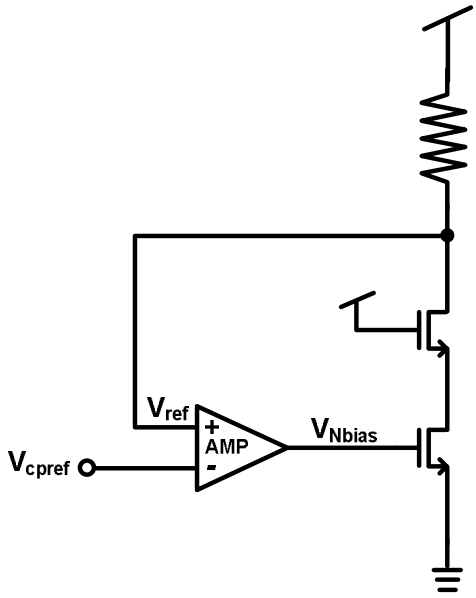
Fig. 4-8. Multi-phase VCO clock waveforms

4.5. Charge Pump & Frequency Divider

The block diagram of charge pump is shown in Fig. 4.9 (a) [38]. A charge pump generates the current to compensate the phase error between received data and recovered clock. And current generating the charge pump drives the control voltage of the voltage controlled oscillator (VCO). When the up pulse is generated from the XOR, the current charges the loop filter and when the down pulse is generated from XOR bar, the current discharges the loop filter. Conventional CMOS charge pump circuits have some current mismatch characteristics. The current mismatch of the charge pump generates static phase error when the CDR circuit is locked. This phase error makes the frequency harmonics at the control voltage. As a result, frequency harmonics is generated a jitter. To reduce the mismatch current, we used a charge pump with the replica path and feedback amplifier in our design. The transistor size of the left side circuit is the same as the right side circuit at the charge pump circuit. Charge pump current is determined by V_{Nbias} generated form the charge pump bias circuit. The output voltage of the amplifier in the charge pump adaptively generates V_{Pbias} to minimize the charge pump mismatch current under charge pump output voltage variation and process



(a)



(b)

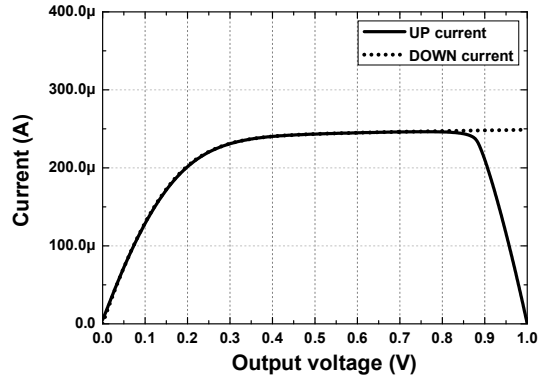
Fig. 4-9. Structure of the (a) Charge pump circuit and (b) Bias circuit

variation. Fig. 4.9 (b) shows the charge pump bias circuit. The gate voltage V_{Nbias} is controlled so that V_{cpref} and V_{ref} are equal to each other using the feedback system. Thus, we can control V_{Nbias} by changing the V_{cpref} voltage.

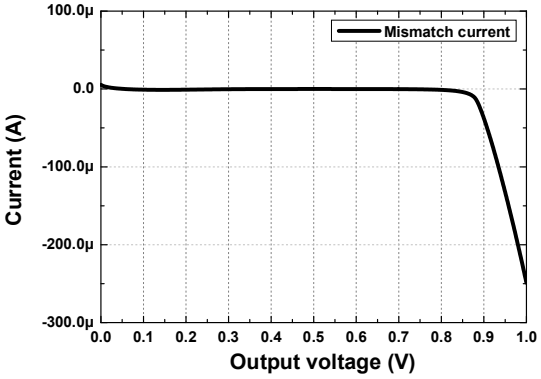
Fig. 4.10 (a) and (b) shows the current mismatch according to the output voltage variations of the charge pump circuit. When the UP and DOWN signal pulse enter the charge pump circuit, V_{Cont} node is changed voltage from 0V to 1V to measure the UP current and the DOWN current. From the simulation result, charge pump current 250uA and mismatch current is 10nA at 0.5V output voltage.

The leakage current according to the output voltage variations of the charge pump circuit is shown as Fig. 4.10 (c). When the UP and DOWN signal pulse enter the charge pump circuit, V_{Cont} node is changed voltage from 0V to 1V to measure the leakage current. From the simulation result, charge pump current 25pA all over the output voltage.

The structure of our frequency divider is shown in Fig. 4.11 (a). It has TSPC divider, 2-to-4 decoder, invertor, and 4:1 MUX. The frequency divider generates CK/8, CK/16, CK/32, and CK/64 dividing clocks from VCO clock signal. It is necessary to make the rotational signals (T0~T3) in the controller. Output clock of frequency divider



(a)



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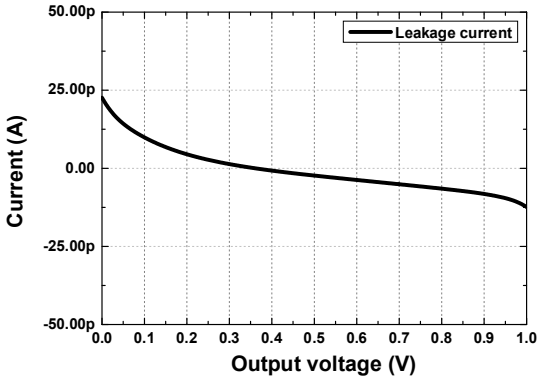


(c)

Fig. 4-10. Simulation of the (a) UP and DOWN current, (b) Mismatch current, and (c) Leakage current

determines the rotating period time of MRPBD. Therefore, to confirm the performance of MRBPD according to rotational period time, the period time is controlled by externally supplied DIV0 and DIV1.

At a static complementary CMOS logic D flip-flop, there are high fan-out load, and signal delay increases. Therefore, the speed of the static complementary CMOS logic D flip-flop is limited. It is not appropriate for high speed operation. The dynamic logic D flip-flop TSPC (True Single Phase Clock) is used at our CDR. The TSPC has two operation modes: the hold mode and evaluation mode. In the hold mode called pre-charge mode as shown Fig 4-11 (b), CK is low, and A node is pre-charged to a certain value due to input data, and B node goes to VDD. The Q node becomes floating as M_{P4} and M_{N4} transistors are turned off. In the evaluation mode as shown Fig 4-12 (c), CK is high, and if A node is pre-charged to VDD, then B node is discharged and the M_{P4} transistor pulls up the Q node. If A node is pre-charged to VSS, then B node is not discharged, and the M_{N4} and M_{N5} transistors pull down the Q node. The timing diagram of TSPC is illustrated in Fig 4.11 (d). The gray region indicates that the TSPC logic has floating nodes when it operates.

Fig 4.12 shows the simulation result of the frequency at each divider output node and the simulation waveform of the frequency

divider. When the output frequency of VCO is 3.5GHz, the output frequency of 8 divider, 16 divider, 32 divider, and 64 divider are 437 / 218 / 109 / 54 MHz respectively.

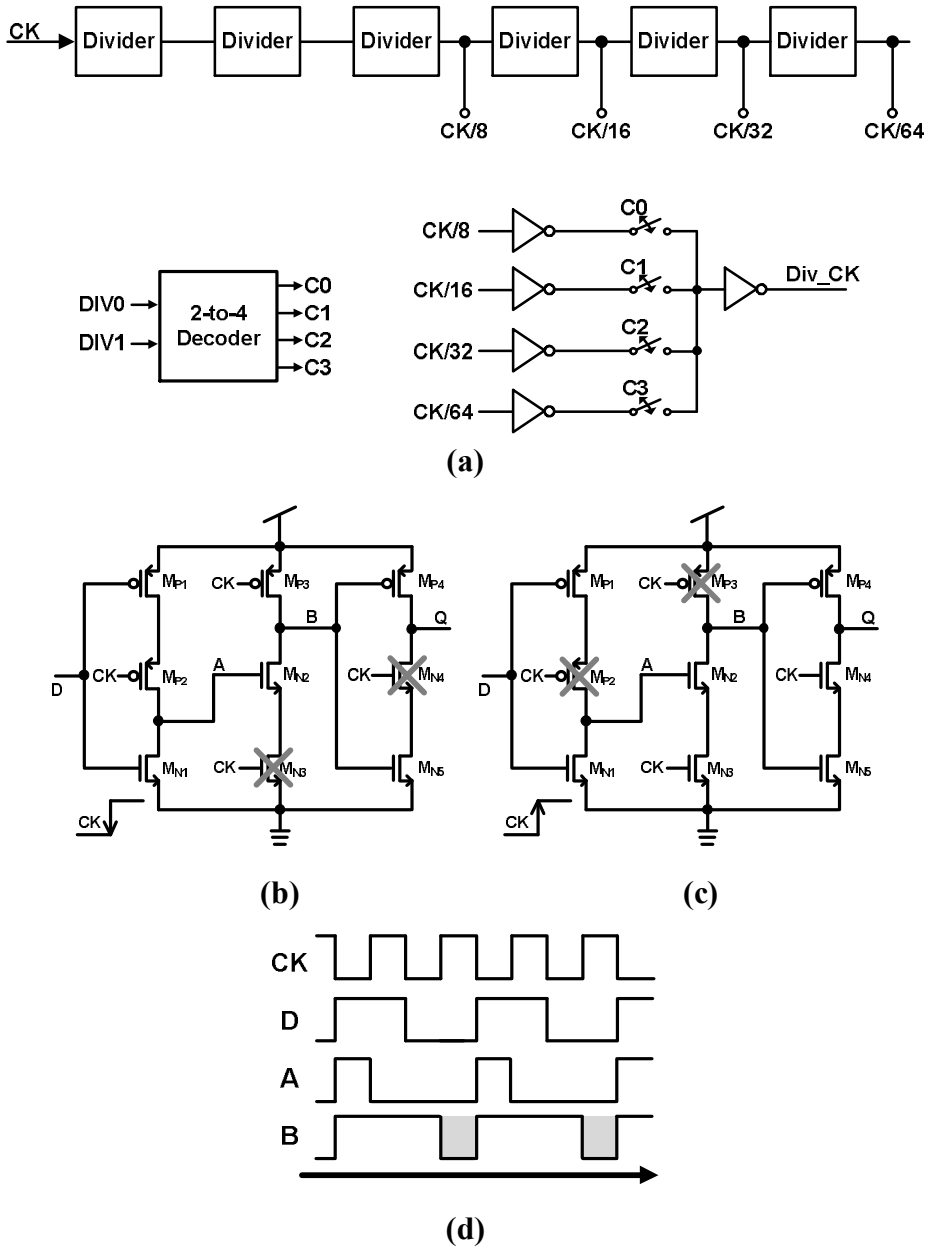


Fig. 4-11. (a) Frequency divider structure (b) TSPC operation of hold mode (C) Evaluation mode (d) Timing diagram of TSPC operation

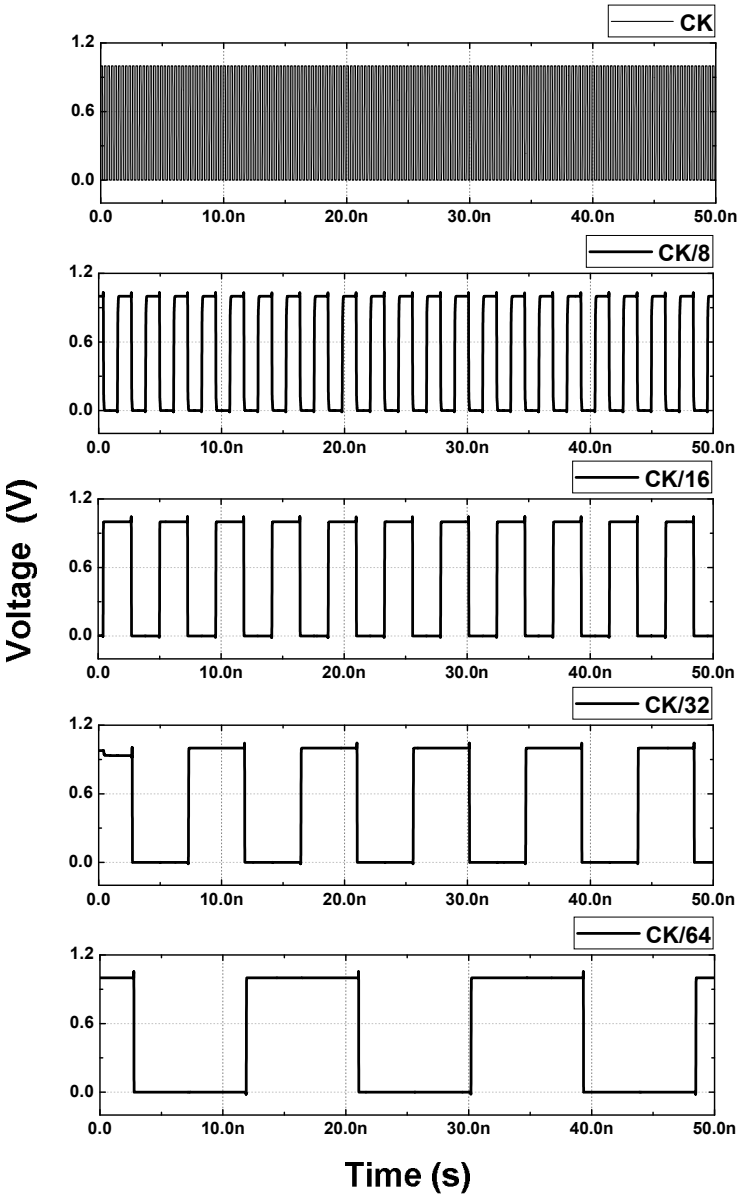


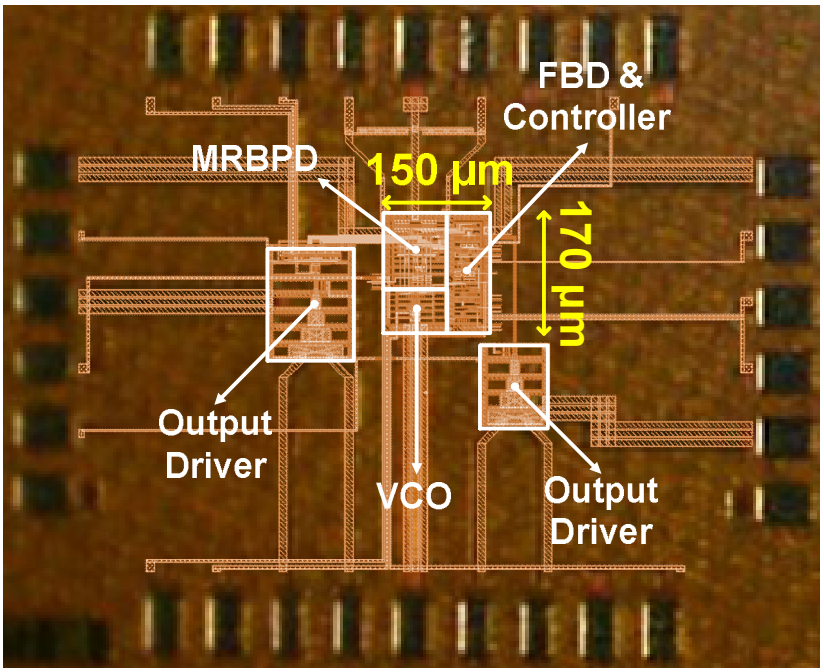
Fig. 4-12. Simulation waveforms of frequency divider

5. Experimental Results

Fig. 5.1 shows the die photograph of our multi-rate CDR realized in Samsung 65-nm CMOS technology. It occupies 0.025 mm^2 except for the output drivers. The total circuit consumes 9.0mW excluding output drivers for 14.0-Gb/s operation with 1.0V supply voltage. Each of MRBPD and VCO consumes 4.0mW. The FBD and controller consume 1.0mW.

The measurement set up for evaluating CDR performance is shown in Fig. 5.2. The chips are mounted on printed circuit board (PCB) with wire bonding. A pulse pattern generator (PPG) produces 3.5-/7.0-/14.0-Gb/s PRBS 2^{11}-1 data, and recovered clock and data are measured by a digital sampling oscilloscope and a signal source analyzer. The bit error rate tester (BERT) checks if the CDR produces any errors when jitter are injected input data.

First of all, we measured the performance of VCO to check the operation frequency range of CDR and process corner of the fabricated chip. Fig. 5.3 (a) shows the range of VCO with coarse voltage tuning. For this measurement, the fine tuning voltage is fixed to 0.5V, and the coarse tuning voltage is controlled by external voltage source. The VCO oscillation frequency range is shown in Fig. 5.3 (a). The process



	Chip area	Power
MRBPD	**0.011 mm^2**	**4.0 mW**
VCO	**0.006 mm^2**	**4.0 mW**
FBD & Controller	**0.008 mm^2**	**1.0 mW**
Output Driver	**0.010 mm^2**	**20.0 mW**

Fig. 5-1. Chip microphotograph

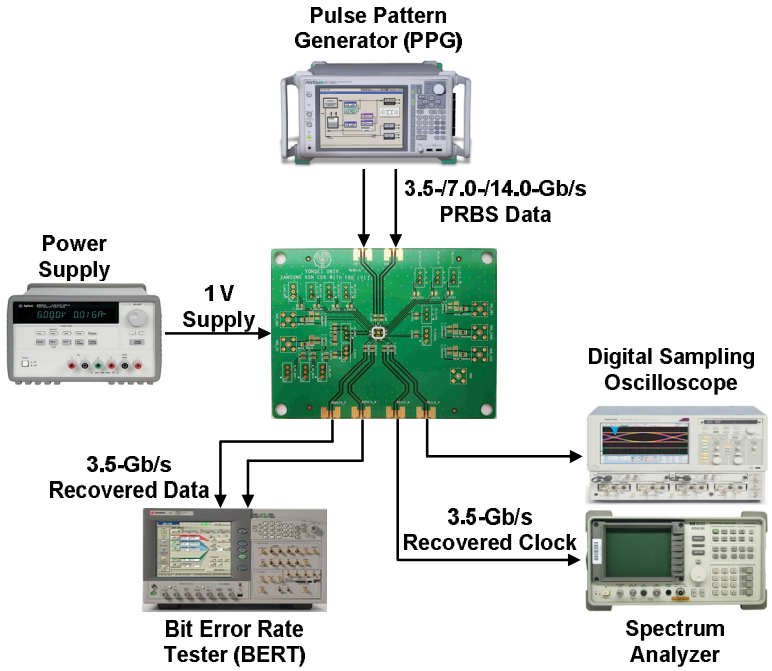
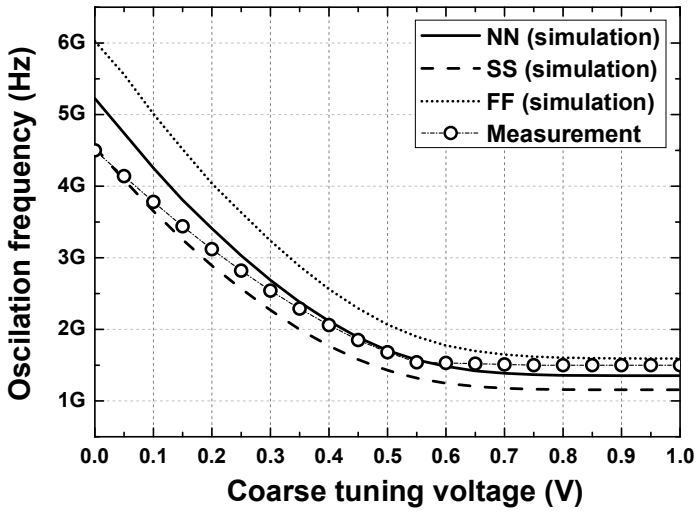


Fig. 5-2. Measurement setup

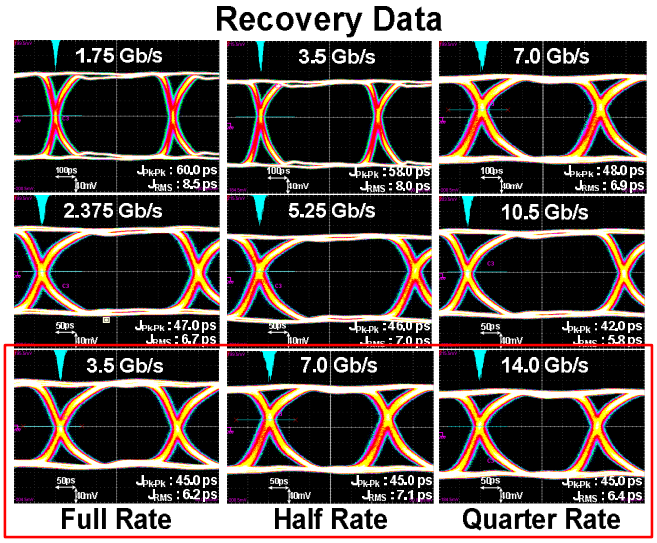
corner of the fabricated chip is approximately between Normal/Normal corner and Slow/Slow corner.

Fig. 5.3 (b) shows measured eye diagrams for the recovered data for full-, half-, and quarter-rate operation with 3.5-, 7.0-, and 14.0-Gb/s input data. For this measurement, the 3.5-, 7.0-, and 14.0-Gb/s 2^{11}-1 PRBS pattern is used. Since recovered output data are de-multiplexed by the MRBPD, output data shown in Fig. 5.4 are 3.5-Gb/s regardless of the input data rate. The recovered data for full-/half-/quarter- rate operations have peak-to-peak jitter of 45.0/45.0/45.0ps and RMS jitter of 6.2/7.1/6.5ps, respectively. The rms jitter of recovered data is almost same as that of the recovered clock. The BER is less than 10^{-12} for all three types of operation.

The recovered clock spectrum is measured by the spectrum analyzer. Fig. 5.4 (a) shows the phase noise the recovered clock for full-, half-, quarter-rate operations with 3.5-, 7.0-, and 14.0-Gb/s input data. The loop bandwidth of the CDR circuit can remain constant regardless of the operation mode. The reason for the constant loop bandwidth is that the same phase detector gain according to operation mode as explained in chapter 3.2.3. Fig. 5.4 (b) shows the phase noise the recovered clock according to rotational frequency to quarter-rate operations with 14-Gb/s input data. The phase noise of the CDR circuit can remain

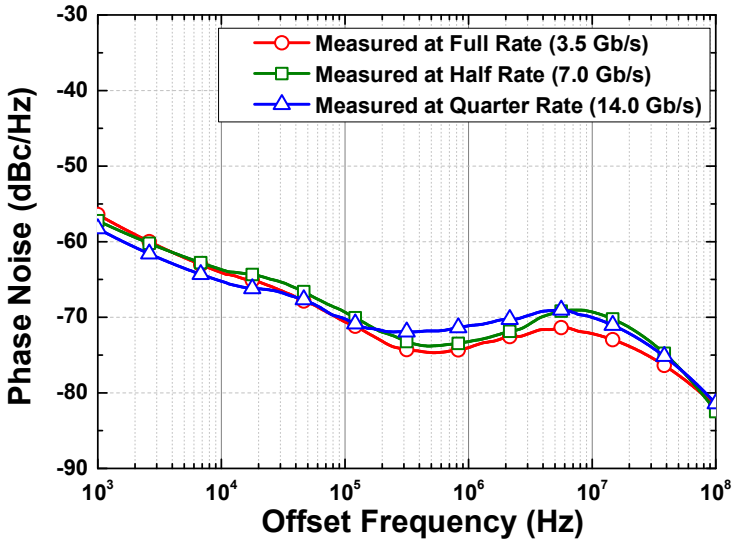


(a)

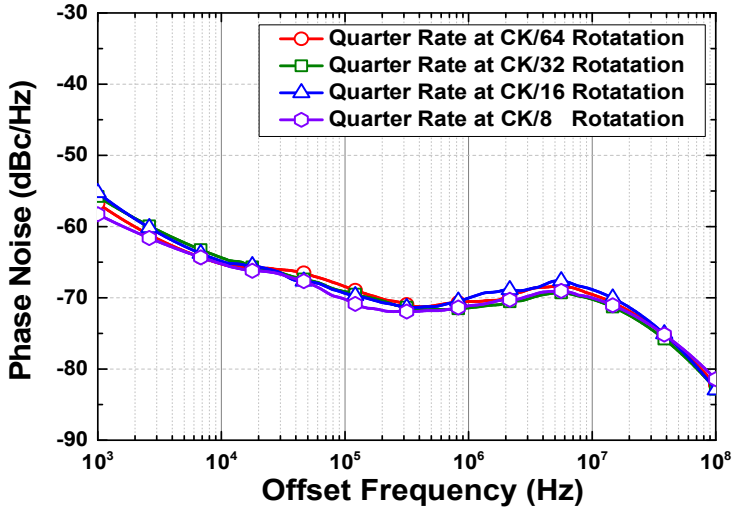


(b)

Fig. 5-3. (a) Measurement result of oscillation frequency range in VCO (b) Measured recovered data to full-, half-, and quarter-rate operation



(a)



(b)

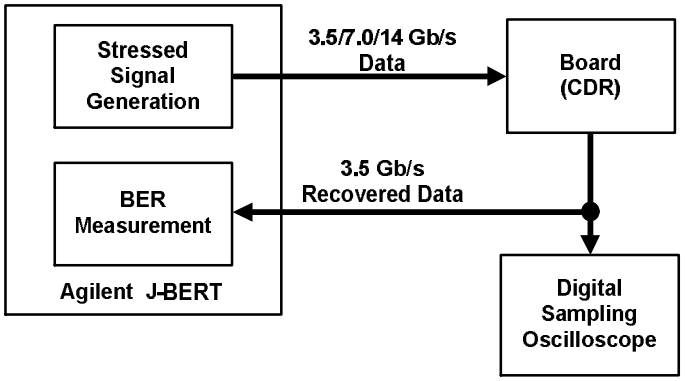
Fig. 5-4. (a) Measured phase noise to full-, half-, and quarter-rate operation (b) Measured phase noise according to rotational frequency

constant regardless of the rotational period time. Because the rotational frequency is much faster than the CDR loop bandwidth.

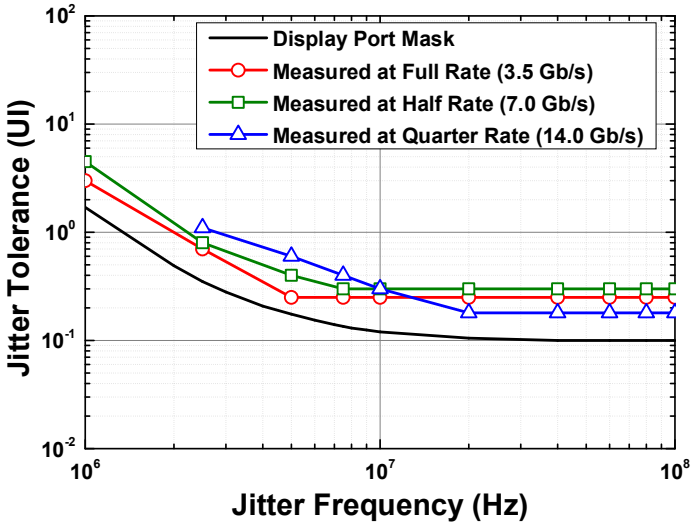
The jitter tolerance test setup is shown in Fig 5.5 (a). The jitter tolerance shows the CDR ability to sustain a 10^{-12} BER under the stressed signaling conditions. Jitter tolerance test has been conducted by following the compliance test specifications and Fig. 5.5 (b) shows the measured jitter tolerance plots for full-, half-, quarter-rate operations with 3.5-, 7.0-, and 14.0-Gb/s input data. The jitter tolerance is measured at 10^{-12} with 2^{11}-1 PRBS with Agilent N4903B J-BERT. This outputs 2^{11}-1 PRBS pattern as defined in specification with Rj (random jitter), ISI (inter symbol interference), and Sj (sinusoidal jitter) jitter injected. 2^{11}-1 PRBS is sufficient for many display interface applications where 8B10B encoding is employed. By the DisplayPort 1.2 compliance test specification (CTS) [39], the injecting jitter frequencies for jitter tolerance test are 2MHz, 10MHz and 100MHz. During the test the total jitter components (ISI+Rj+Sj) at different sinusoidal jitter (Sj) frequencies are generated by the stressed signal generator as specified by the CTS. Clearly, our CDR satisfies the jitter tolerance requirement for DisplayPort. Due to the limitation of the jitter generation equipment at lower jitter frequency, the jitter amplitude at the frequency lower than 1MHz could not be generated [40]. Therefore

the jitter tolerance was measured only over 1MHz jitter frequency.

Table 5-1 shows performance comparison for our CDR with previously reported multi-rate CDRs. The energy efficiency of our CDR is 0.64 pJ/bit and its total power consumption is 9 mW for 14.0-Gb/s operation. Our CDR achieves the smallest chip area and lowest power consumption.



(a)



(b)

Fig. 5-5. (a) Jitter tolerance measurement setup (b) Measured jitter tolerance graph to full-, half-, and quarter-rate operation

TABLE 5-1
PERFORMANCE SUMMARY AND COMPARISON

	This work	2015 [25]	2012 [27]
Data rate (Gb/s)	3.5/7.0/14.0	1.62/2.7/5.4/8.1	1.62/2.7/5.4
Technology (nm)	65	90	130
Supply Voltage (V)	1.0	1.2	1.2
Power (mW)	9.0 @ 14 Gb/s	80.4 @ 8.1 Gb/s	104.4 @ 5.4 Gb/s
BER	< 10-12	< 10-12	< 10-12
Core Area (mm2)	0.025	0.23	0.44
RMS Jitter (ps)	6.40 @ 14 Gb/s	5.52 @ 8.1 Gb/s	3.21 @ 5.4 Gb/s
Power Efficiency (pJ/bit)	0.64	9.92	19.30

6. Conclusion

This paper presents a 3.5/7.0/14.0-Gb/s multi-rate CDR having a multi-mode rotational bang-bang phase detector and a frequency band detector. A multi-mode rotational bang-bang phase detector supports full-, half- and quarter-rate operations to achieve the multi-rate operation with a single VCO. The frequency band detector enables the selection of the desired frequency band without any external signals. To the best of our knowledge, this is the first report of a multi-rate CDR having a single PD that can operate at three different data rates without multiple VCOs, resulting in reduced power consumption and chip area. It is experimentally demonstrated that our CDR successfully satisfies requirements for various display interface applications.

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국 문 요 약

다중 모드 Bang-Bang 위상 검출기와 주파수 대역 검출기를 가진 다중 속도 데이터 복구 회로

데이터 복구 회로는 수신기 설계에 있어 매우 중요한 역할을 담당하고 있다. 따라서 높은 동작속도, 낮은 전력소모, 그리고 다양한 속도로 동작할 수 있는 데이터 복구 회로의 설계는 오래 전부터 연구가 되어 왔다.

본 논문은 새로운 구조의 다중 모드 Bang-Bang 위상 검출기와 주파수 대역 검출기를 사용하여 다양한 속도로 동작하면서 구조적으로 간단하고 적은 면적을 차지할 뿐만 아니라 낮은 전력소모를 할 수 있는 다중 속도 데이터 복구 회로를 제안하였다.

삼성 65-nm CMOS 공정을 사용하여 칩을 제작하였으며, 다중 모드 Bang-Bang 위상 검출기의 다양한 모드 동작과 주파수 대역 검출기의 검출 특성 모두가 성공적으로 동작하는 것을 실험을 통해 확인하였다. 또한 3.5-, 7.0-, 14.0-Gb/s 2^{31}-1 PRBS 입력에 대해서 안정적으로 동작하며 복원된 데이터는 0.02UI 의 rms 지터 성능을 가지는 것을 확인하였다. 복원된 데이터 또한 에러가 없음을 확인하였다.

핵심 단어: 데이터 복구 회로, Bang-Bang 위상 검출기, 주파수 대역 검출기, 다중 모드 동작

List of Publications

International Conference Presentations

[1] **Ki-Hyun Pyun,** Dae-Hyun Kwon and Woo-Young Choi, "A 3.5/7.0/14-Gb/s Multi-Rate Clock and Data Recovery Circuit with a Multi-Mode Rotational Binary Phase Detector" *IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*, Oct. 2016, Jeju, Korea.

Domestic Conference Presentations

[1] **Ki-Hyun Pyun**, Dae-Hyun Kwon and Woo-Young Choi, “A 3/6/12-Gb/s Multi-Rate Clock and Data Recovery Circuit with a Multi-Mode Rotational Bang-Bang Phase Detector,” *제 23회 반도체 학술대회*, Feb. 2016, 정선.